



# DESIGN AND ANALYSIS OF A 3-BIT RF MEMS TUNABLE CAPACITOR

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## ABSTRACT

A 3-bit radio frequency microelectromechanical (RF MEMS) tunable capacitor with electrostatic actuation and a wafer-level package is presented. The structure is made of Au with SiN as an isolation layer. According to one-port measurements, capacitance range is from 0.6 to 1.4 pF and minimal resistance is 0.5 Ohm. Maximum obtained Q-factor is 60 at 6.5 GHz. Q-factor at low frequencies is limited by a low shunt resistance. Activation voltage is 14 V. The capacitor suffers from dielectric charging effect.

**Keywords:** RF MEMS, microelectromechanical devices, RLC circuits, Switched capacitor circuits, tunable circuits, devices.

## 1. INTRODUCTION

RF MEMS tunable capacitors have a wide range of applications in various frequency tuning circuits in RF devices. The advantages of RF MEMS tunable capacitors are low insertion loss, low power consumption and potentially low cost. The main difficulty in the development of RF MEMS devices is their reliability, particularly in terms of the problem of dielectric charging [1].

Because of its electromechanical nature, continuous tuning in a simple planar structure is impossible. Cantilever passes about 1/3 of the air gap before pull-in [1]. There are methods to increase tuning range: relatively simple multi-bit [2] [3], non-planar two-stage [4], zipping effect [2], dual-anchor [5]. Capacitor presented in this paper uses the multi-bit method.

The latest attempts to fabricate RF MEMS elements show the following trends: low [6] and ultralow [7] activation voltage, use of CMOS process [7], use of CMP to achieve better capacitance ratio [6], thick metal process for high power applications [8].

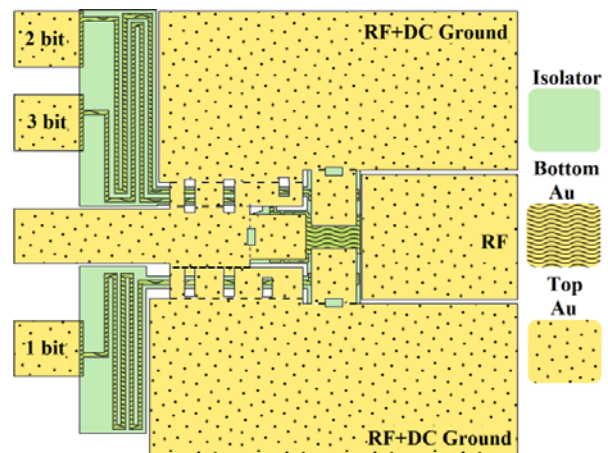
The aim of this work was to create a high-Q tunable capacitor of a relatively simple planar structure with a low activation voltage. This paper presents the designed and fabricated metal RF MEMS tunable capacitor on a high-resistivity silicon substrate. Measurement results of the device RF parameters in a wide frequency range are reported.

## 2. CAPACITOR DESIGN

A shunt 3-bit tunable RF MEMS capacitor has been designed.

The device topology is presented in Figure-1. It is based on three equal-width cantilevers that are connected to CPW ground lines hanging over the CPW central line. A dielectric layer is deposited on the central line and the actuation electrodes. Each cantilever has its own actuation electrode. The overlap areas between the cantilevers and the central line relate as 1:2:4. Therefore, the capability to combine separate actuations of each cantilever provides  $2^3$  states with different capacitances.

Low activation voltage is achieved by geometry of the cantilever and the activation electrode. Thick metallization provides a high Q-factor.

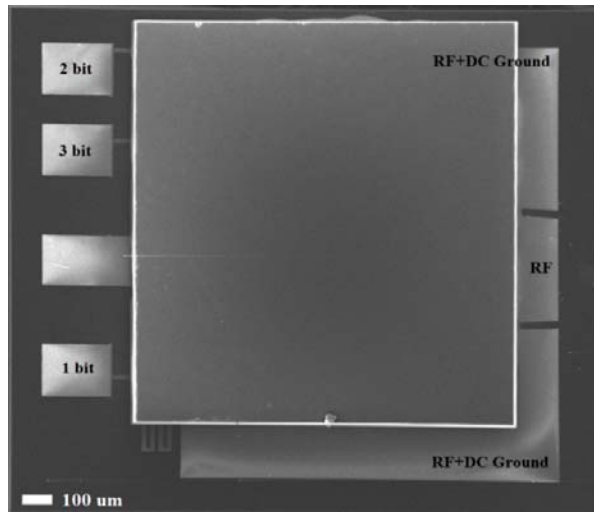


**Figure-1.** Topology of the proposed capacitor.

An additional isolation along the control line is provided by long high-impedance lines and capacitances that are formed between the lines and RF+DC ground.

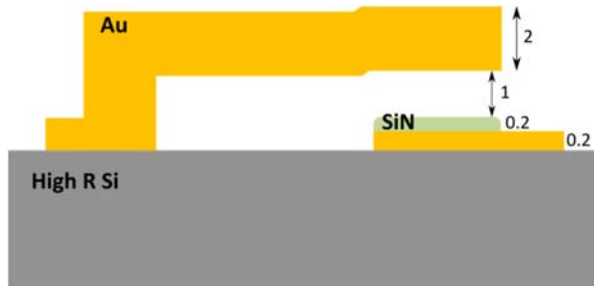
The long CPW transmission line is necessary to provide an adequate space for a package. The wide central line and a narrow gap serve to decrease the effect of the transmission line on the parasitic inductance.

Figure-2 shows the SEM image of the RF MEMS capacitor with a wafer-level package.



**Figure-2.** 3-bit wafer-level packaged RF MEMS capacitor.

The device planar size is  $1.93 \text{ mm} \times 1.72 \text{ mm}$  with 1 mm approximate thickness. Characteristic thicknesses of the structural layers are shown in Figure-3.



**Figure-3.** The capacitor structural layers and their characteristic thickness.

### 3. MANUFACTURING

The capacitor has been manufactured at AirMEMS foundry (France) on a 500 um-thick high-resistivity silicon substrate. The lines and the cantilevers are made of gold, silicon nitride is used as an isolator, and the chip is hermetically packaged. The device has been manufactured using a fabrication technology process developed at AirMEMS. Table-1 contains the measured thicknesses of the fabricated RF MEMS capacitor in comparison with the target values.

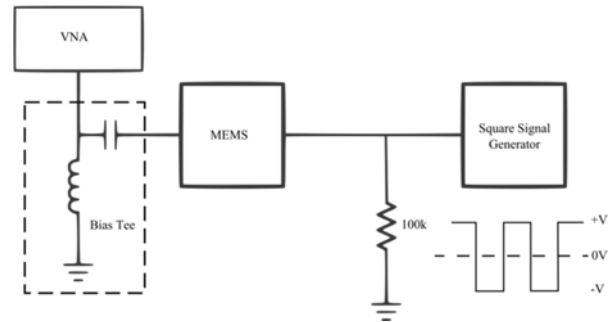
**Table-1.** RF MEMS capacitor layer thicknesses.

Layer	Target thickness, um	Measured thickness, um
Lower metal (Au)	0.2	0.19 – 0.21
SiN	0.2	0.18 – 0.2
Sacrificial (buffer) layer	1	1 – 1.1
Cantilever (Au)	2	2.2 – 2.4

### 4. CAPACITOR PERFORMANCE

The fabricated capacitor has been measured using a wideband one-port measurement system in 0.01 GHz – 20 GHz frequency range comprising a vector network analyzer, a probe station for on-wafer tests and a waveform generator.

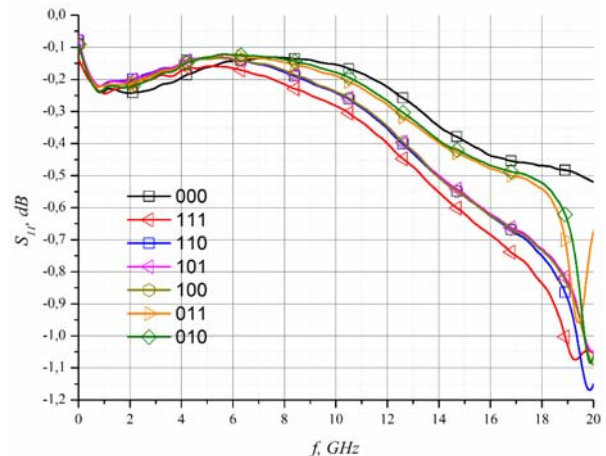
Figure-4 shows the diagram of the measurement setup.



**Figure-4.** Experimental setup.

The measured value of the activation voltage has been found to be 14 V.

Appropriate activation electrodes were supplied with voltage 14 V or 0 V and  $S_{11}$  has been measured. Figure-5 shows the  $|S_{11}|$  parameters in all states from 000 (minimum capacitance) to 111 (maximum capacitance).



**Figure-5.**  $|S_{11}|$  parameters of the RF MEMS capacitor.

Impedance of the capacitor is formulated as follows:

$$Z = 50 \frac{1 + S_{11}}{1 - S_{11}}$$

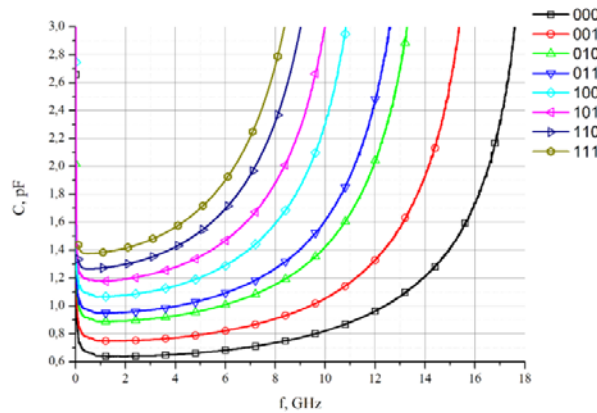
Capacitance and resistance of the device are:

$$C = -\frac{1}{2\pi f \operatorname{Im} Z}$$

$$R = \operatorname{Re} Z$$

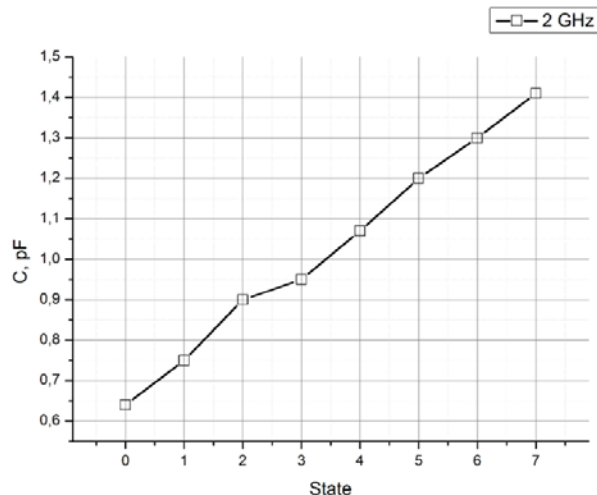


Because the capacitor is not an ideal device, there is a frequency dependence of the capacitance, which is due to the presence of parasitic characteristics. The capacitance is shown in Figure-6.



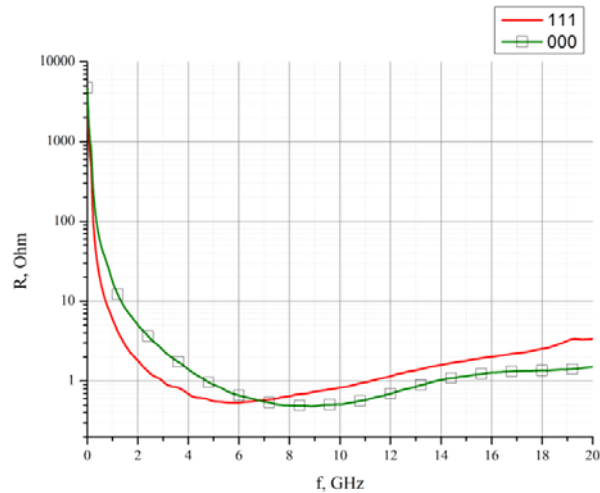
**Figure-6.** Capacitance of the RF MEMS capacitor.

In order to illustrate a linear change in the capacitance depending on the state, graph capacitance at 2 GHz is plotted in Figure-7. The capacitance changes from 0.64 pF to 1.41 pF with increments of 0.1–0.15 pF.



**Figure-7.** Capacitance of the RF MEMS capacitor at 2 GHz.

The dependence of the resistance of the capacitor in two states (000) and (111) is shown in Figure-8.



**Figure-8.** Resistance of the RF MEMS capacitor.

The capacitor also suffers from dielectric charging effect, which is reflected in the change of activation voltage, but detailed research has not been conducted.

## 5. ANALYSIS AND DISCUSSIONS

Consider the obtained frequency dependences of the capacitance (Figure-6) and resistance (Figure-8). Hyperbolic increase in the capacitance is explained by the existence of parasitic inductance. Increased resistance at high frequencies is explained by the resistivity of gold and the skin-effect. The increase in resistance at low frequencies is likely to be connected with low shunt resistance through substrate. In the low-frequency limit, impedance of the capacitance is infinite, but impedance of the shunt resistance is slightly frequency-dependent and finite. Therefore, the capacitor alters its nature from capacitive to resistive. It also explains the sharp increase in the capacitance near 0 GHz in Figure-6.

The capacitance of a plane-parallel capacitor and air-dielectric gap is described by

$$C(h) = \frac{\epsilon_0}{h + d/\epsilon}$$

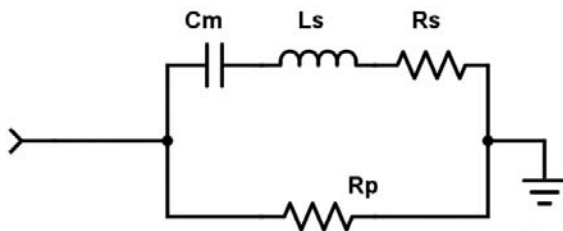
where  $h$  is the thickness of the air gap,  $d$  is the thickness of the dielectric,  $\epsilon$  is the relative permittivity. Silicon nitride permittivity is equal to 7.5 and thickness is equal to 0.2  $\mu\text{m}$ . In the case of minimal capacitance  $h = 1 \mu\text{m}$ , and in the case of maximum capacitance  $h = 0 \mu\text{m}$ . In fact, the minimal air gap is limited to the roughness of the deposited films and the maximum value of the capacitance is substantially reduced.

Considering the areas of overlap obtained using SEM, the capacitance value between the cantilever and the center line can be calculated, as well as the total capacitance. Total capacitance has been calculated using the ideal parallel model. Table-2 contains the calculated capacitances.

**Table-2.** Capacitances.

	S1	S2	S3	$\Sigma$
S, mm <sup>2</sup>	0.0028	0.0055	0.011	
C <sub>min</sub> , pF	0.024	0.048	0.094	0.166
C <sub>max</sub> , pF	0.92	1.84	3.64	6.4

For further analysis, a simple lumped model has been selected. This model should qualitatively illustrate the characteristics of the capacitor considering the features described above.

**Figure-9.** Lumped model of the RF MEMS capacitor.

The model shown in Figure-9 consists of several elements. Cm is the resulting capacitance. Ls is the series inductance, Rs is the series resistance, Rp is the shunt resistance. For the ideal capacitor Rs = Ls = 0, Rp = ∞. Residual:

$$\Delta = \sum_f (\text{Im } Z_{\text{model}} - \text{Im } Z_{\text{real}})^2 + \sum_f (\text{Re } Z_{\text{model}} - \text{Re } Z_{\text{real}})^2$$

The model parameters for the different states are presented in Table 3.

**Table-3.** Parameters of capacitor model.

State	Cmin	Cmax
Cm, pF	0.64	1.37
Ls, nH	0.095	0.143
Rs, Ohm	0.882	1.06
Rp, Ohm	4715	5214
L2 Residual	9.255	5.11

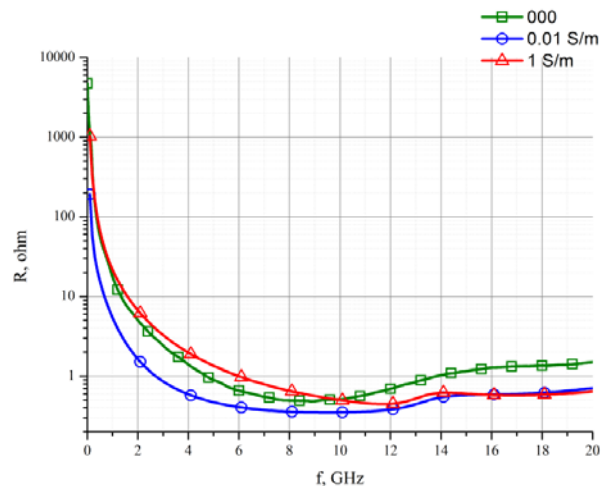
EM simulation of the capacitor in the low capacitance state has been conducted in HFSS program package. The topology and thickness of the layered structure of the capacitor are specified above. The material parameters are as follows: silicon, which is also used for packaging, with permittivity of 11.9. Conductivity is equal to 0.01 S/m which is typical of high-resistivity silicon (R = 10000 Ohm × cm). Conductivity of gold is  $41 \times 10^6$  S/m. Permittivity of silicon nitride is 7.5.

To account for the shunt resistivity, two models have been used: the Low R model has the surface layer of the substrate with conductivity greater than 0.01 S/m and the High R model has no such layer.

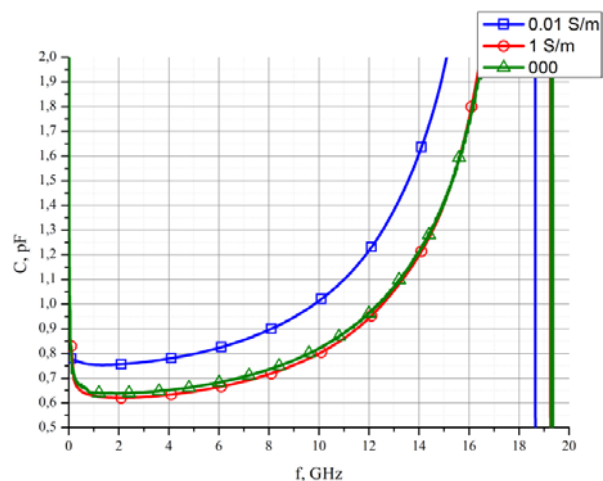
In the Low R model, conductivity and thickness of the surface layer varied.

As a result of the simulation, it has been found that the Low R model with the surface silicon layer thickness of 2 μm and conductivity of 1 S/m has the same resistance at low frequencies and the same capacitance as RF MEMS capacitor. Resistance and capacitance of FEM models and capacitor are shown in Figures 10-11. Significantly increased conductivity of the surface layer can explain experimental results.

Q-factor ( $Q=X/R$ ) suffers from two effects: shunt conductance lowers Q-factor at low frequencies where capacitance is frequency independent, and inductance lowers Q-factor at high frequencies. Maximum obtained Q-factor is 60 at 6.5 GHz, while High R model achieves 86 at 4.1 GHz.

**Figure-10.** Resistance of the RF MEMS capacitor and FEM models.

Capacitor in 000 state (green squares), High R model (blue circles), Low R model (red triangles).

**Figure-11.** Capacitance of the RF MEMS capacitor and FEM models.



Capacitor in 000 state (green triangles), High R model (blue squares), Low R model (red circles).

## 6. CONCLUSIONS

A three-bit packaged RF MEMS varactor has been designed and fabricated; its characteristics have been measured and analyzed. It provides a linear step change in capacitance in the range of 0.64-1.41 pF with increment 0.1-0.15 pF (Figures 6 - 7). Activation voltage is 14 V. Parasitic inductance is about 0.1-0.14 nH (Table-3), which results in the minimum resonance frequency of 12.4 GHz. Quality factor at low frequencies is limited by a low shunt resistance (Table-3) of the surface layer of silicon, since its conductivity has been increased significantly during the manufacturing process. This leads to an active resistance of about 20 Ohm near 1 GHz, while the minimum resistance is 0.5 Ohm (Figure-8).

## ACKNOWLEDGEMENTS

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