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LOW POWER FOLDED CASCODE CMOS OPERATIONAL AMPLIFIER WITH COMMON MODE FEEDBACK FOR PIPELINE ADC

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ABSTRACT

This work proposed a low power and high gain folded cascode CMOS operational amplifier with a common mode feedback (CMFB) for Pipeline ADC. The proposed design is implemented in 0.13-µm Silterra CMOS technology. The folded cascode topology has been used for obtaining a high gain and low power consumption. Meanwhile, the CMFB is modified circuit to be a double detection to stabilize the output of common-mode voltage. The simulation results shown that the DC gain of 64.5dB, unity gain bandwidth (UGB) of 133.1 MHz and a phase margin (PM) of 68.4º have been achieved. The power consumption of 0.3mW in 1.8V power supply with 22.6V/µs of slew rate and 72.4ns of settling time is obtained.

Keywords: CMOS operational amplifier, folded cascode, common mode feedback, pipeline ADC.

INTRODUCTION

Analog-to-digital converter (ADC) is a dominant block in analog or digital mixed signal application. Generally, this block is used as an interface between analog circuits and digital sub-systems that indispensable for wireless telecommunications, instrumentation, medical applications and also audio and video processing. Amongst the variety of ADC structure [1], the pipeline ADC is a good number of favored ADC structure that is designed for sampling and rates which is from a small number of mega samples per second (Msps) and up towards 100Msps with medium to high resolution of 8 to 14bits besides has been proven to be a very efficient architectures for high-speed, low power consumption and medium resolution [2]. The conventional pipeline ADC architecture [2,4] consist of cascade stages which are a low resolution ADC, DAC and also an amplifier. Since the amplifier is basic stages in Pipeline ADC, this paper proposed a low power folded cascode CMOS op-amp with CMFB.

OPERATIONAL AMPLIFIER

The core element and most important elements in Pipeline ADC is the operational amplifier that well known as op-amp. Op-amp has been classified into several topologies which are multi-stage, telescopic and folded cascode [3,5]. All these three topologies have their own advantages and disadvantages.

Multi-stage amplifier is actually a combination of several stages from single stage op-amp since the stages are connected in cascade, i.e. the output of the first stage is connected to form an input of the second stage, whose the output becomes an input for the third stage, and so on [6]. Commonly, this op-amp is implemented on integrated circuits which have a large number of transistors with common matched of the parameters. The advantages of this op-amp topology are increasing the input resistance, reduced the output resistance, increase the gain and capability of power handling while the disadvantage of this topology is difficulty in matching of stages or with other words is for the next stage.

In [5] a telescopic topology is discussed. This topology becomes as telescopic op-amp because the cascades are connected between the power supplies in series with the transistors in the differential pair, where it occurs in a structure where each branch transistor connected directly together in a straight line. Traditionally, telescopic topology has smaller swing because of lesser current legs and produces a smaller power consumption and also lower noise. But this topology will occurred a slowdown in the linear range of operation when the input and output is decreased.

Folded cascade topology is called as 'folded cascode' because it comes from a folding down n-channel cascode active loads of a different-pair and changing the MOSFET to the p-channel [7-8]. These topologies permits the particular input common-mode level of being near to the power supply voltage as well as provide a high output swing, wide input common-mode range and preferably steering in low voltage supply circuits. However, this topology contributed to a greater noise compared to the telescopic op-amp.

CIRCUIT IMPLEMENTATION

The desired op-amp topology is designed with respect to the op-amp specifications as posed in Table-1. Folded cascode topology is ideal to be a main op-amp for this work because the design has been used for obtaining a high DC and fast settling with high unity high gain besides low power consumption [3,8]. Commonly, the folded cascode has been designed with a pair of PMOS type or else NMOS type for the input of the op-amp through the limits of input common mode range [7].

Table-1. Op-amp specifications for pipeline ADC.

Parameter	Value
Power supply	1.8V
V_{in}	±1.2V

V_{out}	1.2V
DC gain	>70dB
Unity gain bandwidth	>130MHz
Phase Margin	>50°

Figure-1 illustrates the proposed folded cascode op-amp architecture with CMFB circuit. The folded cascode op- amp is designed with using NMOS input because these input types give more large output gain compare to PMOS input type. The 1pF of capacitor load also used in this circuit design thus to stabilize the phase of the op-amp circuit.

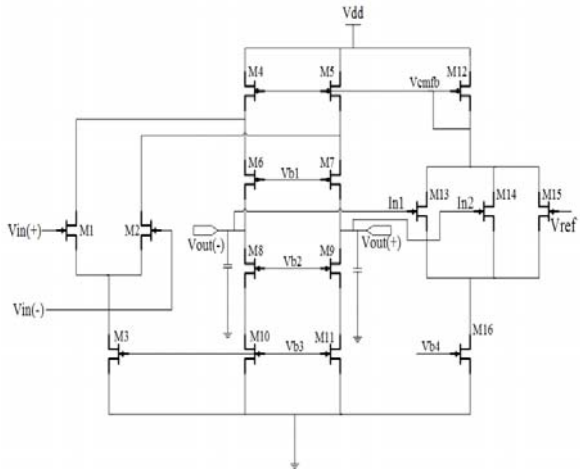

Figure-1. Folded cascode op-amp with CMFB circuit**.**

As can be seen in Figure-1, this amplifier folds the input transistors, which is M1 and M2 to the V_{DD} and the two tail current source are applied at the point of folding, which are between transistor M4, M6 and also transistor of M5, M7. In the interim, the transistor of the M4 and M5 are presented as the DC bias voltage of CMFB circuit. The DC bias voltage that connected to each pair MOS transistor of M6-M7, M8-M9 and M10-M11 will produce a low-voltage cascode. The gain of the folded cascode architecture is given by:

$$A_v = G_m R_o \quad (1)$$

where, G_m is a short-circuit trans conductance of the output current gain across the transistor of M6 that express as:

$$Gm = g_{m1} \quad (2)$$

and R_o is the output impedance of folded cascode op amp and it comes from a parallel combination of the impedances looking into the drains of M6 and M8; where $ß_x = g_{mx}.r_{ox}$. So,

$$R_o = ß_6.(r_{o1}||r_{o4})||(ß_8.r_{o10}) = g_{m6}.r_{o6}.(r_{o1}||r_{o4})||(g_{m8}.r_{o8}.r_{o10}) \quad (3)$$

Thus, the substitution of the Equation. (2) and Equation. (3) into Equation. (1) can be written as:

$$A_v = g_{m1} \{[g_{m6}.r_{o6}.(r_{o1}||r_{o4})] \,||\, [g_{m8}.r_{o8}.r_{o10}]\} \quad (4)$$

Common-mode feedback circuit is presented to stabilize the common-mode voltages for differential-mode circuits [9-10]. There are three techniques that have been used in implementing CMFB circuits [10] which are differential difference amplifier (DDA) CMFB, switch capacitor CMFB and resistor-averaged CMFB. For this op-amp architecture, the differential difference amplifier (DDA) CMFB technique is applied. The CMFB circuit is designed for this op-amp architecture owing to make sure a proper operation of the fully differential op-amp as well as to fix the voltages at high impedance node in the op-amp circuit with the desired values of CMRR performance. The CMFB circuit is modified from Figure-1(a) in [9] to be a double detection CMFB in order to stabilize the output of common-mode voltage for this op-amp design. Such illustrated in Figure-1, the CMFB is used to feedback the outputs of the folded cascode op-amp where the Vout(+) and Vout(-) are fed to the input of In1 at M13 and In2 at M14 of CMFB.

RESULT AND DISCUSSION

The proposed op-amp has been simulated using Cadence spectral. The performances of op-amp are verified based on the AC analysis. The performance of the gain, unity gain bandwidth (UGB) and phase margin are obtained by using AC analysis. In the meantime, the result of slew rate and settling time are presented by transient analysis. The simulated DC gain and a phase margin of a folded cascode op-amp are demonstrated in Figure-2 and Figure-3, respectively. The DC gain exhibits a high gain of 64.5 dB and a phase margin of 68.4° with the unity gain bandwidth (UGB) of 133.1 MHz.

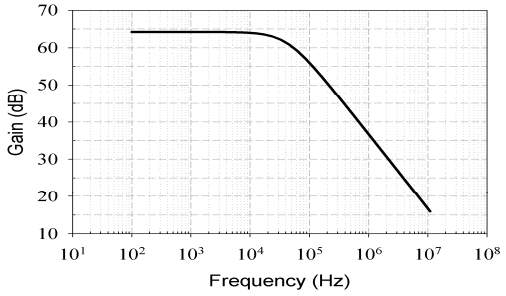

Figure-2. DC gain**.**

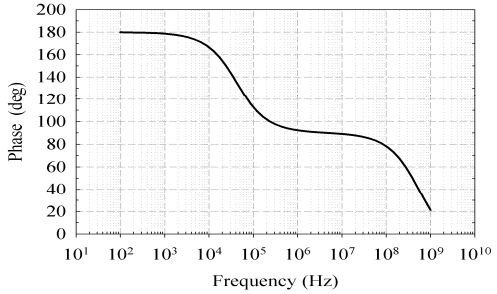

Figure-3. Phase margin.

As represented in Figure-4, the transient analysis is defined in order to obtain the rate of change of output with time which is slew rate and settling time. As can be seen, the proposed op-amp performs a high slew rate of 22.6V/µs with a settling time of 72.4ns.

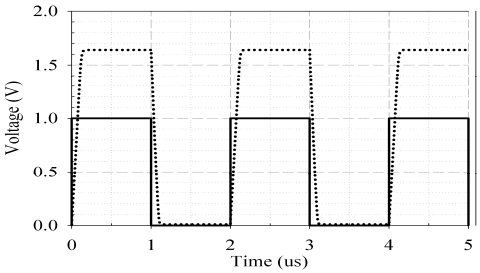

Figure-4. Transient analysis.

The comparison of the performances among the folded cascode op-amp design for pipeline ADC is summarized as in Table-2. In this work, the folded cascode op-amp with CMFB obtains low power as compared to the previous worked with the other performances is comparable. In addition, the proposed design used the smallest load capacitance, thus the chip size can be reduced.

Table-2. Comparison of folded cascode op-amp performances.

References	[11]	[12]	[13]	This work
Technology (µm)	0.35	0.18	0.13	0.13
Power Supply (V)	3.0	1.2	1.8	1.8
DC gain (dB)	95.0	110	91.5	64.5
UGB (MHz)	412.0	821	714.5	133.1
Phase Margin (º)	75.0	70	62.0	68.4
Slew rate (V/ µs)	N/A	35	N/A	22.6
Settling time (ns)	7.5	3.7	40.0	72.4
Power consumption (mW)	12.8	7.8	9.0	0.3
Capacitive load (pF)	1.9	1.0	7.5	1.0

RESULT AND DISCUSSION

The low power and high gain folded cascode CMOS operational amplifier with a common mode feedback for pipeline ADC is presented in this paper. The folded cascode topology with a modified circuit of CMFB obtains low power about 0.3mW. Moreover, the proposed design demonstrates a DC gain of 64.5dB with UGB of 133.1MHz. The simulated results confirm that the design of op amp can be intended in a low power pipeline ADC.

REFERENCES

[1] G.R Harris and T. Kocak, A novel asynchronous ADC Architecture, IEEE 11th International NASA Symposium on VLSI Design, 2003.

[2] S.I. Ahmed, Pipelined ADC Design and Enhancement Techniques, Analog Circuits and Signal Processing, Springer Science Business Media B.V., 2010.

[3] S. Kant and O.P. Sahu, Design of Low Voltage High Speed Opertaional Amplifier for Pipelined ADC in 90nm Standard CMOS Process, International Journal of Engineering Research & Technology (IJERT2012), Vol. 1. Issue 4, 2012.

[4] M. Fan, J. Ren, N. Li, F. Ye and J. Xu, A 1.8-V 11-bit 40-MS/s 21mW pipelined ADC, Springer:Analog Integrated Circuit Signal Process, Vol.63, pp:495-501, 2010.

[5] D. Nageshwarrao, S. Venkata C. and V. Malleswara R., Gain Boosted Telescopic OTA with 110dB Gain and 1.8GHz UGF, International Journal of Electronic Engineering Research, Vol. 2, No.2 pp.159-166, 2010.

[6] S.L.M Hassan, I.S.A Halim, A.A AbRahim, N.A Aziz and T.N.T Yaakub, Comparative Study on Multistage Amplifier and Folded Cascode Amplifier Design in Sample and Hold Circuit using 0.18um CMOS Technology, International Symposium on Computer Applications and Industrial Electronics (ISCAIE2012), Kota Kinabalu, 2012.

[7] Gu Wei and Gao Wei, Design of OTA with Common Drain and Folded Cascode Used in ADC, World Academy of Science, Engineering and Technology Vol. 67, 2012.

[8] Z. Kun, W. Di and L. Zhangfa, A High-performance Folded Cascode Amplifier, International Conference on Computer and Automation Engineering (ICCAE2011), pp:41-44, 2011.

[9] M. F.Ahmad, S.A.Z.Murad, M.M Shahimin, S.A.A Rais, and A.F. Hasan, Modified CMFB circuit with enhanced accuracy for data converter application, Applied Mechanics and Materials, vol. 446-447, pp.: 992-996, 2014.

[10] Weixun Yan and Zimmermann, H., Continuous-Time Common-Mode Feedback Circuit for Applications with Large Output Swing and High Output Impedance, 11th IEEE Workshop on Digital Object Identifier, 2008.

[11] R. Musa, Y. Yusoff, T.K yew and M.Rahmad, Design of Single Stage Folded-Cascode Gain Boost Amplifier for 100mW 10-bit 50MS/s Pipelined Analog-to-Digital Converter, ICSE Kuala Lumpur, 2006.

[12] B. Dhore, D.S. Ajnar and P.K. Jain, A low Power

High Gain Folded-Cascode CMOS Op-Amp with Slew Rate Enhancement Circuit for 100mW 10-bit 50MS/s High Speed ADC Designed in 0.18µm CMOS Technology, International Journal of Computer and Network Security (IJCNS), Vol.2, No.8 pp. 90-93, 2010.

[13] X. Liu and J.F McDonald, Design of Single-Stage Folded Cascode Gain Boost Amplifier for 14bit 12.5Ms/S Pipelined Analog-to-Digital Converter, IEEE-ICSE Kuala Lumpur, 2012.