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ELECTRICAL CHARACTERIZATION OF DIFFERENT HIGH-*K* DIELECTRICS WITH TUNGSTEN SILICIDE IN VERTICAL DOUBLE GATE NMOS STRUCTURE

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ABSTRACT

The limitation of Poly-Si/ SiO_2 devices in producing a greater value of drive current (I_{ON}) has become a major issue, especially for very small scale devices. It is believed that the problem may be resolved by introducing metal-gate/high-*k* dielectrics to replace traditional Poly-Si/SiO_2 technology. This paper presents the performance analysis of several different high-*k* dielectrics technology with tungsten silicide (WSi_x) as a metal-gate in ultrathin pillar vertical double-gate (DG) NMOS architecture. The device was virtually fabricated by using an ATHENA module of Silvaco TCAD tools. At the same time, the device characterization was carried out using an ATLAS module of Silvaco TCAD tools. The dielectric materials used for the simulation are known as Al_2O_3, HfO_2, TiO_2 and ZrO_2. Analysis of the results revealed that the WSi_x/TiO_2 device has superior electrical characteristics compared to others. The significant improvement was observed in terms of the drive current (I_{ON}) where the WSi_x/TiO_2 device produced 2.845.2 µA/µm at 0.205 V of threshold voltage (V_{TH}). This I_{ON} value exceeds the minimum requirement predicted by the International Technology Roadmap Semiconductor (ITRS) 2013 for high performance (HP) multi-gate (MG) technology.

Keywords: drive current, high-*k,* metal-gate, NMOS.

1. INTRODUCTION

The performance of metal-oxide-semiconductor field effect transistor (MOSFET) incorporating high-*k* dielectric significantly improves channel transport performance. It is difficult to apply traditional Poly-Si/SiO_2 technology to ultra-small gate length MOSFET especially to meet the requirements of high performance (HP) logic technology, which requires a very high drive current (I_{ON}) specification [1]. The small dimension of a Poly-Si/SiO_2-based MOSFET has difficulty producing a drive current (I_{ON}) exceeding 1,480 µA/µm as predicted by the International Technology Roadmap 2013 [1].

The smaller MOSFET device requires an increased capacitance gate dielectric to control the short channel effects such as hot carrier degradation [2, 3]. This can be achieved by modifying several device designs and reducing the gate oxide thickness (EOT). However, the reduction of EOT leads to the increased gate leakage which eventually decreases the drive current (I_{ON}) [4]. For a thickness below 2 nm, the leakage is unacceptably high when SiO_2 is used as the gate dielectric material [5]. Therefore, the high-*k* dielectrics have been widely used as a gate dielectric material to replace the SiO_2 in current MOSFET's technologies due to their high dielectric constants [6, 7]. The dielectric layers with higher electrical permittivity are used in thicker films to reduce the leakage current and improve upon the reliability of the gate dielectric layer with electrical thickness equal to an ultra-thin SiO_2 layer [8].

In this regard, Titanium dioxide (TiO_2) has been extensively studied because of its remarkable optical and electrical properties. Studies on thin films of TiO_2 have reported dielectric constants ranging from 40 to 86 [9]. The TiO_2 dielectric has the highest dielectric permitivitty compared to SiO_2, Al_2O_3, HfO_2 and ZrO_2. Several reports on the TiO_2 effects towards the device characteristics of a single metal-gate MOSFET have been done by Afifah Maheran *et al.* The type of metal-gate used in their work is Tungsten Silicide (WSi_x). The compatibility of a single WSi_x gate with the TiO_2 dielectric was reported to result in a nominal V_{TH} value (0.306 V) and a low leakage current (0.258 nA/µm) that satisfy the requirements of ITRS 2011 for a bulk single-gate device [10, 11]. Another report has proven that the combination of a single WSi_x gate with TiO_2 dielectrics have allowed the reduction of the gate length (Lg) from 32 nm to 22 nm while keeping the nominal V_{TH} value [13]. The application of WSi_x as a metal-gate is due to its compatibility with both NMOS and PMOS devices via metal-gate workfunction engineering proposed by Hong *et al.* patent [14].

Furthemore, Rahul *et al*. reported that the integration of Hafnium dioxide (HfO_2) with the Nickel (Ni) as the metal-gate in Junctionless Vertical Double-gate MOSFET yielded a very high drive current (I_{ON}) value of 1772 µA/µm [14]. Their approach was based on varying the work function of the metal-gate in order to set the appropriate threshold voltage (V_{TH}) of the device [14]. Therefore, a significant attempt to find the correct work function of the metal-gate is very crucial in order to stabilize the threshold voltage (V_{TH}) [8]. The compatibility of different high-*k* dielectric materials with a metal-gate may differ due to their different dielectric constants [14].

In this paper, the electrical characteristics for the WSix integrated with Al_2O_3 (k~9), HfO_2 (k~25), TiO_2 (k~85), ZrO_2 (k~22)and Poly-Si/SiO_2 (k~3.9) are compared and analyzed utilizing Silvaco TCAD, ATHENA and ATLAS modules. The electrical performances of all the high-*k* materials with WSix gate in the vertical double-gate NMOS structure are investigated and presented in the following section.

2. PROCESS SIMULATIONS

The key feature of the device fabrication method is depicted in Figure-1. A P-type silicon with <100> orientation was used as the main substrate for the device's design. The silicon substrate was doped with boron by a concentration of 1 x 10^{14} atom/cm^3. The doping with donors and acceptors was implemented in order to modify the electron and hole concentration in the silicon substrate within a very large range of 10^{13} up to 10^{21} [15]. The virtual process was followed by the gate oxidation process in which the silicon substrate was oxidized in dry oxygen for a short period of time.

Figure-1. Vertical double gate NMOS with WSix/TiO_2Stack Technology process flowchart.

The next process was to etch the gate oxide in order to replace it with a thin layer of dielectric material. For instance, the titanium dioxide (TiO_2) was selected as a dielectric material. The thickness of the TiO_2 dielectric was approximately 3 nm. Therefore the equivalent oxide thickness (EOT) of the dielectric can be computed by using (1) [14]:

$$EOT = \left[\frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}}\right] T_{high-K} \quad (1)$$

Where$\varepsilon_{SiO2}$is the permittivity of SiO_2 which is 3.9, $\varepsilon_{high\text{-}k}$ is the permittivity of high-*k* which is TiO_2 (85) and is the high-*k* dielectric physical thickness. Since the $T_{high\text{-}k}$is approximately 3 nm, the EOT of the dielectric will be 0.138 nm. The gate oxide material with a dielectric constant (k) higher than SiO_2 will result in a smaller EOT even with a physical thickness ($T_{high\text{-}k}$) larger than the SiO_2 (T_{ox}).

The tungsten silicide (WSi_x) was then deposited at the top of TiO_2 layer. Both TiO_2 and WSi_x layers were etched to form the vertical gate. The work function of 4.5 eV was set for the WSi_x gate [16]. After that, halo implantation was implemented in order to mitigate the short channel effects in MOSFET devices [17–19]. The sidewall spacers were then deposited in order to separate the two high dopant areas. It also acts as a diffusion buffer for the dopant atom in the source/drain that will cause the interception between the source / drain and gate when the distance is too close.

Since the device was a n-type, the source/drain implantation was done by implanting arsenic dosage as a n-type dopant.The compensation implantation was utilized later by implanting phosphor dosage. This process was performed to reduce parasitic capacitance that might slow down the device, thus deteriorating the device's performance. The top of the structure was then placed in contact with aluminum metal. The aluminum layer was deposited on the top structure's surface and any unwanted aluminum was etched to develop the contacts [20, 21].

Next, metallization and etching were performed to form electrodes at the drain and source regions. The completed structure of the vertical double gate NMOS device with metal-gate/high-*k* stack technology was completed by mirroring the right-hand side structure. The completed structure of the Vertical Double Gate NMOS device with WSi_x/TiO_2 stack technology is illustrated as in Figure-2. The process parameters that were used in the process simulation is summarized in Table-1.

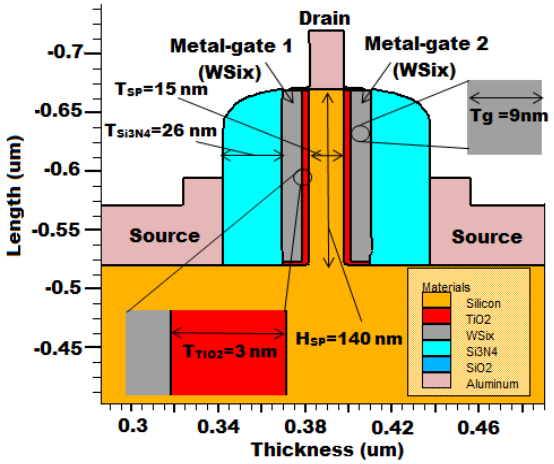

Figure-2. Final structure of vertical double gate NMOS device with WSi_x/TiO_2 Stack Technology.

Table-1. Process parameters of vertical double gate NMOS device.

Process parameters	Units	$WSix/Al_2O_3$	$WSix/HfO_2$	$WSix/TiO_2$	WSi/ZrO_2
Substrate Implant Dose	atom cm^{-3} ($x10^{-14}$)	1	1	1	1
V_{TH} Implant Dose	atom cm^{-3} ($x10^{-12}$)	1.81	1.81	1.81	1.81
V_{TH} Implant Energy	kev	20	20	20	20
V_{TH} Implant Tilt	degree	10	10	10	10
Halo Implant Dose	atom cm^{-3} ($x10^{-12}$)	3.86	5.47	2.82	5.23
Halo Implant Energy	kev	170	170	170	170
Halo Implant Tilt	degree	28	28	28	28
S/D Implant Dose	atom cm^{-3} ($x10^{-18}$)	1.25	1.25	1.25	1.25
S/D Implant Energy	kev	20	20	20	20
S/D Implant Tilt	degree	80	80	80	80
Compensation Implant Dose	atom cm^{-3} (10^{-12})	2.51	2.51	2.51	2.51
Compensation Implant Energy	kev	60	62	60	60
Compensation Implant Tilt	degree	7	7	7	7

3. DEVICE CHARACTERIZATION

Once the devices were built with ATHENA module, the completed devices were characterized by utilizing ATLAS module to provide specific characteristics such as the I_D versus V_{GS} curve. Device characteristics such as threshold voltage (V_{TH}), drive current (I_{ON}), off-leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold swing (SS) and drain induced barrier lowering (DIBL) were retrieved from the simulation. The simulation results for the WSi_x-based gate with different high-*k* dielectric materials and poly-Si/SiO_2 channel devices were then compared and investigated. The device simulation setup condition is listed in Table-2 [22].

Table-2. Device simulation conditions [22].

Device characteristics	Drain voltage, V_D (V)	Gate voltage, V_G (V)		
		$V_{Initial}$	V_{Step}	V_{Final}
Threshold Voltage (V_{TH})	1.0	0	0.1	2.0
Drive Current (I_{ON})	1.0	0	0.1	2.0
Leakage Current (I_{OFF})	1.0	0	0.1	2.0
Subthreshold Swing (SS)	1.0	0	0.1	2.0
Drain Induced Barrier Lowering (DIBL)	0.1	0	0.1	1.5
	3.0	0	0.1	1.5

It is important to ensure that all the devices are set to the same level of V_{TH} during the simulation. This was 0.205 V as predicted by ITRS 2013 for high performance (HP) multi-gate technology in the year 2020. This was done to precisely evaluate device performance in terms of the corresponding I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS and DIBL.

4. RESULTS AND DISCUSSIONS

The device characteristics of both WSi_x/TiO_2 and Poly-Si/SiO_2 Vertical Double-gate NMOS devices were extracted by utilizing ATLAS module. Figure-3 depicts the contour mode of vertical double gate NMOS device that shows the device's doping profile. The channel length (Lc) between the source and the drain region was measured to be 90 nm approximately.

Figure-4 shows the graph of drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 1.0 V for Vertical Double-gate NMOS device with different high-*k* dielectric materials such as Al_2O_3 (k~9), HfO2 (k~25), TiO_2 (k~85), ZrO_2 (k~22) and Poly-Si/SiO_2 (k~3.9). The threshold voltage (V_{TH}) value for the device was fixed at 0.205 V.

Figure-5 depicts the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 1.0 V for vertical double gate NMOS device. The value of leakage current (I_{OFF}), drive current (I_{ON}) and subthreshold swing (SS) was extracted from the graph. The I_{ON} is the maximum drain current (I_{Dmax}) when $V_{GS}=V_{DD}$ and

V_{DS}=V_{DD}[23]. Meanwhile, the off-leakage current (I_{OFF}) defined as a drain to source current and was measured when V_{GS}=0 and V_{DS}= V_{DD} [24]. In other words, the off-state current (I_{OFF}) is the drain current when no gate voltage is applied.

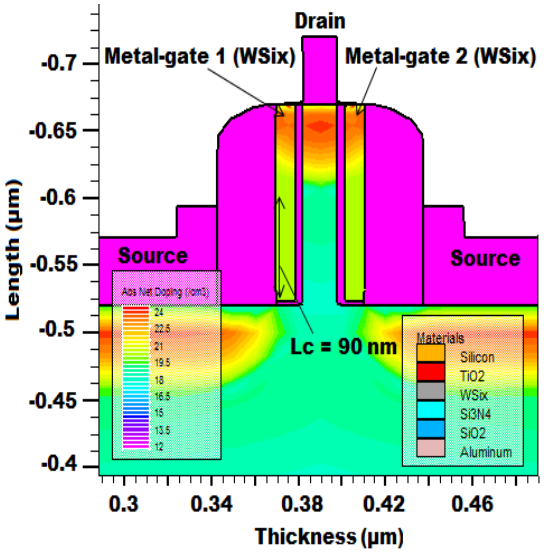

Figure-3. Contour mode of vertical double gate NMOS device with WSi_x/TiO_2 Stack Technology.

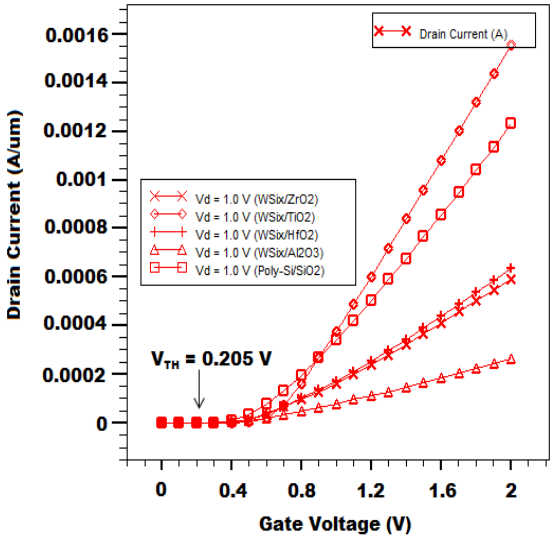

Figure-4. Graph of drain current (I_D) versus gate voltage (V_G).

The model equations for both the I_{ON}/I_{Dsat} and I_{OFF} are stated in (2) and (3) [25,26]:

$$I_{Dsat} = \frac{W}{L}\mu C_{inv}\frac{(V_{GS}-V_{TH})^2}{2} \quad (2)$$

where W is the effective channel width, L is the effective channel length, μ is the carrier mobility in the channel (assumed constant here), C_{inv} is the gate capacitance density with channel in inversion, V_{GS} is the gate to source voltages, and V_{DS} is the drain to source voltages, and V_{TH} is the threshold voltage.

$$I_{OFF}(V_{GS},V_{DS}) = I_O e^{(V_{GS}-V_{TH})/nV_T}(1-e^{-V_{DS}/V_T}) \quad (3)$$

where $I_o = \mu_o C_{ox}\frac{W}{L}V_T^2$, $V_T = kT/q$ = 26mV is the thermal voltage, C_{ox} is the oxide capacitance, μo is the zero bias mobility, W/L is the width over length ratio of the device, and n is the subthreshold swing coefficient.

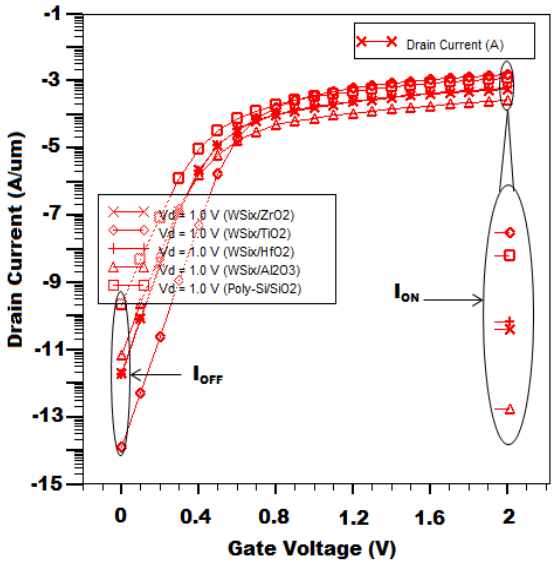

Figure-5. Graph of subthreshold drain current (I_D)-gate voltage (V_G).

The subthreshold swing (SS) value was obtained from the inverse slope of $\log_{10} I_D$ vs. V_{GS} characteristic. It shows how much change in the gate voltage is required to change the drain current by one decade as shown in (4) [27]:

$$SS = \left[\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right]^{-1} \quad (4)$$

Table-3 shows the results of the device characteristics for the Poly-Si/SiO_2 based device and the WSi_x with Al_2O_3, HfO_2, TiO_2 and ZrO_2 based device. Based on Table-3, it is observed that the WSi_x/TiO_2 device has produced the highest value of drive current (I_{ON}) which is 2845.2 µA/µm. In fact, all the device characteristics of the WSi_x/TiO_2 based device were observed to be better than the others.

Table-3. Results of device characteristics for different technologies of vertical double gate NMOS devices.

Device characteristics	PolySi/SiO_2	WSix/Al_3O_2	WSix/HfO_2	WSix/TiO_2	WSix/ZrO_2
I_{ON}(μA/μm)	1231.9	1717.3	2169.8	2845.2	2071.8
I_{OFF} (pA/μm)	225.4	0.480	0.002	0.088	0.002
I_{ON}/I_{OFF} ratio (x10^9)	0.006	3.575	1108	0.323	1020
SS (mV/dec)	75.38	63.64	59.92	59.82	60.80
DIBL (mV/V)	23.64	28.16	19.41	1.817	20.84

Figure-6 depicts the effect of different high-*k* dielectric materials upon the I_{ON} value of vertical double-gate NMOS device. It can be observed that the I_{ON} is proportional to the permittivity of high-*k* dielectric materials. There is a significant improvement of the I_{ON} value when TiO_2 is used as a gate dielectric. This is due to a decrease in depletion as there is less boron penetration when a higher permittivity of high-*k* dielectric is applied [28]. The I_{ON} is one of the important characteristic that determines the drive capability of the device [23].

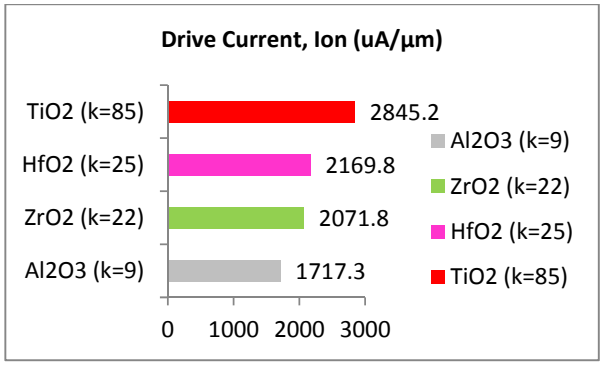

Figure-6. I_{ON} Values for different High-*k* dielectrics.

Figure-7 shows the effect of different high-*k* dielectric materials towards the I_{OFF} value of the vertical double-gate NMOS device. Ideally, the I_{OFF} value will be zero when no voltage is applied to the gate and the V_{DS} is set equal to V_{DD} (voltage supply) [23]. A higher dielectric constant material is introduced to replace SiO_2 which allows a thicker dielectric to be deposited to reduce leakage without electrical thickness penalties [29, 30]. As a result, the thicker high-*k* dielectric gate will increase the overall capacitance, hence, decreasing the leakage current (I_{OFF}). It is important to ensure that the I_{OFF} is kept as minimal as possible in order to reduce the power consumption of the device [23]. It can be observed that the I_{OFF} value value was at the lowest level when the HfO_2 (hafnium dioxide) dielectric is applied as the insulator of the WSi_x (tungsten silicide) gate.

The I_{ON}/I_{OFF} ratio is the important characteristic that indicates the ratio of total I_{ON} to the I_{OFF}. The I_{ON}/I_{OFF} ratio represents the power consumption of a device. The higher the I_{ON}/I_{OFF} ratio, the better will be the power consumption of the device. From Figure-8, the highest I_{ON}/I_{OFF} ratio recorded is produced by WSi_x/HfO_2 device, which indicates that the combination of WSi_x-gate with the HfO_2 dielectric demonstrates a better power consumption than the other devices.

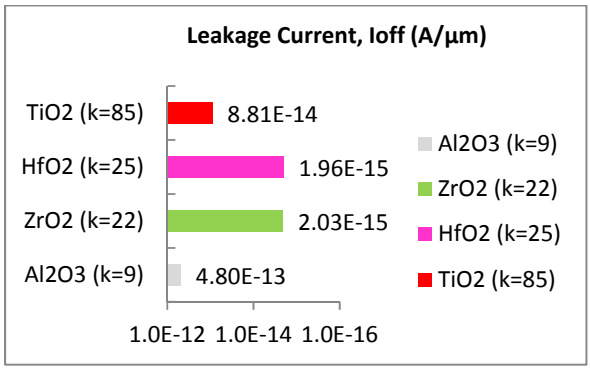

Figure-7. I_{ON} Values for different High-*k* dielectrics.

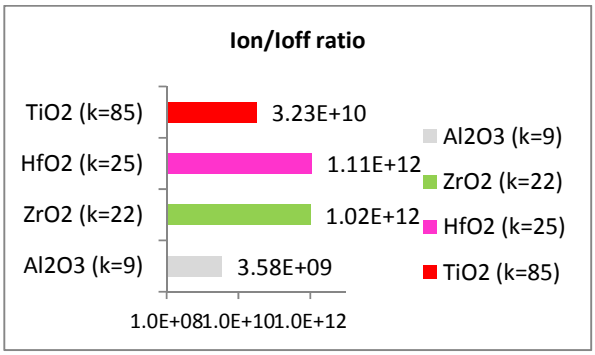

Figure-8. I_{ON}/I_{OFF} ratio for different High-*k* dielectrics.

The subthreshold swing (SS) is an important characteristic in MOSFET's device that indicates the speed of the switching transition from "ON" to "OFF" state, or vice versa [27]. The lower SS value, the faster will be the switching operation. It also indicates how effectively the flow of drain current can be halted when V_{GS} is decreased below V_{TH}. In this regard, Figure-9 exhibits the decrease of the SS value when a higher dielectric constant of high-*k* material is applied as the WSi_x gate insulator.

The drain induced barrier lowering (DIBL) is a type of short channel effect in MOSFETs. It refers to a reduction of V_{TH} at higher drain voltage (V_D). The DIBL effect occurs in short channel devices when the depletion region of the drain and the source interact with each other.

This interaction turns on the device prematurely [31]. In other words, DIBL is defined as the ratio of change in threshold voltage, ΔV_{TH} to the change in drain voltage ΔV_D. To measure the DIBL value, two values of threshold voltage, V_{TH1} and V_{TH2} must be extracted at V_{D1}=0.1 V and V_{D2}=3.0 V. The value of DIBL is computed by using (5) [32]:

$$DIBL = \frac{V_{TH1} - V_{TH2}}{V_{D2} - V_{D1}} \quad (5)$$

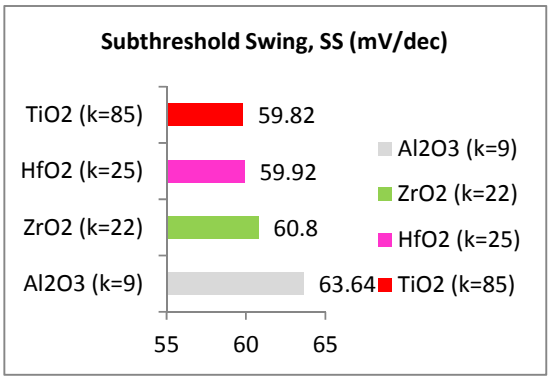

Figure-9. SS values for different High-*k* dielectrics.

Figure-10 shows the effects of different high-*k* dielectric towards the DIBL value in vertical double-gate NMOS device. It can be observed that the DIBL value of vertical double WSi_x-based gate NMOS device can be suppressed by using a higher dielectric constant of high-*k* materials. Based on all the experimental results, it can be concluded that the vertical double WSi_x-based gate NMOS device is more compatible with the TiO_2 due to its superior device characteristics, especially the I_{ON} value that meets the requirement of high performance (HP) multi-gate (MG) technology predicted by International Technology roadmap Semiconductor (ITRS) 2013 (ITRS 2013).

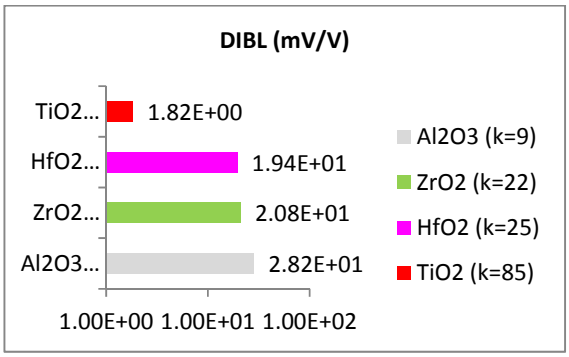

Figure-10. DIBL values for different High-*k* dielectrics.

Table-4 shows the comparison of observed device characteristics for the WSi_x/TiO_2 vertical double gate NMOS device with other researchers. There are a few improvements on the overall device characteristrics of the simulated device compared to the results obtained from previous works. The I_{ON} value of the WSi_x/TiO_2 vertical double gate NMOS device is slightly lower than the result obtained by Rahul *et al.* [13]. This might be due to the different types of material, channel length (Lc) and workfunction of the metal-gate [8,13].

However, the I_{ON} value of this recent work still exceeds 1,480 µA/µm predicted by ITRS 2013 [1]. The DIBL value of the device is the lowest among others due to its long channel length (Lc) and the presence of nitride barrier (Si_3N_4) that can reduce the possibility of charge sharing effect between the source and the drain region. The channel length (Lc) can be controlled by varying the height of the silicon pillar [21,33]. Alternatively, the channel length (Lc) can also be controlled by varying the source and the drain implant tilt angle [34]. The vertical double gate MOSFET structure developed by Kim *et al.* produced a very low SS value compared to the others due to the hetero-junction and the selective epitaxial growth (SEG) technique [35].

Table-4. Benchmark of vertical double gate NMOS devices through simulation.

Author	Device technology	Channel length (nm)	I_{ON} (µA/µm)	I_{OFF} (pA/µm)	I_{ON}/I_{OFF} ratio (x10^9)	SS (mV/dec)	DIBL (mV/V)
Saad et al. (2008) [34]	Poly-Si/SiO_2	90	200	0.00001	20,000	100	94
Saad et al. (2010) [36]	Poly-Si/SiO_2	50	588	0.0552	10.65	81.9	62
Rahul et al. (2014) [13]	Poly-Si/SiO_2	N/A	720	113.4	0.006349	63.74	44.29
Rahul et al. (2014) [13]	Nickel/HfO_2	N/A	1772	1422	0.001246	61.01	40.4
Kim et al. (2015) [35]	TiN/SiO_2	N/A	100	N/A	N/A	32	N/A
From this work	Poly-Si/SiO_2	90	1231.9	225.4	0.006	75.38	23.64
From this work	WSix/TiO_2	90	2845.2	0.088	0.323	59.82	18.17

5. CONCLUSIONS

In conclusion, the WSi_x/TiO_2 stack technology has been virtually integrated with the vertical double-gate NMOS device. Based on the simulation results using SILVACO TCAD tools, the TiO_2 has been recognized as the most suitable high-*k* dielectric material for vertical WSi_x-based double-gate NMOS device due to its excellent device characteristics that meets the requirement of high performance (HP) multi-gate (MG) technology predicted by ITRS 2013. In the present investigation, the major difference between WSi_x/TiO_2 device with the others was in terms of the drive current (I_{ON}) value. The drive current (I_{ON}) of WSi_x/TiO_2 device exceeded the minimum value which is 1,480 μA/μm as specified in ITRS 2013. The presence of both WSi_x and TiO_2 dielectric enormously increased the channel capacity of the device. The rapid mobility of ion movement in the channel tremendously increased the drive current (I_{ON}). Moreover, the WSi_x/TiO_2 device demonstrated excellent power consumption due to its higher I_{ON}/I_{OFF} ratio.

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