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LOW POWER AND HIGH SPEED CARRY SAVE ADDER USING MODIFIED GATE DIFFUSION INPUT TECHNIQUE

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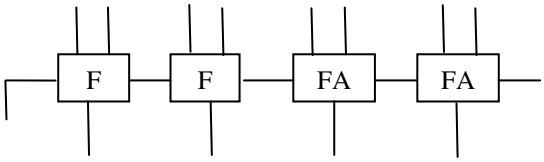
ABSTRACT

Low power and high speed adders are the most essential components of every contemporary signal processing applications. Among the many adders, Carry Save Adder (CSA) is the high speed multi operand adder used in many applications. This paper presents the design of low power and high speed Carry Save Adder with reduced no. of transistors using Modified Gate Diffusion Input (MGDI) technique. This technique has been adopted from Gate Diffusion Input Technique (GDI) and is used achieve reduced power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. This paper aims at designing of 4 operand 8 bit and 16 bit CSA using conventional CMOS, GDI and MGDI techniques. After various performance comparisons, it is stated that total power dissipation, propagation delay and transistor count are much smaller in MGDI technique than compared to CMOS and GDI technique.

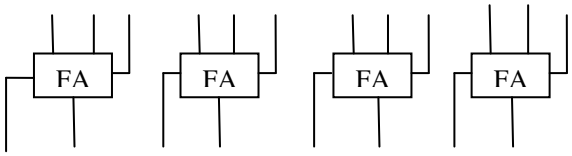
Keywords: carry save adder, GDI, MGDI, low power dissipation.

INTRODUCTION

In the digital systems, adders having a key role in computational circuits and other complex arithmetic circuits which will be used many signal processing applications. The arithmetic function attracts a lot of researcher's where they can use them in many applications. Among the complex adders, the most widely used primary adder is the Ripple Carry Adder (RCA) [1]. In the designing of RCA it uses row of cascaded one bit Full Adders (FA) to compute the addition of two operands. With slight modification to this design, this row of FAs can also be arranged as a mechanism to reduce three binary numbers into two binary numbers in multi-operand (three or more operands) addition. This method is used in carry save adder (CSA) where it is indeed an RCA with its carries saved rather than propagated. Therefore, CSA operator is often called (3:2) counter. The block diagrams for RCA and CSA are shown in Figure-1 for comparison [2], [3]. Unlike RCA, Carry Lookahead Adder (CLA) and Carry Select Adders (CSA), the CSA realizes concurrent addition of multiple operands, multiplication. Instead of using the 2-operand adders that necessitate the time consuming carry propagation to repeat several times, depending on the number of operands, the CSA's timing could be improved with a little increase or even a reduction in area [4].



(a)



(b)

Figure-1. Sample block diagram of a) The RCA; b) The CSA.

This paper initially describes the design procedure and operation of CSA along with small introduction to MGDI technique. Latter it gives the design of 8 bit and 16 bit CSAs by using MGDI technique. Finally, the results are compared with of power, propagation delay and transistor count with respect to CMOS and GDI technique.

CARRY SAVE ADDER (CSA)

A CSA tree consists of CSA operators and one adder at the root of the tree. The CSA operation are used to transform an arbitrary number of operands in the addition process two adding operands, of operands in the addition process to produce two adding operands, after which the adders at the root of the CSA tree computes the final sum[5]. Figure-2(a) and 2(b) shows the addition of three 1-bit binary numbers, A, B and C, implemented without the CSA operator and with the CSA operator, respectively.

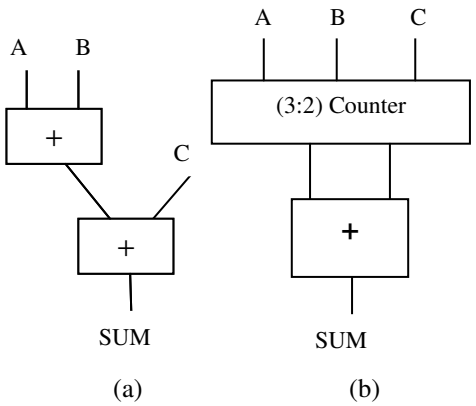


Figure-2. The addition process a) Without CSA operation b) With CSA operation.

The 1-bit multi-operand addition mentioned earlier can be extended to an n-bit multi-operand addition by cascading the CSA operators. An n-bit CSA consists of n disjoint FAs operating in parallel. Each FA has three i^{th} bit input and generates two outputs, namely an i^{th} bit partial sum, S, and an i^{th} bit carry, C. As for adding more than three operands, there is a second or further subsequent levels of the CSA operators. They receive the S and C from the previous CSA operator level, together with another input operand, and produce a set of new S and C values. The levels with CSA operators contain no carry propagation. The carries propagate only in the last step. Consequently, as compared to the RCA's propagation delay of n FAs, the CSA has the same propagation delay as only one FA, and it remain constant for any value of n.

Figure-3 shows a CSA for the addition of four 4-bit binary numbers A, B, C and D, with an initial carry-in,C_0. The upper two levels of the FA or (3:2) counters from the 4-bit CSA, while the third level is the 4-bit carry propagating Adder (CPA). The CPA used in this case is an RCA, but a CLA or any other fast adder can substitute for it. Each CSA operator takes three bits of the same significance and then computes the sum of the same significance and the carry for the bit of higher significance.

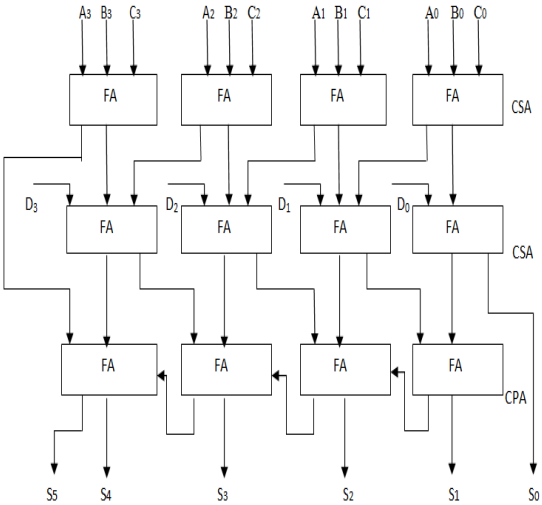


Figure-3. A 4-Operand 4 bit CSA.

The implementation of the CSA can be further expanded to add k operands. Here, (k-2) CSA levels and one CPA are required to realize the addition operation. The time to obtain the summation is

$$T = (k-2).\ \boldsymbol{T}CSA + \boldsymbol{T}CPA \quad (1)$$

Equation (1) gives the time required for implementing k bit CSA. Where ***T***CSA and ***T***CPA are the execution times for a CSA level and CPA, respectively.

MODIFIED GATE DIFFUSION INPUT

Modified Gate Diffusion Input (MOD-GDI) is a new technique of low power digital circuit design. This technique is adopted from the GDI technique [6]. The MOD-GDI technique is mainly used to reduce the power dissipation, propagation delay and transistor count of the digital circuits.

Though all these parameters are achieved using the GDI technique, the MOD-GDI technique is proposed to overcome some of the major limitations of the GDI technique like difficulty in fabrication process and additional circuitry to give inputs to the GDI based circuits. By using this technique the combinational logic gates like OR, AND, Inverter and 2X1 MUX are designed using two transistors, whereas four transistor are used for OR & AND logics and for 2 X 1 MUX the transistor count is 14 using CMOS design. Hence the MOD-GDI technique is a useful technique to reduce the area and also for less power dissipation [7].

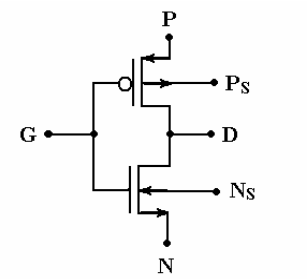


Figure-4. Basic MOD-GDI cell.

The Generalized equation for the output of the basic MOD-GDI logic cell when the inputs given to it is given in Eq2. as follows:

$$D = PG' + NG \quad (2)$$

Table-1, shows the input configuration of the different functions which are obtained by the basic MOD-GDI cell. The inverter input configuration is same for both the CMOS and MOD-GDI technique, so there will be no difference in the power dissipation. The remaining functions vary in configuration. The input configuration of the EX-OR and EX-NOR as given in the table are the basic configuration

Table-1. Functionality table of MGDI technique.

N	S_N	P	S_P	G	Output	Function
0	0	1	1	A	A1	Inverter
A	0	0	1	B	AB	AND
A	0	B	1	A	A+B	OR
B^1	0	1	1	A	A1 B1	NAND
0	0	1	1	A+ B	$(A+B)^1$	NOR
A^1	0	A	1	B	A^1 B+AB^1	EX-OR
A	0	A	1	B	AB+A^1 B^1	EX-NOR
B	0	A	1	S	AS^1+BS	2X1 MUX

. In order to get more output swing the configurations were modified to achieve better computation. Table 2, 3, 4 gives the comparison of power dissipation, Transistor count and Propagation delay of various logic gates. Here all the logic gates are designed for 2 input only expect inverter.

Table-2. Power dissipation of different primitive gates.

Primitive gates	Total power dissipation		
	CMOS in nw	GDI in nw	MGDI in nw
INVERTER	30.23	9.20	9.20
AND	9.29	11.07	$6.48x10^{-5}$
OR	59.19	11.07	$647 x10^{-5}$
NAND	7.97	9.21	9.21
NOR	60.37	12.67	9.3
XOR	183.19	9.34	9.34
XNOR	183.89	20.28	5.83

Table-3. Transistor count of different primitive gates.

Primitive gates	Transistor count		
	CMOS	GDI	MGDI
INVERTER	2	2	2
AND	6	2	2
OR	6	2	2
NAND	4	4	4
NOR	4	4	4
XOR	12	6	4
XNOR	14	6	6

Table-4. Propagation delay of different primitive gates.

Primitive Gates	Propagation delay		
	CMOS In ns	GDI In ns	MGDI In ns
INVERTER	20.7	20.8	19.25
AND	30.5	42.7	19.95
OR	29.69	48.7	18.08
NAND	20.57	76.13	16.49
NOR	40.97	19.0	19.0
XOR	102.5	78.3	29.15
XNOR	20.4	28.1	14.9

From the above Tables it can be concluded that there is much reduction in all the three parameters in MGDI technique than comparative to CMOS and GDI. Therefore, this technique is further extended to high complex logic circuits where the power dissipation and delay are essential along with less area.

PREREQUISITES FOR DESIGNING CSA USING MGDI

As mentioned earlier, A CSA tree consists of CSA operators and one adder at the root of the tree. The generalized block diagram for n bit addition using CSA is depicted in Figure-4. Here it is clear that in the last stage, the carry propagate adder used is simple Ripple Carry Adder.

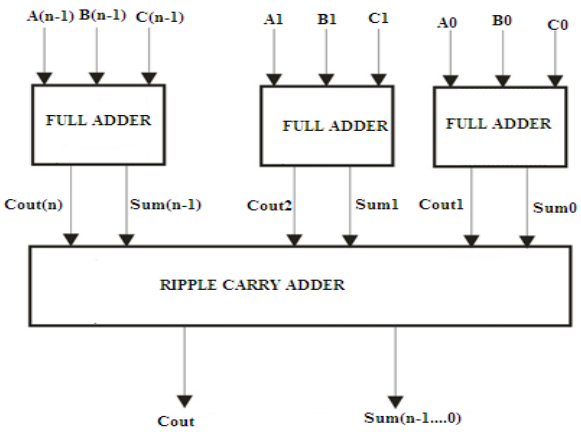


Figure-5. Block diagram of n-bit carry save adder.

From the Figure-4, an 8 bit and 16 bit CSAs would be designed. From Equation1, it is calculated that for 8 bit CSA, 6 one bit adders and a ripple carry adder is required. Similarly for 16 bit CSA, 14 one bit adders and correspondingly one more ripple carry adder is required. So initially it is required to design a one bit full adder and ripple carry adder. Therefore, this paper presents low power dissipated and high speed one bit adders using MGDI technique and the performance have been

compared with CMOS and GDI techniques. Latter, 8 bit and 16 bit RCAs are also designed by using MGDI technique. Then by using these sub modules the required 8 bit and 16 bit CSAs are designed.

One bit Full Adder

Though many researchers have already designed CMOS one bit full adders, this paper also compares with CMOS full adder with 28 No. of transistors and with GDI full adders.

The 1-bit Full adder is also designed using the MOD-GDI technique. The Logic equations for the 1- bit Full adder are shown in Equation (3) and Equation (4).

$$SUM = A \oplus B \oplus C_{in} \quad (3)$$

$$CARRY = A (A \odot B) + C_{in} (A \oplus B)$$
$$= A (A \oplus B)^{1} + C_{in} (A \oplus B) \quad (4)$$

The SUM for the proposed 1 -bit full adder can be implemented by cascading the two EX-OR gates and the CARRY can be implemented by the Equation (4) as it in the form of $S^{1}A+ SB$ which is the logic function for the 2 X 1 MUX. As the 2 X 1 MUX shown in the Figure-5 can be implemented using MOD-GDI with minimal transistor count of 2 transistors, the proposed full adder circuit gets optimised. The proposed full adder is as shown in the Figure-6.

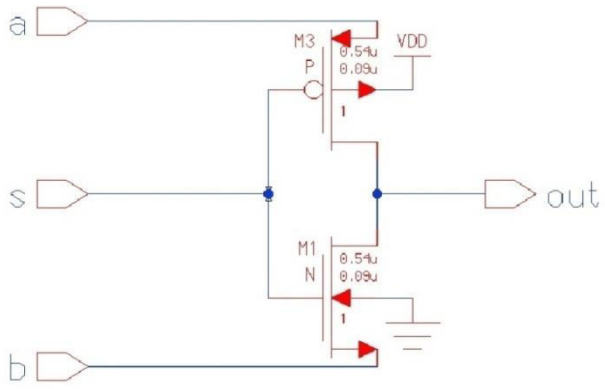


Figure-6. 2 x 1 MUX using Mod-GDI technique.

Here all the adders are designed with 90nm technology and W and L values are 0.54µm and 0.18µm respectively. Shows the design using MGDI, 12 transistors are required. In Figure-6, transistor M2 is used as a feedback transistor to improve the full swing. Comparison of various parameters are shown in Table 5.Because of using optimized design by Eq.3 and Eq.4, MGDI has reduced no. of transistors, less power dissipation and low propagation delay than CMOS and GDI techniques.

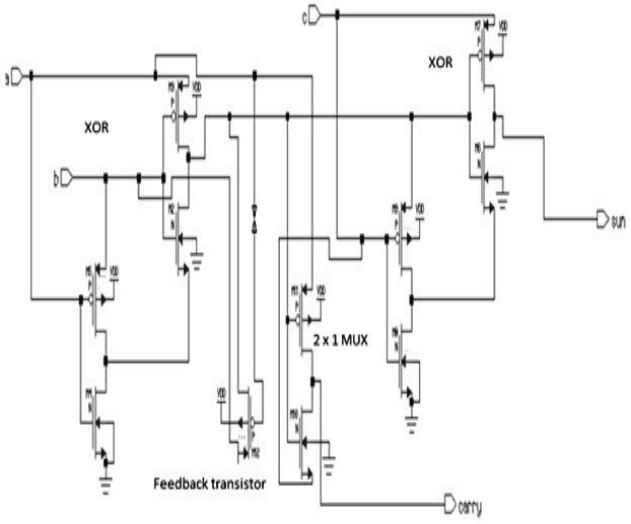


Figure-7. One bit Full Adder design using MGDI technique.

Table-5. Comparison of various parameters for one bit full adder in different technique.

Design technique	Total Power dissipation In nw	Transistor Count	Propagation delay In ns
CMOS	99.21	28	47.03
GDI	2.32	12	19.58
MGDI	0.0388	11	33

From the above table it is concluded that MGDI technique gives the solution for total power dissipation and propagation delay but with small amount increase in area. Due to large amount of reduction in power dissipation this MGDI technique can be used in many complex designs.

8- bit and 16- bit ripple carry adder

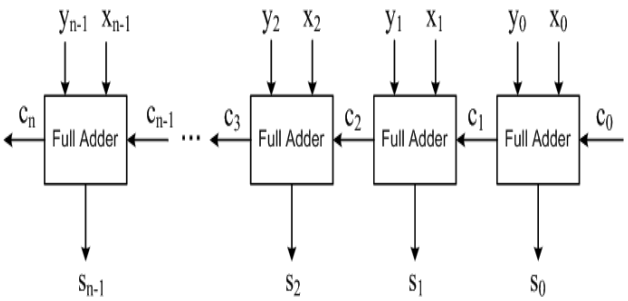


Figure-8. Block diagram of the n bit Ripple Carry adder.

Figure-7 shows the basic structure of n bit ripple carry adder. By using this block diagram, it is possible to design a 8 bit and 16 bit adders. Here the one bit full adder used is MGDI based one bit full adder. The design and comparative table are shown in the previous section. For 8 bit RCA, 8 such one bit adders used and for 16 bit RCA,

16 no. of such adders are used. Table-6. Gives the comparison table for power, propagation delay and no. of transistors used in various techniques. It is observed that MGDI based design obviously satisfies all three parameters.

Table-6. Comparision of various paramters for RCA in different technique.

Type of Adder	Parameter	CMOS	GDI	MGDI
8 Bit RCA	Total power dissipation in pw	$668x10^6$	402.7	310.9
	Propagation Delay in ns	568	235	49.9
	Transistor Count	224	96	88
16 Bit RCA	Total power dissipation in pw	$133x10^7$	632.9	481.67
	Propagation Delay in ns	663	452.9	79.54
	Transistor Count	448	220	176

PROPOSED CARRY SAVE ADDER

4 operand- 8 bit CSA

Figure-8. Shows the architecture of 4 operand 8 bit CSA, where it is consists of 24 one bit full adders. Top two levels are related carry save and the bottom one belongs to carry propagation. The design these internal blocks has been discussed in previous section. While designing this adder, there are many issues like low output swing, glitches in output have occurred. These issues have been carefully considered by choosing proper W and L ratios and input voltage. Initially W has taken as 0.54µm and it has been varied to 0.72 µm and input pulse voltage is also changed 0.9 V to 1 V.

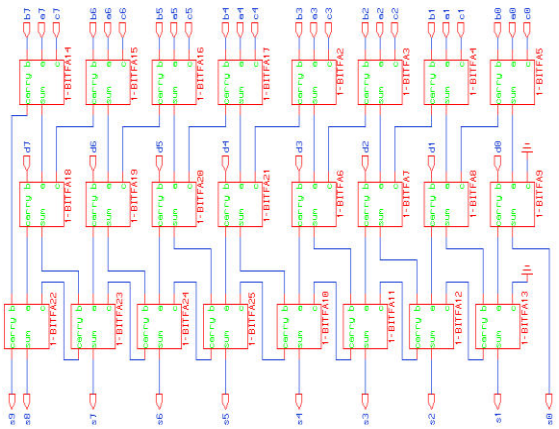


Figure-9. Schematic of 4 operand 8 bit Carry Save Adder

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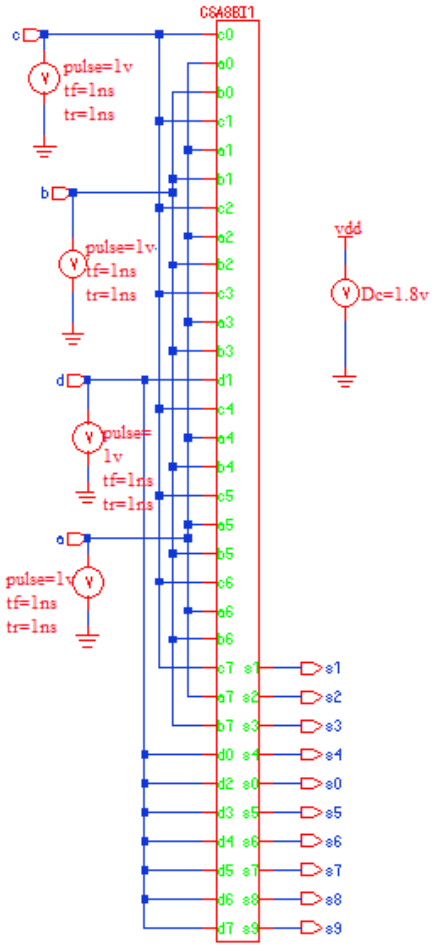

Figure-10. Testbench for 4 operand 8 bit Carry Save Adder.

Figure-9 Depicts the test bench symbol for the given 4 operand and 8 bit CSA is obtained from the architecture shown in Fig 8. Functionality of these adders has been verified for all the combinations, some combinations of the input and outputs are shown in Figure-10.

The input combinations are considered for functionality verification.

a(7:0) = 11111111; b(7:0) = 11111111
c(7:0) = 11111111 ; d (7:0) =11111111
and the resultant Sum and Carry are
s(0:9) = 0011111111 (s0 to s8) and s9 is and carry

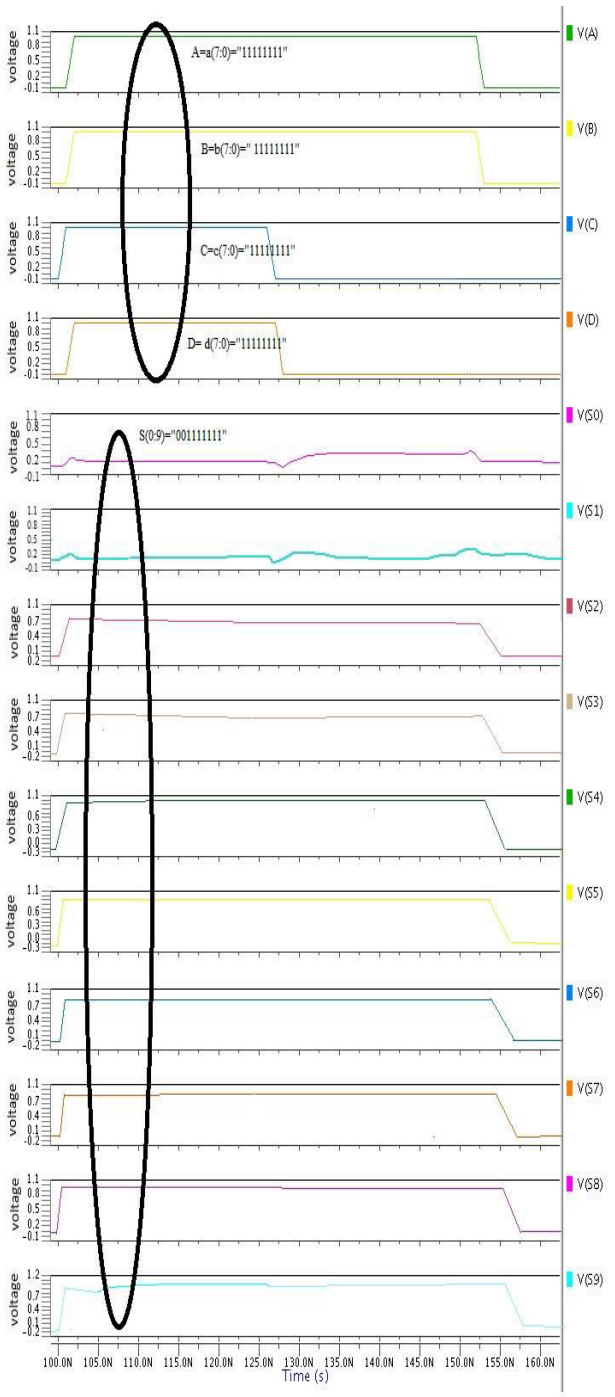

Figure-11. Output of 4 operand 8 bit CSA for the given inputs.

From Figure-10. It is observed that the generated sum and carry signal have satisfied with theoretical values. For simplicity, it has been considered that all the a(7:0), b(7:0),c(7:0),d(7:0) are connected A which is "11111111" and individual outputs are taken for sum and carry. Here carry bit is S_9. Similarly the same combinations of inputs are considered for designing of GDI and CMOS techniques and the outputs are verified.

4 operand- 16 bit CSA

After successful implementation of 4 operand 8 bit CSA, the MGDI technique has been applied to 4 operand 16 bit CSA and also verified the functionality. The architecture and test bench of this adder is similar to the Figure-8 and Figure-9. But only modification here is it requires 48 no. of one bit full adders. No particular issues were found during the implementation of this adder. The issue with pulse input voltage and W and L were already addressed in the 4 operand 8 bit CSA.

The input combinations are considered for functionality verification.

a(15:0) = "1111111111111111";
b(15:0) = "1111111111111111";
c(15:0) = "1111111111111111" ;
d (7:0) = "1111111111111111";
and the resultant Sum and Carry are
s(0:17) = " 001111111111111111" (s0 to s16) and s17 is and carry

To avoid the redundancy, architecture and test bench of this adder are not shown here. Figure-11 shows the waveforms of functionality for given input sequences.

Finally comparision has been made among CMOS,GDI and MGDI techniques for various parameters like total power dissipation, propagation delay and transistor count.Table-7. Gives the complete comparision information of 4 operand 8 bit CSA and Table-8. give the comparisoin results for 4 operand 16 bit CSA.

Table-7. Comparison of various parameters for 4 operand 8 bit CSA using different techniques.

Parameter	CMOS	GDI	MGDI
Total power dissipation In nw	812.67	$5.517x10^{6}$	$287.9x10^{-5}$
Propagation Delay In ns	350.05	198.07	152.36
Transistor Count	672	264	240

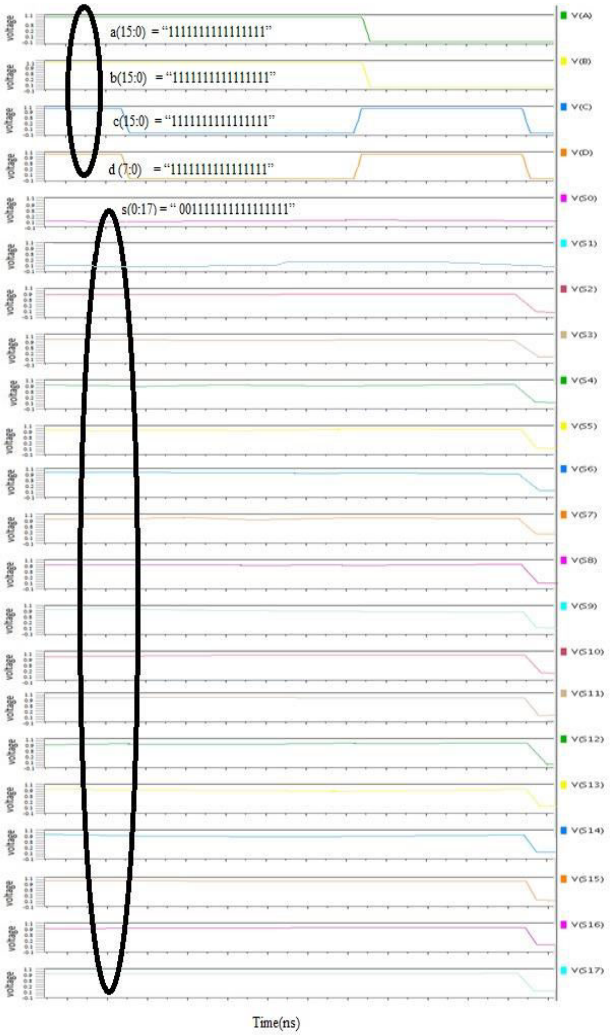

Figure-12. Output of 4 operand 16 bit CSA for the given inputs.

Table-8. Comparison of various parameters for 4 operand 16 bit CSA using different techniques.

Parameter	CMOS	GDI	MGDI
Total power dissipation In nw	$2.67x10^6$	$15.009 x10^6$	14.39
Propagation Delay In ns	486.83	248	182.30
Transistor Count	1344	480	440

CONCLUSIONS

This work proved that the MGDI technique is the best technique to get less power dissipation, propagation delay and minimum transistor count over the existing CMOS and GDI techniques. Initially, this paper presented the power, propagation delay and transistor count comparisons for basic logic gates. It is observed from the results in all the cases MGDI technique has much advantageous than the other techniques. All results have compared in 90nm technology with supply voltage of 1.8V.Also verified that one bit full adder cell and Ripple Carry Adders are also dissipates less power dissipation and less propagation delay with reduced no. of transistors. Thereafter, considered a most powerful adder called CSA and designed it for 4 operand 8 bit and 16 bit using all three techniques and verified the functionalities and are satisfied. Propagation delay is calculated for paths existing between the input to out and the highest delay has been considered. Later on comparison has been made for these adders with respect to power dissipation, propagation delay and transistor count and proved that MGDI technique exhibits less power, delay and minimum transistors. These designs can be extended to high complex processors used in signal processing and other communication applications.

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