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IMPACT OF DIFFERENT GROUND PLANES OF UTBB SOI MOSFETS ON DIGITAL AND ANALOG FOM

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ABSTRACT

In this work, we investigate the impact of different ground plane (GP) structures of the ultra-thin body and buried oxide SOI MOSFETs (UTBB SOI MOSETs) on the digital and analog figures-of-merits (FoM) with gate length of L_g= 25 nm and 10 nm. Different GP structures are found to have significant impact on the drain-induced barrier lowering (DIBL) while the impact on subthreshold-slope (SS) is negligible. Incorporation of localized ground plane of p-type in the substrate underneath the channel (referred herein as GP-B structure) provides excellent results of DIBL as of the incorporation of n+/p+/n+ structure underneath the buried-oxide (referred herein as GP–C structure). The effective suppression of the substrate depletion effect is observed with showing no increase in the potential under the channel for both GP–B and GP-C structures between low (V_d=20 mV) and high (V_d=1 V) drain bias. However, as the simulations were extended to analog FoM, it is found that only GP-B structure managed to maintain excellent result in terms of voltage gain, A_v while GP-C showed deteriorations due to an early increase in output conductance, $g_d$at low frequency.

Keywords: UTBB SOI MOSFETs, ground planes, digital and analog figures-of-merit.

INTRODUCTION

In Ultra-Thin Body and BOX (UTBB), the reduction of BOX thickness reduces the lateral electrostatic coupling between the source and drain, which allows for better control of short channel effects (SCEs) (Burignat *et al.*, 2010; Liu *et al*., 2010; Xu *et al.*, 2012). However, when the BOX is very thin, a depleted zone can extend into the underlying substrate, which causes the BOX to behave as a thick-BOX due to an increase in the BOX equivalent thickness. In order to counter this effect, implementations of ground plane (GP) doping has been introduced to limit the field penetration under the BOX from propagating to the source (Wong *et al*., 1999; Ernst *et al*., 2002).The GP can be achieved with incorporations of heavily doped substrate (Wong *et al.*,1998; Fenouillet-Beranger *et al*., 2009; Yan *et al.,* 2010; Fenouillet-Beranger *et al*., 2011; Fenouillet-Beranger *et al*., 2010). With GP, the reduction of DIBL in the order of ~50 mV has been reported (Fenouillet-Beranger *et al*., 2009; Fenouillet-Beranger *et al*., 2010) which are the results of suppression of the depletion layer under the BOX (Kumar *et al.*, 2008; Arshad *et al*., 2012). The incorporation of GP also allows for modulation of the threshold voltage if a ground plane contact is added for back-biasing (Wong *et al*., 1998; Fenouillet-Beranger *et al*., 2010; Grenouillet *et al.*, 2012; Tsuchiya *et al.*, 2004).In this work, we investigate and compare the impact of different ground planes of UTBB SOI MOSFETs. This is to determine which GP structures can effectively eliminate substrate depletion effects and produce the best digital and analog performance.

SIMULATION METHODS

Simulation methodology

The simulations were carried out using Sentaurus Device simulator. The physics models used include the hydrodynamic transport model, Lombardi mobility model and Shockley-Read-Hall recombination model.In this work, the density gradient model is used to evaluate the influence of quantization effectsThe gate length used in the simulations were of 25 nm and 10 nm in order to observe the changes in the short-channel behaviour. Graphs of drain current versus gate voltage (I_d-V_g) were plotted at V_d=20 mV and 1.0 V.We verify the simulated results of I_d-V_g for device with std-GP at L_g=25 nm are comparable with experimental results as in Burignat *et al*., 2010 and Liu *et al*., 2010.

Simulated device structure

The simulations started off with a no-ground plane (no-GP) UTBB SOI MOSFET structure with $V_d$of 20 mV and 1 V. Gate voltage (V_g) is swept from 0 to 1.5 V in 10 mV incremental steps. The buried oxide (BOX) and Si-body thickness are 10 nm and 7 nm respectively. The channel was undoped with acceptor concentration of $6.5x10^{14}$ cm^{-3} while S/D donor concentrations doping are of $1x10^{20}$ cm^{-3}. Metal gate work function of 4.65 eV and an effective oxide thickness (EOT) of 1.2 nm were used.Detailed reviews on advanced silicon-on-insulator MOSFETs can be found in Arshad *et al.*, 2015.

We made comparison of the no-GP structure with several ground plane structures as illustrated in Figure-1 i.e. standard ground plane (std-GP), ground plane A (GP-A), ground plane B (GP–B) and ground plane C (GP–C).

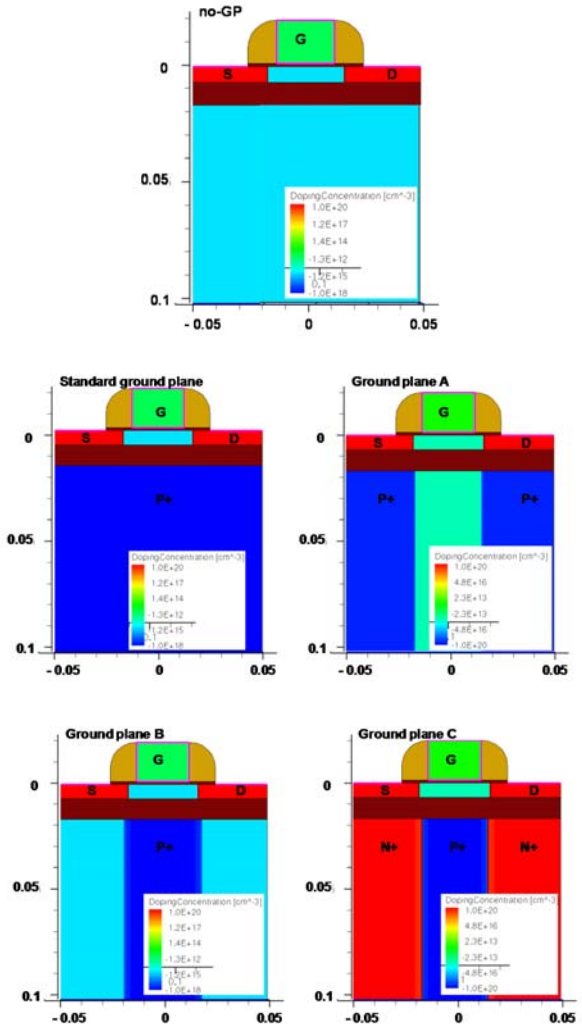

Figure-1. Different ground plane structures of UTBB SOI MOSFETs: no-GP,standard ground plane (std-GP), ground-plane A (GP-A), ground-plane B (GP-B) and ground-plane C (GP-C).

The std-GP structure employed a thin layer of P+ doping of $1x10^{18}$ cm^{-3} under the BOX region. For GP-A structure, P+ doping of $1x10^{20}$ cm^3 were created under the S/D area, which are similar to Makiyama *et al*., 2012. InGP-B structure, P+ doping of $1x10^{18}$ cm^3 was formed under the channel. The last structure of GP-C simulated N+ doping of $1x10^{20}$ cm^{-3} under the S/D area while area under the channel was P+ doped with $1x10^{20}$ cm^{-3}. This structure was similar to Yan *et al*., 2010. All these structures can be done in a self-aligned manner: the formation of localized highlydoped regions in the substrate underneath the BOX has been demonstrated both theoretically and experimentally(Xiong & Colinge, 1999)(Xiong *et al*., 2002).We then extend our analysis by reducing the gate length from the initial 25 nm down to 10 nm to observe the changes in the short-channel behavior

RESULTS AND DISCUSSIONS

DIGITAL FIGURES-OF-MERIT

Drain-induced barrier lowering, DIBL

DIBL is caused by the encroachment of the depletion region from the drain into the channel due to high drain bias (V_d), which in turn causes the lowering of the potential energy barrier for electrons in the channel. As a result, drain current, (I_d) increases and the threshold condition can be reached at a lower gate voltage (V_g) since the drain has already created a large portion of the depletion region. Strong DIBL is an indication of poor short-channel behavior as it implies that the gate no longer has total control over the channel. The strength of the DIBL is usually measured as the difference in V_{th} between a low V_d (i.e. V_d=20-100 mV) and a high V_d (i.e. V_d=1 V).In this work, DIBLis extracted as $(V_{thlin}-V_{thsat})/\Delta V_d$(Colinge & Colinge, 2002) at drain current, I_d of 10^{-7} A for two drain voltages i.e. V_d=20 mV and V_d=1.0 V. This method is widely used and seems to be the most suitable method to extract DIBL.

Figure-2 shows the DIBL extracted at two different gate lengths i.e. L_g=25 and 10 nm. As expected, when the gate length is reduced, DIBL is also increased. At L_g=10 nm, both GP–B and GP–C showed comparable results with both seemed to exhibit the lowest DIBL as compared with other GPs.In order to explain the superiority of GP-B and GP–C structures and to investigate substrate depletion effects, we take a look at the horizontal potential ($\phi_{Horizontal}$) distribution at 1 nm under the substrate/BOX interface from the source through the channel and end at the drain as shown in Figure-3 for 10 nm gate length. As reported in Othman *et al*., 2014, the simulated DIBL curves translate into different space-charge conditions at the substrate/BOX interface. DIBL is a function of gate voltage that is highly dependent on ϕ_F whereby ($V_{th}=V_{fb}+2\phi_F+(|Q_d|/C_{ox})$. At the substrate/BOX interface, the surface potential referred to quasi-neutral substrate,i.e.$\phi_s=\phi_{Horizontal}-(V_{sub}-\phi_F)$ where ϕ_F here is the Fermi level equals to 276 mV which allows for examining the potential rise due to drain bias in terms of the obtained operating regime, i.e.ϕ_s <0 indicates accumulation, $0<\phi_s<0.53$ V indicates depletion and$\phi_s>$ 0.53 V indicates strong inversion. One can see that:

i. In the channel, GP–B and GP-C are in accumulation, whereas standard-GP and GP-A are in depletion while no-GP is in inversion. For GP-B, the depletion region terminate within the S/D boundary under the BOX, without extending into the channel region (unlike of std-GP).
ii. When the drain bias is increased from V_d=20 mV to V_d=1.0 V, the potential remain the same i.e. there is no increase of potential under the channel region for GP-B and GP–C. This shows that both GPs provide better shield to the channel from the influence of drain electric field when a high drain voltage is applied. This benefit translates into the low DIBL value as illustrated in Figure-2 for 10 nm gate length.

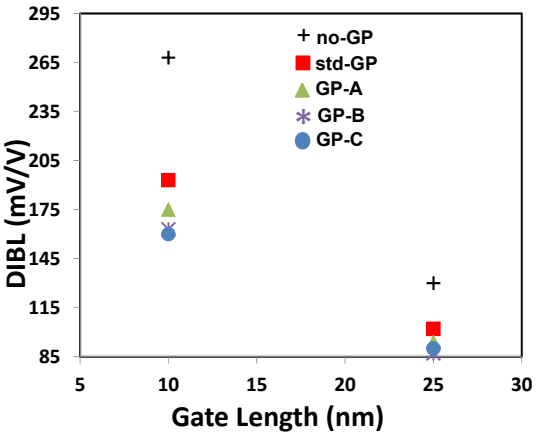

Figure-2. Results of DIBL as a function of gate length, L_g.

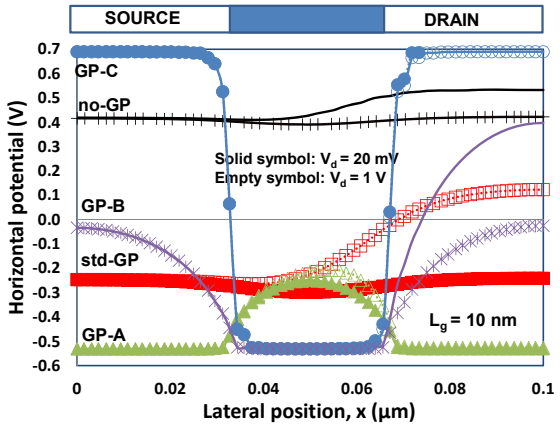

Figure-3. Horizontal potential along the substrate/BOX interface at linear (V_d=20 mV) and at saturation (V_d=1 V) for L_g=10 nm.

Subthreshold slope, SS_{lin}

Next, we look into the subthresholdslope, since GP structures normally yield higher body factor than no-GP due to suppression of depletion effect (Arshad *et al.*, 2013).S-slope can be defined as the change in gate bias (V_g) required to change the subthreshold drain current (I_d) by one decade as given by $SS=\Delta V_g/\Delta \log I_d$. In other words, it indicates how effective the flow of drain current of a device can be stopped whenV_g is decreased below V_{th}. Low S-slope is desirable as it indicates faster transition of the transistors from OFF to ON state. Table-I shows that higher S-slopewere obtained when the gate length is being reduced. It can be seen that GP structures showed better S-slope than no-GP. However, the improvements of S-slope with different GPs are quite small in overall (only between 3mV/dec-8mV/dec improvements). Although GP-B and GP-C are highly doped underneath the channel, they did not degrade the S-slope. This shows that both structures provide greater capacitive coupling between gate and channel, hence a better control of the gate over the channel potential(Numata *et al.*, 2002; Numata and Takagi, 2004).

Table-1. Linear subthreshold slope (mV/dec) versus gate length.

	L_g=25 nm	L_g=10 nm
No-GP	**89**	**112**
Std-GP	**79**	**96**
GP-A	87	95
GP-B	79	93
GP-C	79	94

Analog figures-of-merit

From digital, we extend our investigation to analog figures-of-merit. Ingeneral, the amplifying performance of analog transistors deteriorates with increasing frequency. In Makovejev, 2012, it is reported that the analogue performance degradation caused by the substrate effects are stronger than self-heating for UTBB devices with 7-8 nm Si body and 10 nm BOX. Moreover, the effect of parasitic elements whose impact on the device performance increases enormously in deeply downscaled devices can also be seen in the evaluations of a wide-frequency band (Kilchytska *et al.*, 2014; Arshad *et al.*, 2014).In this work, we look into different perspective i.e. the analogue performance of the different GP structures with L_g=10 nm evaluated for frequency range from 0.01 Hz to $1x10^{14}$Hz. The evaluations are made on the results of the transconductance (g_m), output conductance (g_d) and intrinsic gain (A_v).

Small-signal transconductance, g_m

In small-signal analysis, g_m as a function of frequency is determined from the Y-parameter, $g_m=|Y_{21}-Y_{12}|$where Y_{21} is the forward transconductance and Y_{12} is the reverse transconductance.The maximum transconductance was normalized to the gate width and length and is given by: $g_{m\_max\_norm}=g_{m\_max}/(W/L)$.From Figure-4(a), it can be seen that different GP structures only give minor impacts on the results of $g_{m\_max\_norm}$.This can be seen from Figure-4(b) that reveals GP-C structure showing a slight increase of $g_{m\_max\_norm}$ at a much lower frequency in contrast with its other 3 GP counterparts. However, the $g_{m\_max\_norm}$ differences between the GP structures can still be considered very small i.e. ~12 μS.

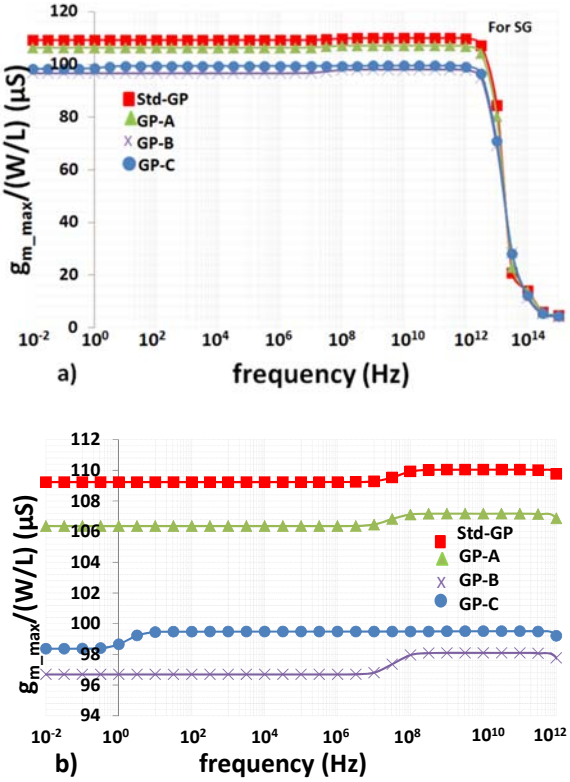

Figure-4. (a) $g_{m\_max}/(W/L)$ as a function of frequency. L_g=10 nm, W=1 µm and V_d=1 V. (b) Emphasizing slight differences of $g_{m\_max}/(W/L)$ between the different GP structures as a function of frequency.

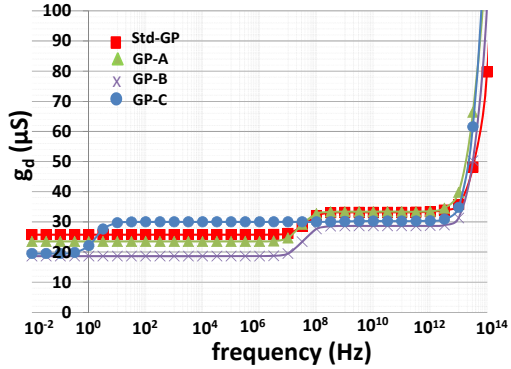

Figure-5. Simulated g_d as a function of frequency for SG .L_g=10 nm, W=1 µm.

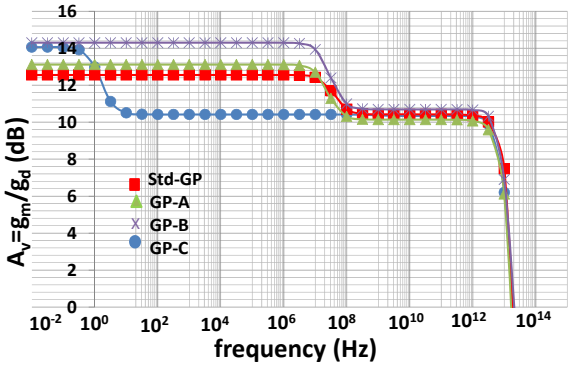

Figure-6. Intrinsic gain, A_v as a function of frequency.L_g=10 nm, and V_d=1 V.

Intrinsic gain, A_v

The amplification factor, also called gain, is the extent to which an active device boosts the strength of a signal. Variation of voltage gain is denoted as $A_v=g_m/g_d$ where $g_m=|Y_{21}-Y_{12}|$ and $g_d=Y_{22}$. Figure-5 shows the results of the corresponding g_d (refer to Figure-4 for the g_{m_max}).It can be seen that with an increase in frequency, $g_d$also increases. Different GPs are translated into g_d increase at different frequency level with GP-C is the first one to increase. From Figure-6, different GP structures were found to have only minor impacts on the maximum A_v that varies from 12 dB to 14 dB, due to a more pronounced effect of $g_d$on A_v as compared to g_m. This is evident where it is noted that the gain for GP-C started to drop at a very low frequency which correspond to an increase in g_d as shown in Figure-5. The same trend is also observed for std-GP, GP-A and GP-B. In overall, GP-B which showed the best DIBL among its GP peers in the digital analysis, managed to maintain good A_v results in terms of the highest maximum A_v and a stable gain up to 10 MHz frequency.

CONCLUSIONS

In this work, implications of different ground plane (GP) structures on the digital and analogFoM were evaluated. It is found that the introduction of p+ doping under the channel as in GP-B and GP-C structures enable potential pinning in the channel area, resulting in no increase in the potential under the channel between low (V_d=20 mV) and high (V_d=1 V) drain bias. Meanwhile, in the analogFoM, the different GPs seemed to give impacts on the voltage gain, A_v (degradation at different frequency) as a result of different g_d increase across the frequency range. It is found that as the simulations were extended to analogFoM, only GP-B structure managed to maintain excellent result in terms of voltage gain, A_v while GP-C showed deteriorations due to an early increase in output conductance, $g_d$at low frequency.Overall, the application of GP is dependent on the device application i.e. digital or analogFoM.

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