VOLTAGE CLAMP SIMULATIONS OF CARDIAC EXCITATION: FPGA IMPLEMENTATION

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ABSTRACT

This paper presents the simulation study of voltage clamp technique that enables to analyse current-voltage (I-V) characteristics of ion currents based on Luo-Rudy Phase-I (LR-I) model by using a Field Programmable Gate Array (FPGA). Here, the I-V relationship presents the characterization of each ion channel by a relation between membrane voltage, $V_m$ and resulting channel current. In addition, the voltage clamp technique also allows the detection of single channel currents in biological membranes and is known to be applicable in identifying variety of electrophysiological problems in the cellular level. As computational simulations devote a vast amount of time to run due to the increasing complexity of cardiac models, a real-time hardware implementation using FPGA could be the solution as it provides high configurability and performance, and able to executes in parallel mode operation for high-performance real-time systems. For shorter time development while retaining high confidence results, FPGA-based rapid prototyping through HDL Coder from MATLAB software has been used to construct the algorithm for the simulation system. Basically, the HDL Coder is capable to convert the designed MATLAB Simulink blocks into hardware description language (HDL) for the FPGA implementation. As a result, the MATLAB Simulink successfully simulates the voltage clamp of the LR-I excitation model and identifies the I-V characteristics of the ionic currents through Xilinx Virtex-6 XC6VLX240T development board.

Keywords: voltage clamp, luo-rudy phase-I model, field programmable gate array, MATLAB simulink HDL coder.

INTRODUCTION

Voltage clamp technique allows the detection of single channel currents in biological membranes and is known to be applicable in identifying variety of electrophysiological problems in the cellular level. During the implementation of the voltage clamp to the cell, the membrane potential is kept at a controlled value which is typically at several constant levels with stepwise changes to record the transmembrane current [1]. This technique has contributed to the understanding of the electrical behavior of the current-voltage (I-V) characteristics of the ionic currents [2, 3, 4]. Here, the I-V relationship presents the characterization of each ion channel by a relation between membrane voltage, $V_m$ and resulting channel current. Due to a tedious and an expensive procedure of the voltage clamp experiment, a simulation approach of the voltage clamp is more preferred as it is easier and cost effective. However, simulating the dynamics of cellular models requires a significant amount of computational processing time which would increase a time required for computer simulation of the models [2]. In addition, the voltage clamp method needs to be developed by real-time system because it requires the real-time evaluation and injection of simulated membrane current. In order to solve the problems, the real-time hardware implementation is needed to model the I-V on ion currents.

In [5, 6, 7] real-time analog-digital hybrid model has been developed in order to perform I-V relationship of six ionic currents which are a fast inward sodium current ($I_{Na}$), a slow inward current ($I_h$), a time-dependent potassium current ($I_K$), a time-independent plateau potassium current ($I_{Kp}$), a time-independent plateau potassium current ($I_{Kp}$) and a background current ($I_s$) based on the Luo-Rudy Phase-I (LR-I) model [8] for hardware implementation. However, one of the ionic currents, which is a fast sodium inward current, $I_{Na}$ was not quantitatively comparable because the $I_{Na}$ produced by hybrid model relatively smaller than the LR-I model since it was developed by analog circuit. Therefore, digital implementation of Field Programmable Gate Array (FPGA) is one of the solutions needed to solve the analog problem because it is capable to run in real-time simulation, and it can be adapted to any changes in design by dynamic reconfiguration. Moreover, it provides high configurability and performance and also executable in parallel mode operation [9, 10]. Thus, through this study, a real-time performance of voltage clamp simulations in quantitative descriptions of the six ionic currents of the LR-I model for single biophysical cellular membrane can be realized by using the FPGA.

The structure of this paper is as follows. Discussion on the methodology with an overview of the proposed system applications is presents in next section. Research findings are presented on the next section. Finally, concluding remarks are given in the last section of this paper.

DESIGN METHODOLOGY

In this research, voltage clamp simulation is developed based on the LR-I model [8]. The LR-I is developed to model the generation of cardiac excitation for mammalian ventricular cell. This model is chosen because it well described the six ionic currents that retain enough structure of basic currents involved in cardiac excitation to reproduce exact AP morphologies [11] and is flexible enough that the parameters can be fitted to replicate accurately the properties and dynamics of other
complex ionic models as well as experimental data [12-13] such as action potential duration (APD), thresholds for excitation, upstroke velocities, minimum APD before reaching conduction block, and phase-locking response characteristics to current stimulations. Based on the previous work, the LR-I algorithm has been done for FPGA hardware implementation [14-15]. The work is designed by using the MATLAB Simulink that gives an opportunity for obtaining Hardware Description Language (HDL) code without handwriting of the HDL code and by using an automatic code generation process [10]. Moreover, HDL Coder also has a tool to verify the code (HDL) code without handwriting of the HDL code and by using an automatic code generation process [10]. The work is designed by using the MATLAB Simulink that gives an opportunity for obtaining Hardware Description Language (HDL) code without handwriting of the HDL code and by using an automatic code generation process [10].

**FLOATING-POINT VOLTAGE-CLAMP OF LR-I MODEL**

**TIME-INDEPENDENT IONIC CURRENTS**

Figure 3(a) shows the result of the I-V relationship of $I_{Ki}$. The LR-I time-independent potassium current, $I_{Ki}$ plays a role to maintain the resting potential as it flows at negative potential. The LR-I time-independent plateau potassium current $I_{Kp}$ is activated during the plateau phase of the action potential along with the other potassium currents to restore the cell to its resting state. This current does not flow at low but at high membrane potential. A graph of the I-V relationship of $I_{Kp}$ for the LR-I model designed by using the MATLAB Simulink is depicted in the Figure-3(b). The background current, $I_b$ in the LR-I, is a composite current representing the hodgepodge of other currents left in the cell. The I-V relationship of this current is a linear function of membrane potential. Plots of the I-V relationship of $I_b$ is shown in Figure-3(c). These I-V relationships of $I_{Ki}$, $I_{Kp}$ and $I_b$ obtained from the MATLAB Simulink are generally comparable to the features of LR-I model [8].

**TIME-DEPENDENT IONIC CURRENTS**

The fast inward sodium current $I_{Na}$ in the LR-I causes the rapid upstroke of the action potential. A short time-constant behavior of $I_{Na}$ is reproduced by using the MATLAB Simulink blocks as shown in Figure-4(a). Dynamics of $I_{Na}$ are analyzed by plotting the ion current over time in response to the voltage step inputs as refer to the voltage clamp experiment with various clamp voltage from -60 mV to 80 mV by voltage clamp step of 20 mV. The LR-I time-dependent potassium current $I_{K}$, is activated by the increase of the membrane potential and it is not activated until the cell returns to its resting state. A long time-constant behavior of $I_{K}$ is reproduced by using the MATLAB Simulink. The dynamic response of the current to the voltage step shown in Figure-4(b). The slow inward current $I_{si}$ flows due to the entry of $Na^+$ during the plateau phase. $I_{si}$ changes slowly over time. Figure 4(c) illustrates the dynamics response of $I_{si}$. These I-V relationships of $I_{Na}$, $I_{K}$ and $I_{si}$ from the MATLAB Simulink are generally comparable to the features of LR-I model [8].

**FIXED-POINT VOLTAGE-CLAMP OF LR-I MODEL**

In this paper, the fixed-point voltage clamp of $I_{K}$ is designed by using MATLAB Simulink as depicted in Figure-5 and Figure-6. The clock is used to represent the simulation time based on the step size of 0.001 ms. Data type converter block is used to convert the double data types into fixed-point data types. Whole algorithm of voltage clamp of $I_{K}$ of Luo-Rudy phase-I is designed inside the light blue subsystem. Lastly, the result is displayed on the scope current_of_IK is illustrated in Figure-7.
Figure-2. The designed MATLAB Simulink blocks for the voltage clamp simulation of $I_k$. 
Figure-3. Time-independent I-V characteristic waveforms. Panels (a), (b) and (c) represents corresponding $I-V$ characteristic of $I_{K1}$, $I_{KP}$ and $I_b$, respectively.
Figure-4. Time-dependent I-V characteristic waveforms in response to various intensity of voltage step inputs (from -60 mV to 80 mV) for an initial holding voltage of -85 mV. Panels (a), (b) and (c) represents the I-V characteristics of $I_{Na}$, $I_K$ and $I_{le}$, respectively.

Figure-5. Top level of voltage clamp $I_K$ fixed-point.
Figure-6. Voltage clamp $I_K$ inside the subsystem.

Figure-7. Voltage clamp of $I_K$ by using fixed-point.
FPGA-IN-THE-LOOP OF VOLTAGE CLAMP MECHANISM

FPGA-in-the-Loop (FIL) is one of the HDL Verifier approaches to test the behaviour of the designed algorithm for FPGA hardware implementation. The FIL is done by using HDL Workflow Advisor tool. After the process of running the tool finished, the new model named as voltage_clamp_of_IK_fil block is generated as shown in Figure-8. Next, the program file is loaded through the JTAG and ethernet cable by clicking the generated block. Then, the simulation is runned to get the results to be displayed on the scope as shown in Figure-9. Simulation by using MATLAB software and FPGA board is verified by using FPGA-in-the-Loop approach and shows no difference which indicates a high confidence level in the FPGA-based simulations.

SYSTEM-ON-BOARD OF VOLTAGE CLAMP MECHANISM OF IK

The generated code is implemented on the XC6VLX240T FPGA Xilinx Virtex-6 board. Table-1 shows the summary of the utilization of the board for voltage clamp of $I_K$.

<table>
<thead>
<tr>
<th>Table-1. Summary utilization of voltage clamp $I_K$ on FPGA Virtex-6.</th>
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<tr>
<td><strong>Slice register</strong></td>
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<td><strong>Slice of LUTs</strong></td>
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<td><strong>IOBs</strong></td>
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<td><strong>DSP48E1s</strong></td>
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<td><strong>Maximum Frequency (MHz)</strong></td>
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<td><strong>Power (mW)</strong></td>
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CONCLUSIONS

In conclusion, the AP dynamics is successfully designed by using MATLAB Simulink that could generate the AP that is quantitatively comparable to the previous LR-I model [8]. This mathematical model is designed using MATLAB Simulink in order to implement it on the FPGA since this graphical user interfaces have significant link in order to auto-generated HDL code that will be used for FPGA board programming afterwards. In order to develop FPGA algorithm design by using MATLAB Simulink, several processes have been performed. These include the process of designing algorithm using a fixed-point data type in discrete-time system using the Simulink HDL supported libraries and applying optimization in setting the value of the fixed-point data type to enhance the performance of the designed system according to the speed, power consumption and hardware utilities. For future work, the designed model will be implemented on FPGA board for the stand-alone implementation of the system. Besides, other mechanisms such as conductions in cardiac tissues could be performed on FPGA board.

Figure-8. New voltage_clamp_of_IK model generated for FIL verification.
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REFERENCES


