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LOW POWER CMOS CIRCUIT DESIGN FOR R WAVE DETECTION AND SHAPING IN ECG

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ABSTRACT

R wave is an important morphological feature in ECG which plays a vital role in identifying Cardiac arrhythmias. A band pass filter is used to detect QRS complex which after rectification is shaped into a 200ms square pulse utilizing comparator circuit with auto threshold. This is implemented in 180nm technology and is simulated using Cadence Virtuoso. The circuit is tested with simulated ECG with heart beat ranging from 40 beats/min to 200 beats/min with an operating voltage of 0.4V and total power measured is 3.997µW.

Keywords: cardiac arrhythmias, QRS complex, R-wave.

1. INTRODUCTION

QRS complex is detected as pulse to identify cardiac arrhythmias. The various morphological features and amplitude provide more information that helps the doctors to analyze and diagnose heart diseases. Apart from this several algorithms have been developed to detect the QRS complex accurately with offline data [1]. Algorithms for detecting QRS complex like nonlinear transformations using differentiation [2], a combination of differentiation, squaring and integration, a combination of differentiation and correlation, methods based on optimized and matched filtering, adaptive methods, wavelet transform, neural networks, combination of wavelet transform and neural-network based adaptive filtering, and quite recently proposed methods based on mathematical morphology, voting algorithm , geometrical matching and modified p-spectrum [3].

The properties of QRS complex like Slope, Amplitude and Width are considered and an algorithm is constructed by Pan Tompkins for real time applications [4]. A futuristic approach is introduced on simple moving average with wavelet based de-noising for real time detection. Most of the pre-recorded data is used to analyze the Cardiac Arrhythmias condition in real-time which is most essential to understand the practical requirements.

In practical patient monitoring and diagnostic system the heart rate variability(HRV), any abnormalities, classification arrhythmias has been inherently calculated in QRS detection methods based on software[5]. The QRS detector must be optimized for various conditions like high respiration, moving patient which are noise prevalent. But to design a system with above factors and to reduce the noise the Application Specific Integrated Circuit (ASIC) is required [6].

ASIC chips are designed using linear filtering and peak detection techniques to implement the QRS detection with threshold. Non-linear transformation and wavelet transform are also used to enhance the detection of QRS complex. Some of the QRS detectors reviewed in the literature have used wireless transmission [7]. Which are operated with supply voltage ranging from 2.5-3.3V and consumes current of 30 µA except transmitter. A QRS detector chip for wireless health monitoring system is developed with piezo-microphone sensor and a transmitter operating with 0.9V and consuming 7.5 µA.

The programmable DSP HR for the ASIC model [8] is implemented in 1 µm CMOS technology with specified Supply voltage and Power consumption values. The wavelet transform technique is utilized in the chip implementation [9] which detects the peaks values by Dynamic Trans-linear circuit approach [10]. It has 5 Parallel scales and the reported power consumption is 55nW with the supply voltage of 2V which implemented in custom Bipolar IC design process. The design which is presented in another proposed model is developed and implemented in 0.13 µm technology with a supply voltage of 1.2V which includes the same transformation of wavelet and includes a wavelet transformation ratio threshold along with filter banks for wavelets [11] with the power consumption of 114 nW and 37.9 nW in alert and normal modes. The other demonstrated models comprise of filter banks and multi-scale multipliers is implemented in 0.18 µm technology with simulated power consumption of 644.9 nW when all the filters are active and 318.4 nW in normal operation [12]. When first half of the filters are active 90% of the power consumption is caused by deep submicron technology which has leakage issues. As a final point of cessation, among the many presented models in literature review, a very rare number of models have a supply voltage of below 1V.

The design approach is presented in Section II which introduces the principle operation of half wave rectifier, sample and hold circuit, Comparator and Monostable circuit. Section III reports the measurement results. The proposed work is concluded in Section IV.

2. SYSTEM DESIGN

The block diagram of the system for detecting R-peak and shaping it into 200ms is in Figure.1. The ECG signal is filtered by band pass filter that allows only QRS complexes which was given input to the proposed system. The half wave rectifier removes the negative components

Q and S in the QRS complex and allows only R peak. The sample and hold circuit samples this R peaks which set an automatic threshold for the comparator when turned ON triggers a monoshot produces 200ms pulse. This in turn triggers a second monoshot to produce the pulse of 50ms duration to act as a sampling clock.

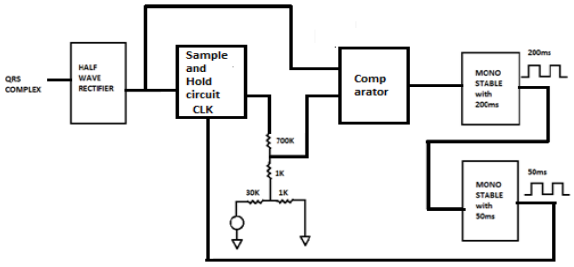

Figure-1. R peak detection and shaping circuit

Design of half wave rectifier

A low power half wave rectifier is designed using floating current source and four complementary MOS transistors M1, M2, M3 and M4 which are connected as two differential pairs as M1-M2 and M3-M4 are assumed to match and operate in the saturation region. The symbol and circuit is shown in Figures.2 & 3. The output current generated from circuit is balanced to gratifying the Kirchhoff's current law. The output current equations are given below.

$$I_{B2} = I_{B1} + I_{O1} + I_{O2} \quad (1)$$

$$I_{B2} = I_{B1} \quad (2)$$

$$I_{O1} = -I_{O2} \quad (3)$$

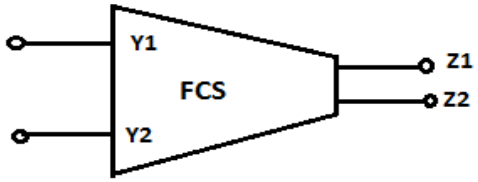

Figure-2. Symbol of floating current source.

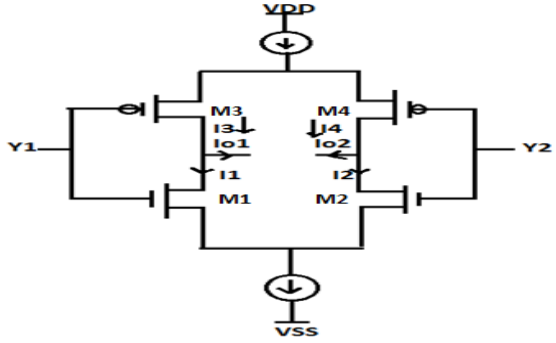

Figure-3. CMOS Implementation of floating current source circuit.

The transconductance of M1 - M_2 ($g_{m1} = g_{m2}$) and M_3 – M_4 ($g_{m3} = g_{m4}$) are equal as they are assumed to equal transistors. The transconductance and output impedance of the FCS circuit is given in equation (2) & (3).

$$g_{mo1} = -g_{mo2} = (g_{m1} + g_{m3}) / 2 \quad (4)$$

$$R_{o1} = R_{o2} = [(((g_{m3} g_{ds3}) / (g_{m3} + g_{m4})) + ((g_{m1} g_{ds1}) /(g_{m1} + g_{m2})))]^{-1} = 2/(g_{ds1}+g_{ds3}) \quad (5)$$

Two balanced output currents are given by

$$I_{o1} = -I_{o2} = -1/2\ V_d\ [\sqrt{k_n}\ \sqrt{(I_{B1} - (k_n V_d^2/4))}] + \sqrt{k_p}\ \sqrt{(I_{B1} - (k_p V_d^2/4))} \quad (6)$$

Where $V_d = V_1 - V_2$

V_1 and V_2 are voltages applied to Y_1 and Y_2 respectively K_n and K_p is the NMOS and PMOS transconductance parameters given by

$$K_n = \mu_n\ C_{ox}\ W_1 / L_1 \quad (7)$$

$$K_p = \mu_p\ C_{ox}\ W_1 / L_1 \quad (8)$$

Where
μ = mobility of carrier
C_{ox} = gate capacitance per area
W_1, L_1 = Channel width and channel length of MOS transistor.
I_{B1}, I_{B2} = bias currents

Half wave rectifier circuit consists of FCS, four diode and resistor. The folded current source circuit convert voltage source QRS complex into two current sources. The current source is rectifying by four diodes which are constructed by two transistors M_{D1} and M_{D2} and one pair of diode current is connected to ground as the rectification is half wave. The current output from diode is converted into voltage using M_{R1} and MR2 CMOS transistor which are acted as resistor R_o in saturation region. D_1 and D_2 are initiated to ready for conduction by bias voltage V_b which is shown in Figure-4.

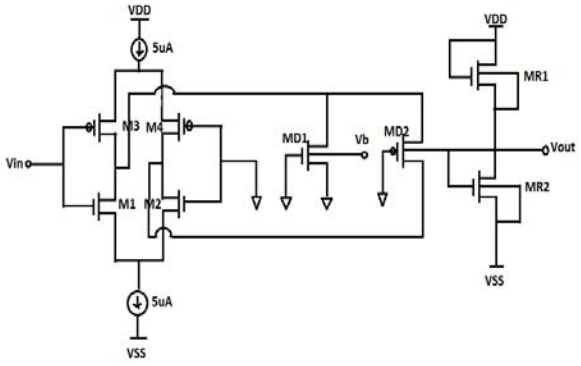

Figure-4. CMOS design of half wave rectifier.

The R_o and the relativity of the positive and negative polarity input voltage and output voltage are expressed as

$$K_p = \mu_p C_{ox} W_1 / L_1 \quad (8)$$

Where V_{TH} is the threshold voltage
and $V_{GS}=V_{DD}=|V_{SS}|$
$V_{in} < 0$ $I_{out} = -(g_{m1} + g_{m3})$ Vin/2, $V_{out} = I_{out} . R_o$

$V_{in} > 0$ $I_{out} = (g_{m1} + g_{m3})V_{in}/2$, $V_{out} = I_{out} . R_o$

The schematic and simulation result of half wave rectifier in Cadence environment is given in Figure-5 & Figure-6.

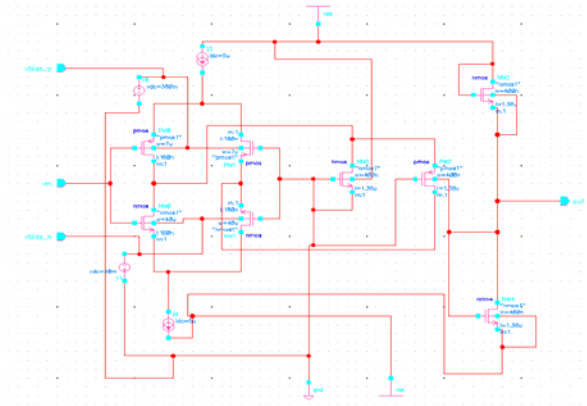

Figure-5. CMOS design of half wave rectifier in cadence.

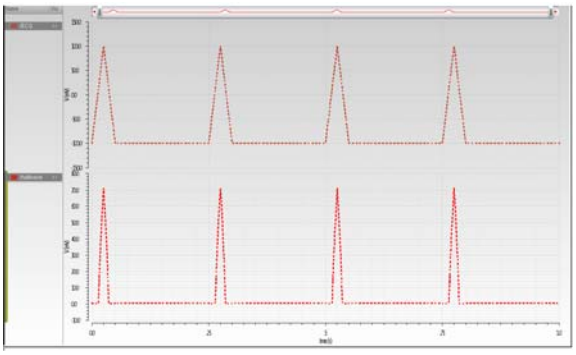

Figure-6. Simulation result of half wave rectifier in cadence environment.

Design of sample and hold circuit

Sample & Hold Circuit is designed to sample the positive QRS complex with 50ms clock and to hold the sampled value for a short interval. The sample and hold circuit is shown in Figure-7. The sampling clock controls whether to sample the input signal or hold the last sampled value of QRS complex. When the pulse is high the signal is sampled and is low the signal value is holded. Thus the circuit has two modes of operation depending upon the logic level of clk signal. Upon receiving the input clock pulse, the circuit samples the input and output follows input by voltage follower. The schematic and simulation result of sample hold circuit in Cadence environment is given in Figure-8 & Figure-9.

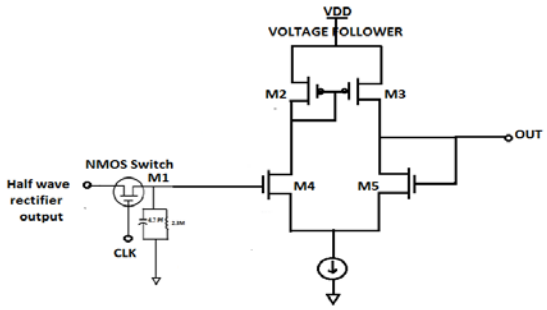

Figure-7. CMOS design of sample and hold circuit.

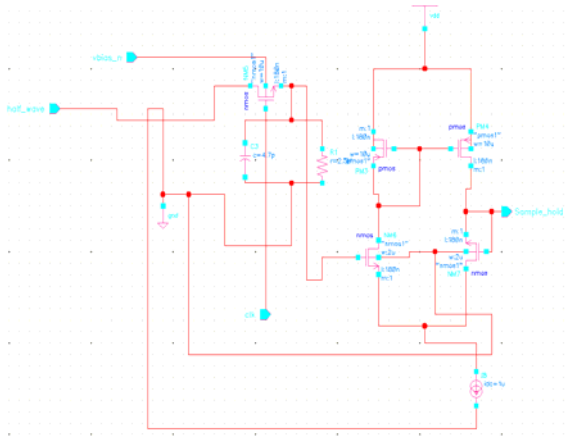

Figure-8. CMOS design of sample and hold circuit in cadence.

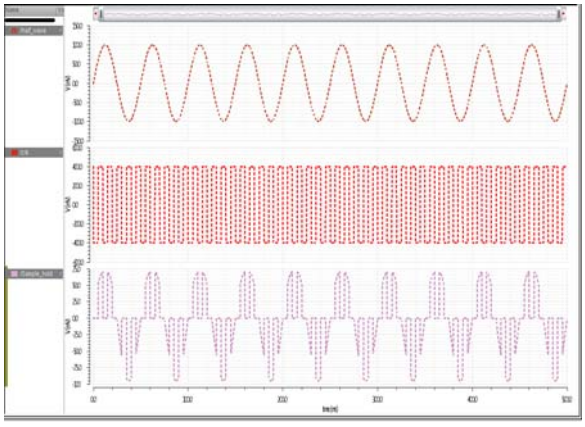

Figure-9. Simulation result of sample and hold circuit in cadence environment.

Design of comparator

The low power comparator is designed by using differential amplifier. It compares half wave rectifier output and with reference voltage. The reference voltage is generated by potential divider with samples from sample

and hold circuit. M2, M3 and M6, M7 transistors are differential pairs.

If Vin = Vp – Vn < Vref Vout = -Vdd

If Vin = Vp – Vn > Vref Vout = +Vdd

The half wave rectifier signal is less than Vref, the non-inverting input of the comparator is less than the inverting input. The output will be LOW at the negative supply voltage -Vdd resulting in a negative saturation of the output.

The half wave rectifier signal is greater than Vref, the non-inverting input of the comparator is greater than the inverting input. The output will be high at the positive supply voltage +Vdd resulting in a positive saturation of the output. Based on this comparator operation, the R-Peak is identified using suitable Vref . The value of Vref is set automatically based on QRS complex R-peak value using potential divider circuit. The CMOS comparator circuit is shown in Figure-10. The schematic and simulation in Cadence environment is given in Figure-11 & Figure-12.

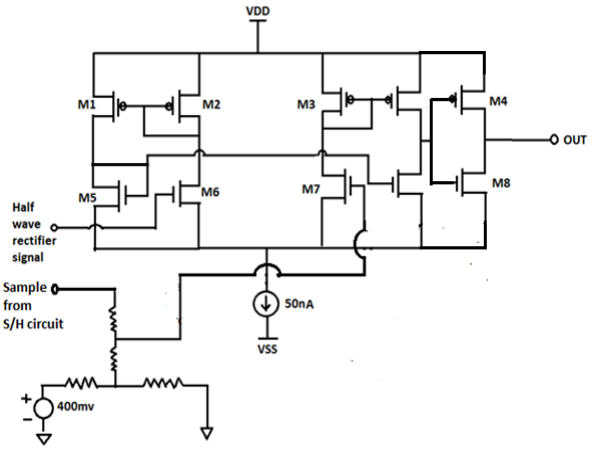

Figure-10. CMOS design of comparator.

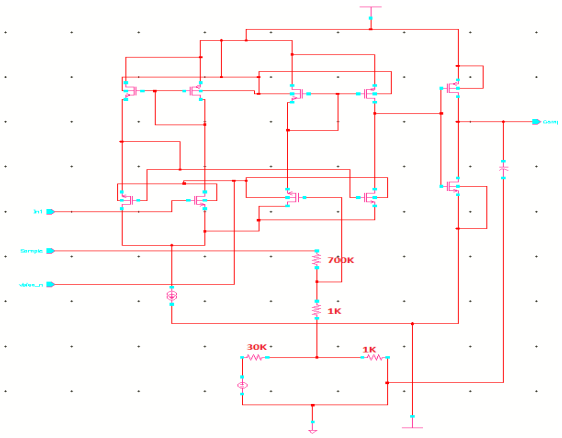

Figure-11. CMOS design of comparator in cadence.

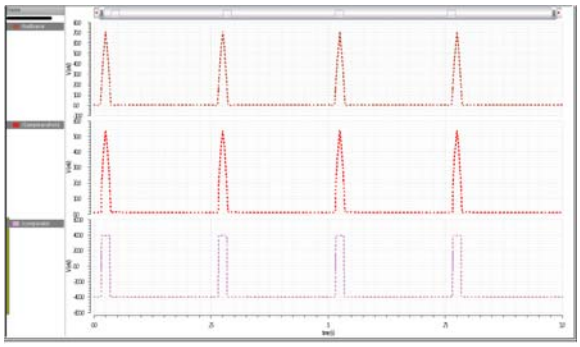

Figure-12. Simulation result of comparator in cadence environment.

Design of monostable multivibrator

Monostable Multivibrators are designed to generate the refractory period of 200ms and to sample the QRS complex with 50ms sampling rate. It is triggered by comparator output pulse where the pulse is denoting the R-peak. Refractory time period is set by the time constant of the RC coupled circuit. The expression for time constant is given below

T = 0.69 RC (6)

The monoshot circuit is given in Figure. If the R-peak pulse trigger is low, the first NOR gate output is high. The resistor R is connected to the supply voltage. So the capacitor C has the same charge on both of its plates. The Junction of R and C voltage is equal and the second NOR gate output is low and the circuit is in "Stable State" with zero output. The R-peak pulse trigger is high, the first NOR gate output is low. So the capacitor C has logic 0 and start to discharge. The second NOR gate output is high and the circuit is in "Unstable State with an output voltage equal to +Vdd.

The second NOR gate maintain unstable state until the timing capacitor charging up through resistor, R reaches the minimum input threshold voltage of second NOR gate. This cause it to change state as logic level "1" value has appeared on its inputs. And change the output into logic "0" which in turn feedback to first NOR gate input. This action automatically returns the monostable back to its original stable state and awaiting a second trigger pulse to restart the timing process once again. The CMOS design of Mono stable circuit is shown in Figure-13. The schematic and simulation in Cadence environment of Mono shot circuit with 200ms width and Mono shot circuit with 50ms width is given in Figure-14, Figure-15, Figure-16 & Figure-17.

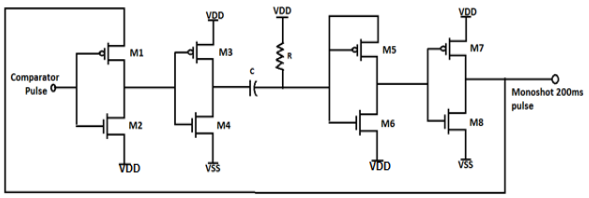

Figure-13. CMOS circuit design of mono shot circuit.

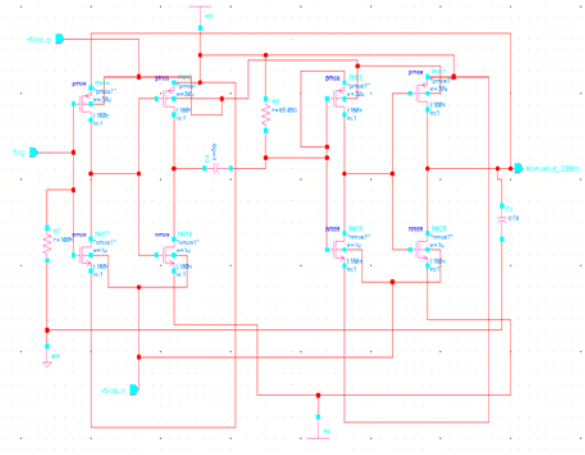

Figure-14. CMOS design of mono shot with 200ms width in cadence.

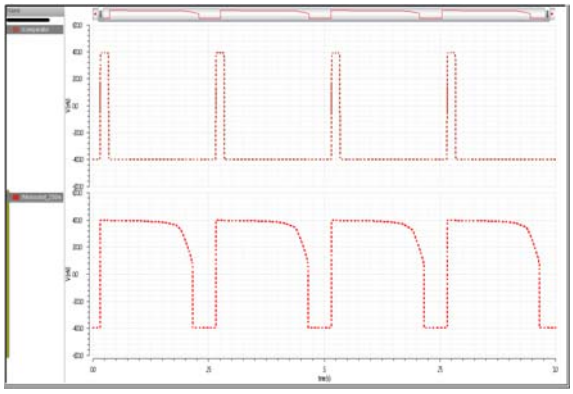

Figure-15. Simulation result of mono shot circuit with 200ms width in cadence environment.

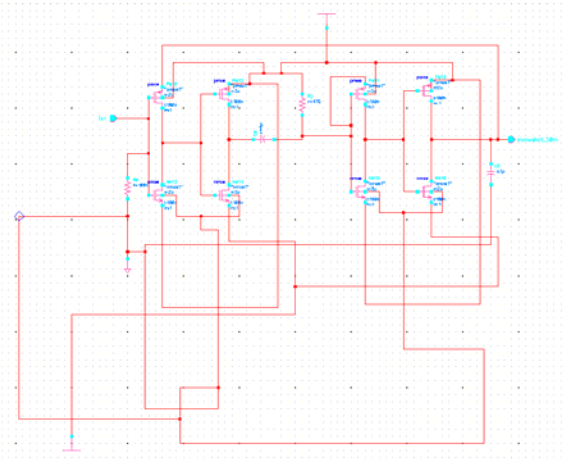

Figure-16. CMOS design of mono shot with 50ms width in cadence.

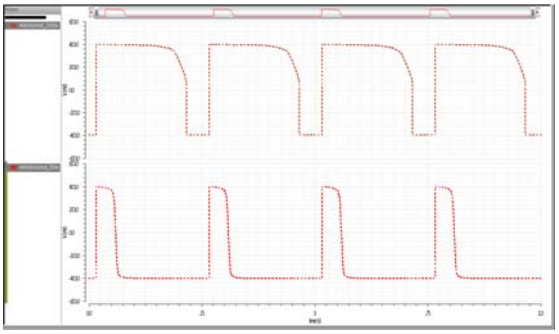

Figure-17. Simulation result of mono shot circuit with 50ms width in cadence environment.

3. MEASUREMENT RESULT

Detection of R- peak and shaping circuit is designed with low power and low voltage using body biasing technique. The overall circuit and simulation result is given in Figure-18 & Figure-19 This circuit is suitable for 40mv to 220mv voltage and 5Hz to 12.5 KHz frequency range. The operating voltage of circuit is + 400mv with 3.99µW power consumption. The measurement result of the circuit is given in Table-1.

Table-1. Measurement result of QRS detection circuit.

CIRCUIT	PARAMETER	MEASURED
Half wave rectifier	Ripple factor	2.11
	Form factor	2.337
	Peak Factor	3.814
	Efficiency	42.78%
	Offset voltage	11.468µV
Comparator	Offset Voltage	651.9897 µV
	Delay	3.298µs
	Rise time	96.34 µs
	Fall time	34.4 µs
Monoshot circuit	Offset voltage	184.492nV
	Delay	130.8µs
	Rise time	123µs
	Fall time	504.59862µs
R-Peak detection and shaping circuit	Operating voltage	±400mv
	Power consumption	3.997µW

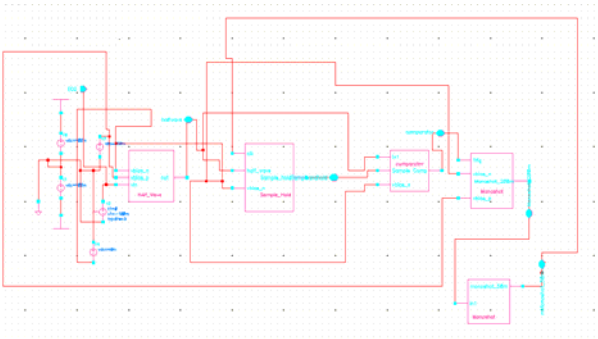

Figure-18. CMOS design of R peak detection and shaping circuit in cadence.

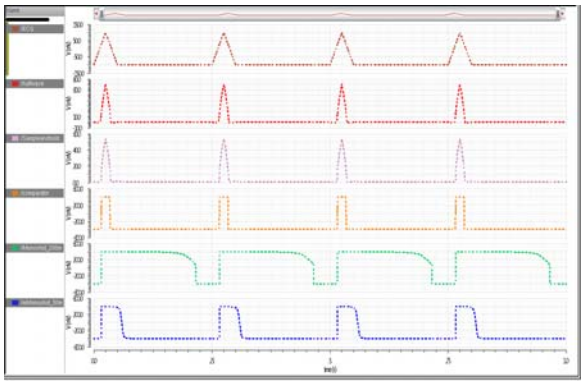

Figure-19. Simulation result of R-peak detection and shaping circuit in cadence environment.

4. CONCLUSIONS

A low power and low voltage approach for detection of R- peak and shaping is presented and it is simulated in 180nm Technology Cadence environment. It had low power and energy efficient as per measured result. This circuit is tested for the ECG frequency ranging from 40 beats/min to 200 beats/min. The proposed circuit can be integrated with the amplifier and filtering circuitry to make a system on chip for identifying Cardiac arrhythmias.

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