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A 0.5V LOW POWER SINGLE STAGE FOLDED CASCODE AMPLIFIER FOR BIO-SIGNALS

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ABSTRACT

Long term monitoring and measurement of bio signals requires new techniques that promise light weight devices consuming low power and are maintenance free. The basic block in processing analog signal happens to be operational trans-conductance amplifier (OTA) and the design of sub-threshold OTA for low voltage low frequency applications consuming less power is proposed. With an operating voltage of 0.5V the gain achieved is 58dB and CMRR of 88.5dB. The input referred noise is measured as 1.159µV and the power consumption has 620nW. The circuit was implemented in 0.18µm technology using cadence tool.

Keywords: bio-signals, OTA, sub threshold, low power.

1. INTRODUCTION

Low power designs using submicron devices are essentially required in battery operated medical electronic devices such as hearing aids, ambulatory monitoring devices, insulin pumps etc., the sub micrometer devices on a single IC is facilitated by scaling down the channel length in CMOS technology.

The design and implementation of bio medical Instrumentation amplifier is leading towards portability, for the devices monitoring the patient for long time low power consumption has become highly desirable. While retaining the precision and to reduce power consumption various methods have been proposed.

A typical low amplitude low frequency bio signal is ECG and this signal is processed through low pass filter having large time constant. Usually a filter with less than 300Hz cut off frequency is preferred. However the conventional OTA has the major limitation of limited linear range. The linearity can be improved by eight to ten times by employing various linearization techniques in which source degeneration and multitanh [1] principles are used.

By scaling down the device size several design challenges are to be met for conventional OTAs operating in saturation region to overcome the problem of linearity and output impedance. The OTA should have high output impedance as it is a voltage controlled current source (VCCS).

The operating region of transistor is maintained in subthreshold for low-power since 1970's [2] which is suitable for low operating voltage. The signal swing is enhanced in this region as the threshold voltage cannot reduce in the same proportion as that of the supply voltage. This region provides highest transconductance and less distortion [3]. However the bandwidth reduction and the large drain current mismatch are the main drawback of subthreshold operation which is attended by proper offset compensation technique. The bulk driving technique is introduced to increase the input swing with saturation region and also extended in subthreshold region [4-10] which limits the input resistance and the leakage currents. They are restricting the use of the bulk -driven technique in many places like switched-capacitor approach [11]. The bulk is also acting as a control terminal to set the quiescent current and it provides common-mode control and replacing the function of tail current generator [12-13].

The small bandwidth is significant drawback of subthreshold region devices which is compensated by scaling technique in less amount in the range of few kilohertz [14-15]. The subthreshold region is suitable for the wireless sensor networks, biomedical applications and the application where the speed is not in concern. Hence, in OTA and analog block design with operating voltage of 1V and few hundred nano amperes current the subthreshold techniques are becoming more popular [11], [15-18].

This paper is organized as follows Section II describes the design approach OTA which explains the principle operation of Operational Transconductance Amplifier. Section III reports the measurement results. The proposed work is concluded in Section IV.

2. SYSTEM DESIGN

High gain and low power can be achieved by the operating the devices in different region (subthreshold and active region) [19]. The cascoding connection is established by stacking source and drain of the MOSFET to increase the gain through high output impedance [20]. The self cascode design provides high gain with high impedance. For High speed application the folded cascode is suitable to provide high gain, large output signal swing and broad bandwidth. The PMOS input pair is used for folded cascode design as it has higher non-dominant poles and lower flicker noise [21-22].The design of sub-threshold OTA for low voltage low frequency low noise applications and consuming less power is proposed.

The schematic of a standard folded cascode OTA is given in Figure-1. The transistors M3 and M4 of OTA form current sources to differential pair transistors M5-M10. The large channel current of M3 and M4 transistors contribute a significant amount of noise in amplifier. This

noise is reduced by minimizing this current using proposed modified standard folded-cascode topology which is shown in Figure-2.

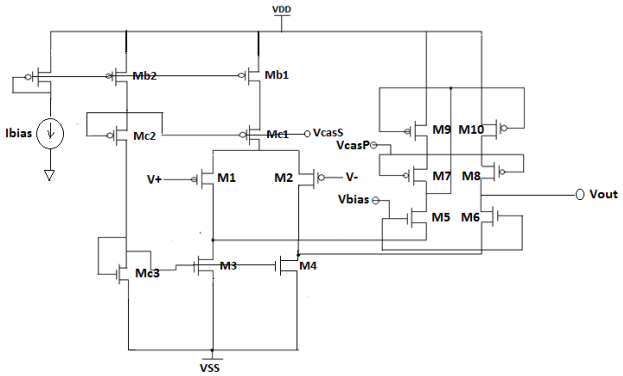

Figure-1. Schematic of standard folded cascode OTA.

The modified OTA is biased in such way that the currents of the individual transistors in the second folded branch M7-M12 of transistors are only a small fraction of the current of the input differential pair transistors M1 and M2. In this design the standard folded cascode OTA given in Figure-1 is modified by adding transistors M5 and M6 which is acting as a source degenerated current source to transistors M3 and M4. The difference of currents between M4 and M6 is maintained as a current in differential pair transistors M7-M8 using resistors R1 and R2. Such a way the noise is reduced by maintaining the current less in differential pair transistors M7-M12.

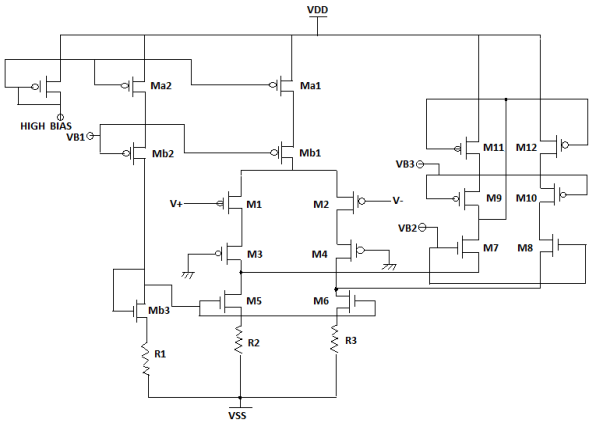

Figure-2. The modified OTA circuit.

2.2 Current scaling

In this design, the current in M7–M12 is scaled to approximately 1/3 of the current in M1 and M2 and this arrangement making the noise contribution is negligible. The total current and the total input-referred noise of the OTA is reduced simultaneously. Such severe current scaling is achieved carefully by setting the bias currents of M5 and M6 through the use of the current mirror circuit formed by Ma2, Mb2 and Mb3. All these transistors are operating in strong inversion to reduce the effect of threshold voltage variations except M1-M12. The combination of Mb3, M5 and M6 are arranged as source degenerated current mirrors. Resistors R1 and R2 are used to set the currents in M5 and M6 in such a way that the difference between the current in M3 and M5 and between the current in M4 and M6 is obtained the currents in M7-M8 respectively.

In order to save power in the bias circuit, the current scaling ratio is maintained strictly in every pair of transistors. Such current ratioing is achieved by making R1 and R2 resistor values are arranged 50 times the value of resistor R3.

Table-1. Operating points for transistors in the OTA with I = 1.24u A.

Devices	W(um)/L(nm)	I_D	Operating region
$M_{1,2}$	20/180	393.4nA	Sub-threshold region
$M_{3,4}$	50/180	393.4nA	Sub-threshold region
$M_{5,6}$	10.02/180	514.1nA	Sub-threshold region
$M_{7,8}$	1/180	120nA	Sub-threshold region
$M_{9,10}$	1/180	120nA	Sub-threshold region
$M_{11,12}$	1/180	120nA	Sub-threshold region

2.1 Transconductance (Gm)

The transconductance of the OTA needs to be maximal for a given current level. In the folded-cascode OTA the current in M5 and M6 is comparable to the current in M1 and M2.Thus, the impedance looking into the sources of M5 and M6 is much smaller than the impedance looking into the drains of M1- M4. The transcondutance relationship of transistors is given below in equation (1) and (2).

$$1/Gs5 < 1/Gd1\ or 1/Gd4 \quad (1)$$

$$1/Gs5\ or 1/Gs6 < 1/Gd7\ or 1/Gd8 \quad (2)$$

Because of the current divider between drain of M5 and M6 to Source of M3 and M4 a small fraction of current flows in the transistor M7-M8. Due to this small fraction of current the impedance looking in to the second folded branch is becoming high. So the overall transconductance of the folded-cascoded OTA is almost equal to the transconductance of the M1-M2 transistors.

2.3 Source degenerated resistors

The basic Drain to source current equation is $I_D = u\ C_{ox}(W/L)\ (V_{in}-V_{th})^2$. So I_D depends on overdrive voltage $(V_{in}-V_{th})^2$ because of square law dependency the OTA produces non linearity. This non linearity effect the overall gain of the OTA.

$$A_V = -g_{m1}R_{d7} \quad (3)$$

$$g_{m1} = \delta I_D / \delta V_{in} \quad (4)$$

The brilliant solution for nonlinearity is Source degeneration. Gm is the effective factor in the gain calculation. The source degeneration arrangement reduces non-linearity and it makes transcondutance stronger which is represented as G_M. Now

$$A_V = -G_m.R_{d7} \quad (5)$$

$$G_M = \delta I_D / \delta V_{in} \quad (6)$$

Where

$$I_D = g_{m1}V_{gs} \quad (7)$$

$$I_D = \delta g_{m1}\ \delta V_{gs} \quad (8)$$

Substitute above equation in equation

$$G_M = g_{m1} * (\delta V_{gs} / \delta V_{in}) \quad (9)$$

Where $V_{gs} = V_G - V_S$

$V_{gs} = V_{in} - I_D R_{S5}$

Differentiating above equation with respect to V_{in}

$$\delta V_{gs} / \delta V_{in} = 1 - R_{S5}\ (\delta I_D / \delta V_{in})$$
$$G_M = g_{m1}[1 - R_{S5}(\delta I_D / \delta V_{in}]$$
$$= g_{m1}\ [1 - R_{S5}\ G_M]$$

$$G_M = g_{m1} / (1 + R_{S5}\ g_{m1}) \quad (10)$$

Gain $A_V = G_M\ R_{d7}$

$$A_V = -g_{m1} / (1 + R_{S5}\ g_{m1}) * R_d \quad (11)$$

Now there is no effect on gain with non linearity.

2.4 Noise reduction with degeneration circuit

In the standard folded-cascode topology the current sources formed by transistors and they contribute large amount of noise due to their large channel currents. In the proposed design, the current-source transistors are replaced with source degenerated which is formed by M5 and M6 and degeneration resistors R1 and R2. The noise from the source-degenerated current source is mainly from the resistors and can be made much smaller with an appropriate choice of degeneration resistance compare with the noise contributions from MOS transistors operating at the same current level,. Another benefit of using source-degenerated current sources is that the noise from resistors is mainly thermal noise when NMOS current sources contribute a large amount of 1/f noise unless they are made with very large area. As a result, the 1/f noise in our amplifier is mainly from the input differential pair. Therefore, the input-differential pair is made with large-area pMOS transistors, which have lower noise than similarly-sized nMOS transistors in most CMOS processes.

To achieve low input-referred noise, it is important that the transconductance of the OTA be maximized for a given total current. The maximum transconductance of the standard folded-cascode OTA can be achieved by increasing the transconductance of one of the transistors in the input-differential pair. It is possible to operate M1 and M2 in the subthreshold region where a transistor's gm is maximized for a given current level. Therefore, M1 and M2 need to have large W/L ratios. The Current Source Transistor, Source degenerated current source and OTA with degeneration resistors are shown in Figure-3.a, b and c.

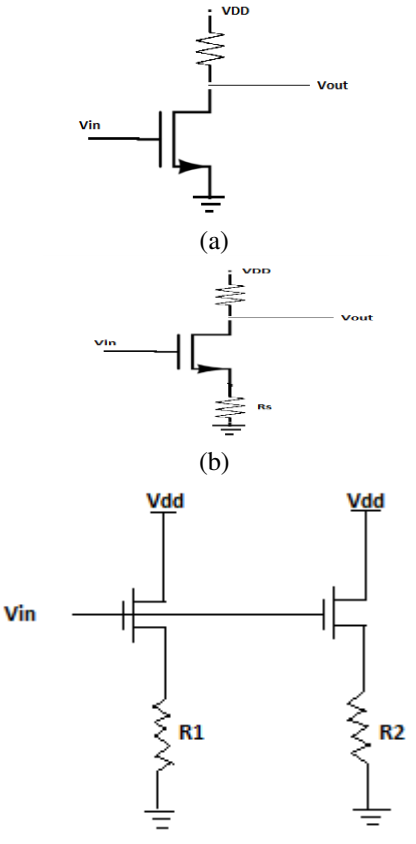

Figure-3. a) Current source transistor. b) Source degenerated current sources. C) OTA with degeneration resistors.

The required Expressions for the design of OTA:

a) The output current of OTA is $I_o = gm(v1 - v2)$

b) The gm of OTA expressed as $g_m = \sqrt{(2\mu C_{ox}(W/L)I_{bias})}$

c) Gain $= gm * rd = \frac{gm1}{Gd10+gd12}$

d) Gain Bandwidth $= \frac{gm1}{CL}$

The CMOS design of modified folded cascode OTA in cadence environment is given in Figure-4.

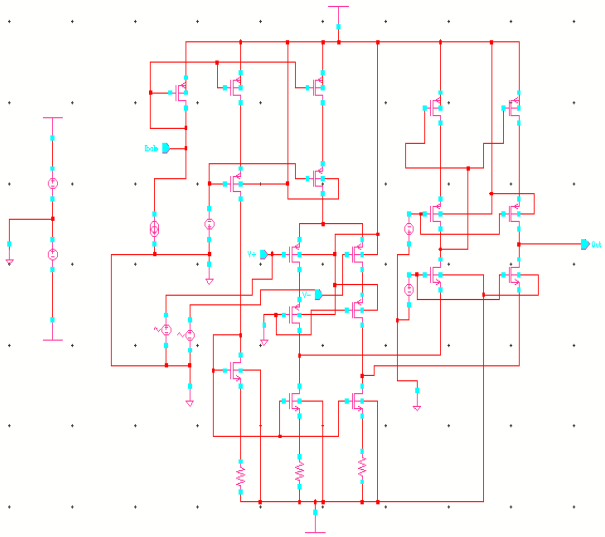

Figure-4. CMOS design of modified folded cascode OTA in cadence environment.

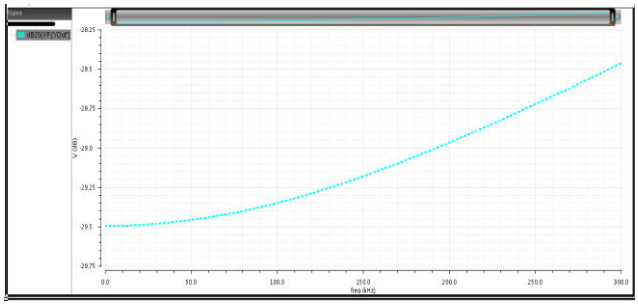

Figure-5. Common mode gain of OTA.

The Common mode gain of OTA is shown in Figure-5. It is plotted during 0-300KHz.

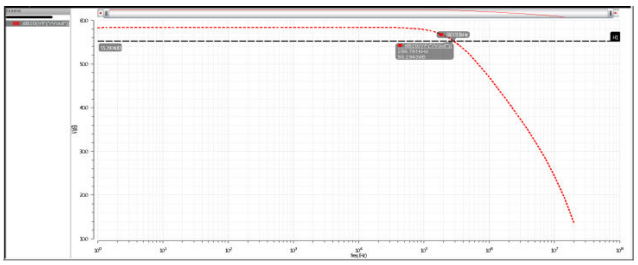

Figure-6. Differential gain with C=100fF and BW = 256.761 KHz of OTA.

The differential gain of OTA is given in figure-6 with 100fF of Capacitance, 256.76 KHz of Bandwidth and 55.254db gain.

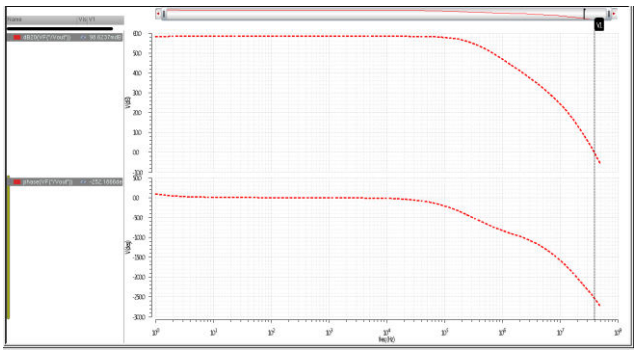

Figure-7. Gain-phase plot of OTA.

The gain phase plot of OTA is given in Figure-7.It is obtained gain of 58db and 3600 phase.

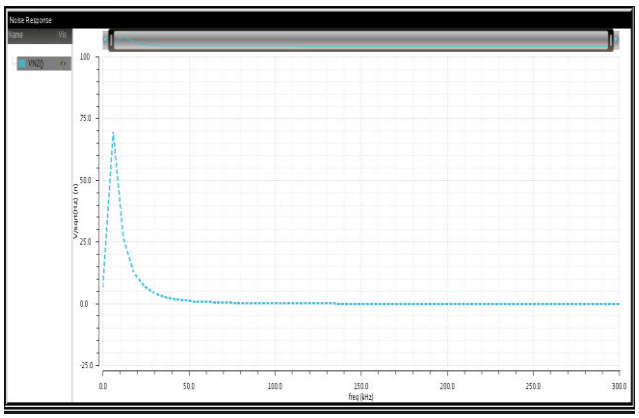

Figure-8. Input noise of OTA.

The input noise of OTA is plotted in Figure-8. The input referred noise is 1.159u Vrms.

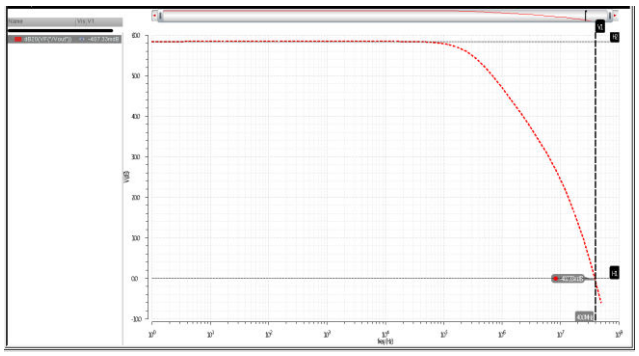

Figure-9. Unity gain bandwidth of OTA.

The unity gain bandwidth is 18.04MHz which is pointed in above Figure-9.

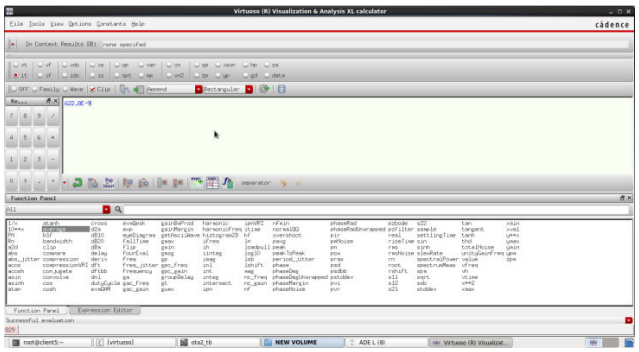

Figure-10. Power analysis of OTA.

The power obtained is 620nW which is calculated using Cadence calculator tool shown in Figure-10.

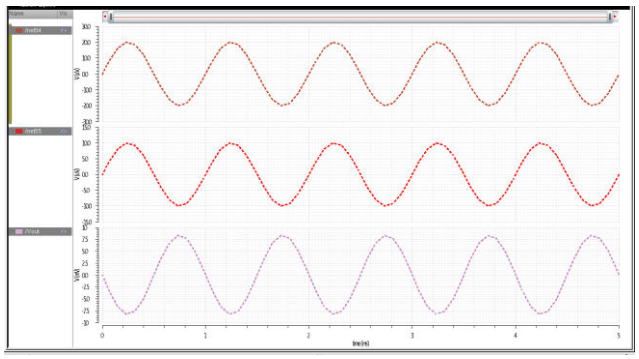

Figure-11. Transient analysis of OTA.

The transient analysis of OTA is plotted for V+,V- and OTA output shown in Figure-11.

3. MEASUREMENT RESULT

A Low Power Single stage folded cascode amplifier for bio-signal is designed with 500mv operating voltage, driving with total current of 1.24µA and 620nW power consumption. The obtained gain of OTA is 58db with 0Hz-282.16 KHz 3dB-bandwidth and 18.04MHz of unity gain bandwidth. The calculated CMRR and PSRR are 89db and 95db respectively. The measurement result of the circuit is given in Table-2.

Table-2. The measured performance characteristics of OTA with 0.5v power supply.

Parameter	Measured
Supply Voltage	500mV
Total Current	1.24uA
Gain	58dB
3dB-Bandwidth	0Hz-282.16KHz
Unity Gain Bandwidth	18.04MHz
Input referred Noise	1.159u V_{rms}
CMRR	89dB
PSRR	95dB
Power Dissipation	620nW

4. CONCLUSIONS

A single stage cascode amplifier has been designed with an operating voltage of 0.5V to achieve low power and low noise. The design is simulated using Cadence tool in 180nm Technology. Current scaling technique has been utilized to which resulted in achieving low input referred noise and low power. The measured results show that the circuit is consuming very low power and less noise which is suitable for bio medical applications.

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