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A SURVEY ON FFT/IFFT PROCESSOR FOR HIGH SPEED WIRELESS COMMUNICATION SYSTEM

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ABSTRACT

The demand for increased channel capacity in mobile and wireless communication has been rapidly increasing due to multi fold increase in demands of multimedia services and mobile data. In the present scenario, high data rate are offered by WLAN, WiMax and LTE/ LTE-Advanced (LTE-A). Developing a wireless system for more spectral efficiency under varying channel condition is a key challenge to provide high bit rates with limited spectrum. MIMO system with OFDM gives higher gain by using the direct and the reflected signals, thus facilitating the transmission at high data rate. Efficient implementation of MIMO-OFDM communication system is based on IFFT/FFT algorithm. There is several variations in the FFT architecture, which are being used in MIMO-OFDM transceivers and are discussed in this paper. In this work, it is seen that the proposed mixed radix algorithm uses only less number of logic gates, adders and counters. It is been evident that FFT architecture can provide higher throughput rate with minimal hardware cost by adding the features of SDF and MDC pipelined architecture.

Keyword: FFT/IFFT processor, MIMO-OFDM, SDF, MDC.

1. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is a popular scheme for high data rate wireless transmission. OFDM may combine with antenna array at the transmitter and receiver to improve the system capacity on frequency selective and time variant channel, resulting in a Multiple Input Multiple Output (MIMO) configuration. MIMO wireless technology is capable of increase the capacity of a particular channel while still obeying Shannon's law. By increasing the quantity of receive and transmit antennas it is able to linearly increase the throughput of the channel with eachpair of antennas added to the system. This makes MIMO wireless technology one of the most remarkable wireless techniques to be employed in recent years. As spectral bandwidth is becoming an ever more vital commodity for radio communications systems, techniques are necessary to use the available bandwidth more efficiently. MIMO wireless technology is one of these techniques. OFDM has been adopted for different transmission systems such as Wireless Fidelity (WIFI), Digital Video Broadcasting (DVB), and Worldwide Interoperability for Microwave Access (WIMAX) and Long Term Evolution (LTE).

MIMO-OFDM has been given specific importance for the growth of this technology in VLSI domain. Even though MIMO-OFDM systems can achieve better reliability and higher capacity, the power consumption also increases because of the added complexity for the multi-stream processing. Therefore, low power becomes a main target in designing MIMO-OFDM devices, especially for portable applications. In the MIMO-OFDM transceiver, the fast Fourier transform (FFT) processor is a key part with high computational complexity. The power consumption of the FFT processor grows proportionally to the stream number, which occupies a huge percentage of system power budget.

The advantages of FFT Implementation for OFDM techniques are 1.Complexity of implementing N separate modulators/demodulators is prohibitive. 2. The IFFT shifts modulated symbols to desired subcarriers. 3. MCM effectively implemented using IFFT at transmitter and FFT at receiver. 4. A cyclic prefix is inserted in the data to remove ISI between blocks and make the linear convolution with the channel circular. 5. The received symbol is just a scaled version of the transmitted symbol. Also, the Implementation challenges in OFDM method such as 1. Interference between sub channels mitigated by minimizing the number of sub channels and using pulse shapes robust to timing errors. 2. Timing and frequency offsets cause sub channels to interfere with each other. 3. OFDM/DMT consists of multiple sinusoids summed together, can have a enormous peak to-average power ratio (PAPR), which leads to amplifier inefficiencies. 4. PAPR compensated through clipping or coding.

This paper structured as follows: the section 2 deals with Fast Fourier Transform basics, Section 3 which describes about MIMO - OFDM concept, Section 4 discuss on FFT Processor for MIMO –OFDM techniques, and Section 5 gives Conclusion of this paper.

2. FAST FOURIER TRANSFORM

The FFT algorithm was first presented by Cooley and Tukey in [4] with an aim to compute Discrete Fourier Transform (DFT) with significant reduction in number of computations. In fact, reduced computations due to FFT algorithm helped to decrease power consumption, area and increase system throughput. Direct computation of N-point DFT would require N^2 - N complex additions and N^2 complex multiplication operations according to equation given by,

The DFT of size N is defined by

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \quad 0 \le k \le N-1 \qquad (1)$$

Where, $W_N = e^{-j2\pi/N}$
Similarly, the iDFT becomes

$$X(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k)W_N^{-nk} \quad 0 \le n \le N-1 \qquad (2)$$

However, using FFT algorithm total number of additions and multiplications reduces to $N(\log_2 N)$ and $\frac{N}{2}\log_2 N$respectively. An N-point FFT equation is given by,

$$X(k) = \sum_{n=0}^{\left(\frac{N}{2}\right)-1} x(2n)\, e^{-\left(\frac{j2\pi nk}{\frac{N}{2}}\right)} + W_N^k \sum_{n=0}^{\left(\frac{N}{2}\right)-1} x(2n+1)\, e^{-\left(\frac{j2\pi nk}{\frac{N}{2}}\right)} \qquad (3)$$

Where $W_N^k = e^{-j2\pi k/N}$, k=0,1,2,… N-1.

Decimation In Time (DIT) FFT algorithm is found to provide better signal-to-noise ratio in comparison with Decimation In Frequency (DIF) FFT for a finite word length according to Tran-Thong *et al*. in [5]

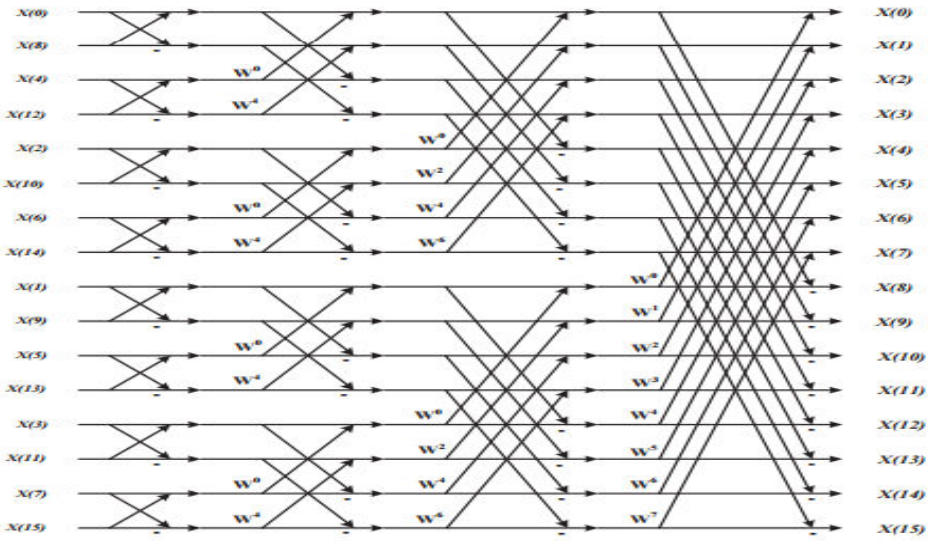

Figure-1. Radix-2 DIT FFT butterfly diagram.

Equation 3 can be depicted as a DIT butterfly diagram for 16-point FFT as shown in Figure-1 where *x(n)*, *X(k)* are N-Point complex inputs and outputs respectively. Inputs *x(n)* are in bit reversed order and outputs *X(k)* are in natural order. The butterfly computation with upper half of data samples is symmetric with lower half till the last stage. In the last stage, butterfly computation merges data samples from lower half and upper half. Such a property of DIT FFT is the basis for address generation scheme and input data storage in data memory of FFT processor. For an N-point FFT there are $\log_2(N)$number of stages and each stage contains $\frac{N}{2}$ butterfly operation.

3. MIMO - OFDM

MIMO is an antenna technology for wireless communications in which more than one antenna are used at bothtransmitter and receiver. The antennas at each end of the communications circuit are combined to reduce errors and optimize data speed. MIMO is one of several forms of smart antenna technology, the others being MISO (multiple inputs, single output) and SIMO (single input, multiple outputs).

For example a 4*4 MIMO will have 4 antennas to transmit signals (from base station) and 4 antennas to receive signals (mobile terminal).This is also called as downlink MIMO. General Figure of a MIMO antenna system is as given below Figure-2.

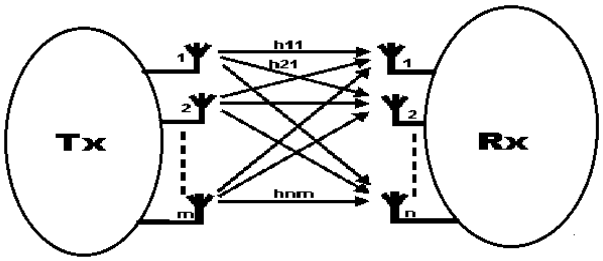

Figure-2. Downlink MIMO.

It is found that the signal can travel many paths between a transmitter and a receiver. Additionally by moving the antennas even a little distance the paths used will be changed. The variety of paths available occurs as a result of the number of objects that emerge to the side or even in the direct path between the transmitter and receiver. Previously these multiple paths only perform to introduce interference. By using MIMO, these additional paths can be used to advantage. They can be used to provide additional strength to the radio link by improving

the signal to noise ratio, or by increasing the link data capacity [8].

In uplink, MU-MIMO can be used. Multiple user terminals may be transmitted simultaneously on the same resource block. This is also called as spatial domain multiple accesses (SDMA). The method requires only one transmit antenna at user equipment (UE) side which is a big plus. The UEs sharing the same resource block have to apply mutually orthogonal pilot patterns

Orthogonal Frequency-Division Multiplexing (OFDM) has emerged as a successful air-communication. For the case of wired environments, OFDM method is also known as Asymmetric Digital Subscriber Line (ADSL) and Discrete Multi-Tone (DMT) transmissions, High-bit-rate Digital Subscriber Line (HDSL), and Very-high-speed Digital Subscriber Line (VDSL).OFDM has a few key advantages over other commonly used wireless access techniques, such as Time- Access (CDMA). The main advantage of OFDM is the fact that the radio channel is divided into many narrow band, low-rate, frequency-non-selective sub channels or subcarriers, so that several symbols can be transmitted in parallel, while maintaining a high spectral efficiency.

Each subcarrier may deliver information for a different user, resulting in a simple multiple-access method known as Orthogonal Frequency-Division Multiple Access (OFDMA). This enables different media such as speech, text, video, graphics, or other data to be transmitted within the same radio link, depending on the particular types of services and their Quality-of-Service (QoS) requirements. OFDM uses IFFT at transmitter and FFT in receiver.

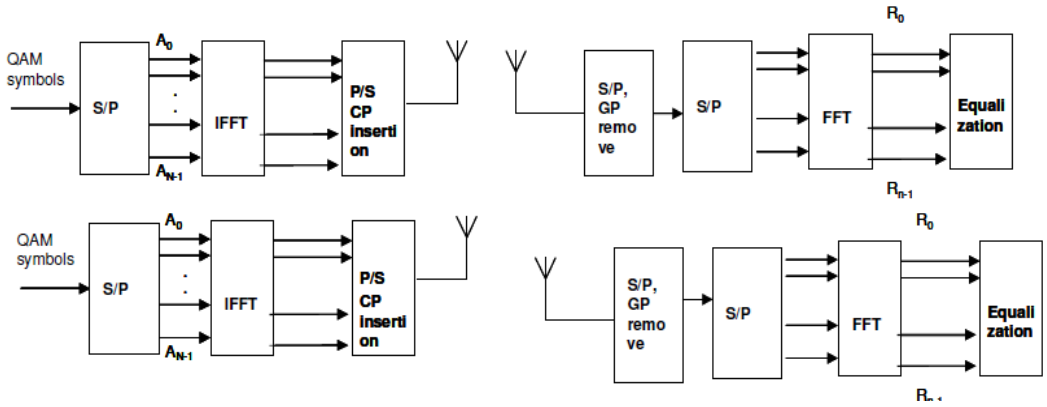

Figure-3. MIMO-OFDM transceiver.

The transceiver structure of MIMO-OFDM is shown in Figure-3. The combination MIMO-OFDM is useful since OFDM enables improved support of more antennas and larger bandwidths since it simplifies equalization significantly in MIMO systems. By adopting Multiple-Input Multiple-Output (MIMO) and Orthogonal Frequency-Division Multiplexing (OFDM) technologies, indoor wireless systems could reach data rates up to several hundreds of Mbits/s and make spectral efficiencies of several tens of bits/Hz/s, which are unachievable for conventional single-input single-output systems [8]. The enhancements of data rate and spectral efficiency come from the fact that MIMO and OFDM schemes are indeed parallel transmission technologies in the space and frequency domains, respectively. MIMO-OFDM when generated OFDM signal is transmitted through a number of antennas in order to achieve diversity or to gain higher transmission rate then it is known as MIMO-OFDM. Combining OFDM with multiple input multiple output (MIMO) technique increases spectral efficiency to attain throughput of 1 Gbit/sec and beyond, and improves link reliability. Thus, OFDM removes ISI; MIMO gives diversity/multiplexing benefits. These systems adapt across space, time, and frequency.

4. FFT PROCESSOR FOR MIMO-OFDM

A dynamic voltage and frequency scaling (DVFS) FFT processor for MIMO-OFDM applications has been explained in this paper [1]. Both voltage and frequency can be scaled to optimal values in real time according to the processing needs in the dynamic voltage and frequency scaling (DVFS) technique. A multimode multipath delay- feedback (MMDF) architecture has been proposed for the FFT processor, which can process 1–8-stream 256-point FFTs or a high-speed 256-point FFT in two processing domains at minimum clock frequency for DVFS operations. A parallelized radix-24 FFT algorithm and scheduling techniques are employed to minimize the number of complex multipliers and hence to save the power consumption and hardware cost. High throughput rate up to 8-stream 300-Msample/s or 2.4-Gsample/s computations was achieved by using parallel-8 data-paths. A 2048 fast Fourier transform (FFT) processor gives high throughput rate by applying the eight-data-path pipelined approach together with a hardware reduction method and a multi-data scaling scheme for wireless personal area network applications. The hardware costs, area and power consumption, increase due to multiple data paths and increased word length along stages. To rectify these, a simplification method to reduce the hardware cost in multiplication units of the multiple-path FFT approach

was proposed. A multi-data scaling scheme in which mantissa and exponent part are handled in Separate paths to reduce word lengths while preserving the SNR is also presented. The mantissa data are operated by eight data paths, and the exponent is operated by one data path [11].
A multimode FFT processor for wireless local area network (WLAN), wireless personal area network (WPAN) and wireless metropolitan area network (WMAN) applications has been presented in this [12] paper. Using the proposed flexible-radix-configuration multipath-delay-feedback (FRCMDF) architecture, variable length/multiple-stream FFTs capable of achieving a high throughput can be performed in a hardware-efficient manner. In this paper, a dual-optimized multipath multiplication scheme is proposed in order to improve the area and energy efficiency associated with the multiple-path multiplier units for high-throughput FFT designs. The FFT processor supports high-throughput 128/256/512-point FFTs for WPAN, 1- to 4-stream 64/128-point FFTs for WLAN, and 128- to 1024-point FFTs for WMAN is proposed.

FIFO register and complex multipliers dominate the area and power consumption in FFT processor at each stage. This paper [9] proposes an 8-path feedback structure (8PFB) for the FFT processor to get high throughput, low hardware cost and low power consumption, which is, implemented for OFDM-based Ultra Wideband (UWB) communication systems. The 8PFB structure can halve the register reverse frequency in the MRMDF structure. The combination of two 64-points and one 128-point FFT has been achieved through 8×8×2 mixed radix arithmetic. The 8-path feedback parallel structure has enabled a 1GS/s throughput at a comparatively low clock frequency of 125MHz, so it saves a large amount of power dissipation without the expense of the signal processing ability. The modified shift-add algorithm used here can remove complex multipliers in the FFT processor.

In this paper [2], a modified radix-2^5 algorithm for 512-point Fast Fourier Transform computation and high speed eight-parallel data-path architecture for multi-gigabit wireless personal area network (WPAN) systems was presented. The FFT processor can provide a high data throughput and low hardware complexity by using eight-parallel data-path and multi-path delay feedback (MDF) structure. It reduces the number of complex multiplications by the use of Booth multiplier and twiddle factor look-up tables. Multi-path delay-feedback (MDF) architecture based on multi-path parallel structure is used for this system because in a gigabit WPAN system, the symbol rate is required up to 2.5 GS/s.

In this [3] paper presents the radix-2^kfeed-forward (MDC) FFT architectures. In feed-forward architectures, radix-2^k can be used for any number of parallel samples which is a power of two. Furthermore, both Decimation in Time (DIT) and Decimation in Frequency (DIF) decompositions can be used using this architecture. Here, proposed designs include radix-2^2, radix-2^3 and radix-2^4 architectures.

A variable length FFT processor for 4×4 MIMO-OFDM systems with 256-point FFT algorithm has been discussed into this paper [6]. Here radix-4^2 algorithm is to deal with 4 data sequences simultaneously and a butterfly sharing technique to increase the hardware utilization. The operating time of the radix-r butterfly is 1/r, and the butterfly is idle for the rest of cycles. The FFT architecture that uses multiple data paths and feedback memory achieve high data throughput with less hardware complexity. Here the memory allocation method has been modified and proposed a Butterfly and Multiplier Sharing (BMS) architecture.

A design of an fast Fourier transform (FFT)/ inverse FFT (IFFT) processor for the applications in a MIMO-OFDM based IEEE 802.11n wireless local area network baseband processor has been presented in this paper [7]. The unfolding mixed-radix multipath delay feedback (MDF) FFT architecture is proposed to efficiently deal with 1–4 simultaneous data sequences. Power consumption can be saved by using higher radix FFT algorithm thus a three-step radix-8 FFT algorithm is chosen to save complex multiplications. The mixed-radix multipath delay feedback (MRMDF) FFT architecture can achieve higher throughput rate with minimal hardware cost by combining the features of MDC and SDF. The hardware costs of memory and complex multiplier were saved by adopting delay feedback and data scheduling approaches.

In mixed radix FFT processor for MIMO-OFDM in wireless communication employing the parametric nature of this core, the OFDM block is synthesized on one of Xilinx's Virtex-II Pro FPGAs with different configurations. The results ofthis logic synthesis for 64 point FFT based MIMO- OFDM using Radix-2, Radix-4, split Radix and mixed radix 4/2 are discussed in below Table-1.

Table-1. Comparison of 64-point FFT algorithm based on CLB slices, utilization factor and power.

64 point FFT	CLB slices/7680	Utilization factor	Power in mW
Radix-2 FFT	851	11.1%	2572.45
Radix-4 FFT	765	9.96%	1962.53
Split Radix FFT	835	10.8%	1582.61
Mixed Radix (4/2 FFT)	750	9.77%	1376.28

The 64-point Mixed Radix FFT based MIMO-OFDM design was found to have a good balance between its hardware requirements and its performance and therefore suitable for use in MIMO-OFDM systems [10].

5. CONCLUSIONS

From the analysis, it is evident that mixed radix FFT architecture has promising feature for the implementation of FFT/IFFT processor in MIMO-OFDM transceiver. For better performance in FPGA implementation can be obtained using SDF and MDC FFT algorithm. From this work, we can summarize the mixed radix algorithm offers greater advantages in terms of reduced the number of multipliers and power consumption level. In future Mixed radix FFT/IFFT core can be designed for effectively implement into the wireless communication system.

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