



A MULTI-OBJECTIVE OPTIMIZATION METHODOLOGY APPLIED TO THE LOW-POWER CMOS OPERATIONAL AMPLIFIERS

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ABSTRACT

This paper presents a novel design methodology for optimizing the performance of CMOS op-amp topologies by using Multi-Objective optimization Methodology. This methodology is used to find the optimal transistor dimensions in order to acquire operational amplifier performances for analog and mixed signal circuit applications. The goal is to automatically determine the device size in order to meet the given performance specifications while minimizing the design time, Area, power and cost function. This strongly suggests that the approach is capable of determining the globally optimal solutions to the problem. Accuracy of performance prediction in the sizing program (implemented in MATLAB) is maintained. These operational amplifiers were simulated by using cadence virtuoso spectre circuit simulator in 0.18 μ m CMOS technology with power supply ± 1.8 v. In this paper six performances are considered i.e., Open loop Gain(Av), Unity gain bandwidth(UGB), Phase Margin (PM), Slew rate(SR), Area(A) and Power consumption(Pc). Finally a good agreement is observed between the program optimization and electric simulation.

Keywords: CMOS operational amplifiers, transistor dimensions, multi-objective optimization methodology.

1. INTRODUCTION

The design automation of analog CMOS integrated circuits (ICs) is a demanding task in microelectronics industry, because of the crescent necessity for low-power design and reduced time-to-market. Nowadays, most analog sizing designs are done manually - with some aid of simulation tools and equation-based models - and the quality of the resulting circuit is dependent on the expertise of the designer. A system-on-chip (SOC) design has analog and digital parts, each one designed with different methodologies and tools. The analog design time must be compatible with the highly automated digital design time, which employs advanced design automation tools.

The automation of fundamental analog design steps is extremely relevant for the success of a project. The transistor sizing stage is, perhaps, the most difficult to automate due to the large and highly non-linear design space. This stage is time consuming and might induce significant delays relating to time-to-marketing. Nowadays, there is no analog circuit sizing tools fully automatic searching the entire design space and taking advantage of state-of-the-art fabrication technologies. Also, layout generation of analog blocks is error-prone and time demanding.

An analog integrated circuit design is composed by transistors with different gate widths and lengths, requiring complex techniques of layout generation to minimize variations and improve matching. A traditional analog design methodology includes poor automated calculations with electrical models based on first order equations, several iterations of spice simulations and analysis, and full-custom layout generation. The experience of the designer is fundamental for the quality of the resulting design and for the amount of time spent. In general, the entire design space is rarely explored, mainly

in transistor weak and moderate inversion regions, which are the most appropriated for power-constrained applications.

The design space for the automatic synthesis of analog CMOS integrated circuits is highly nonlinear. There are tens of free variables in the design of a typical analog integrated block (such as an two-stage op-amp, folded cascode op-amp and telescopic op-amp), related to gate dimensions (W and L), bias currents or inversion levels. As the relation between transistor sizes and circuit specifications (design objectives) is sometimes conflicting, the problem of finding an optimum solution point is difficult to be exactly solvable. Some works have been done in this theme describing the development of tools for analog design automation (ADA), using different meta-heuristics and algorithms (Liu *et al.*, 2009) (Vytyaz *et al.*, 2009). The goal is always the automation of time-consuming tasks and complex searches in highly non-linear design. Analog CMOS Design Automation Methodologies for Low-Power Applications basically all of them can be categorized as equation-based or simulation-based automatic designs.

In the equation-based design strategy, analytical equations are used for modelling device electrical characteristics, such as drain current, inversion level or small-signal parameters. These models are often simplified or manipulated in order to fit certain limitations imposed by optimization heuristics. The simulation-based strategy is based on results of electrical simulations of the circuit to extract device parameters and design characteristics.

The simulation can be automated and performed several times until reaching the design objective. Both strategies have demonstrated limitations but, together with powerful optimization meta-heuristics, they are very promising for finding near-optimum design solutions in an acceptable computational time. The goal of this text is to



compare two different techniques for automatic sizing of analog integrated amplifiers. The first one exploits the analytical gm/ID methodology, in which the transconductance (gm) to drain current (ID) ratio of the transistors are free variables and gate width and length are defined in terms of the technology independent gm/ID versus ID/(W/L) curve; and the second one is numeric, based on an automated sequence of simulations of a spice net list with W and L as free variables. We employed multi-objective optimization Algorithms (MOGA) as optimization heuristics. Both methodologies were implemented for sizing a power-constrained design of a two-stage op-amp, folded cascode op-amp and telescopic operational amplifier.

2. OP-AMP DESIGN OPTIMIZATION

Operational Amplifiers are the backbone for many analog circuit designs. Op-Amps are one of the basic and important circuits which have a wide application in several analog circuit such as switched capacitor filters, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp. Larger the bandwidth and gain, higher the speed and accuracy of the amplifier Op-amp are a critical element in analog sampled data circuit, such as SC filters, modulators.

2.1 Two-stage op-amp

It consists of two stages in which first is differential stage and second is the gain stage. Output buffer is also used. In CMOS Op-Amp compensation network is used to which a feedback network is applied around the amplifier in virtually all Op-Amp applications. Therefore, to obtain stable performance the amplifier must be compensated. There are many types of compensation network used but we used miller compensation.

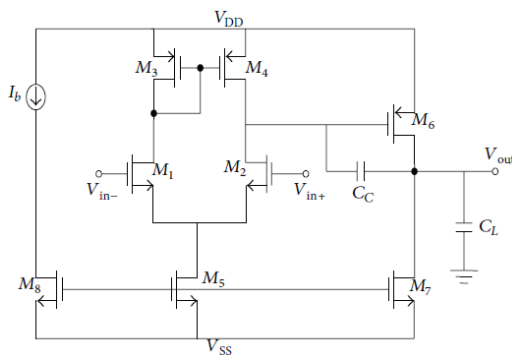


Figure-1. Two stage op-amp.

a) Open loop DC gain

The open – loop voltage gain is

$$A_v = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds7} + g_{ds6}}$$

b) Unity - Gain bandwidth

The Unity gain bandwidth is given by the expression

$$GBW = \frac{g_{m1}}{C_c}$$

Where C_c is compensation capacitor

c) Phase margin

The phase margin is given by the equation

$$PM = \pm 180 - \tan^{-1}\left(\frac{GBW}{P_1}\right) - \tan^{-1}\left(\frac{GBW}{P_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right)$$

d) Slew rate

The slew rate is given by

$$SR = \frac{I_5}{C_c}$$

e) Power consumption

The power consumption is given by

$$P = (V_{DD} - V_{ss})(I_5 + 2I_7)$$

f) Area

$$\text{Area} = \sum_{i=1}^{11} W_i \cdot L_i$$

2.2 Folded cascode Op-amp

We opt for a “folded cascode” opamp due to its large gain and high bandwidth performances the input stage provides the gain of the operational amplifier. Due to the greater mobility of NMOS device, PMOS input differential pair presents a lower transconductance than carrier a NMOS pair. Thus, NMOS transistor has been chosen to ensure the largest gain required.

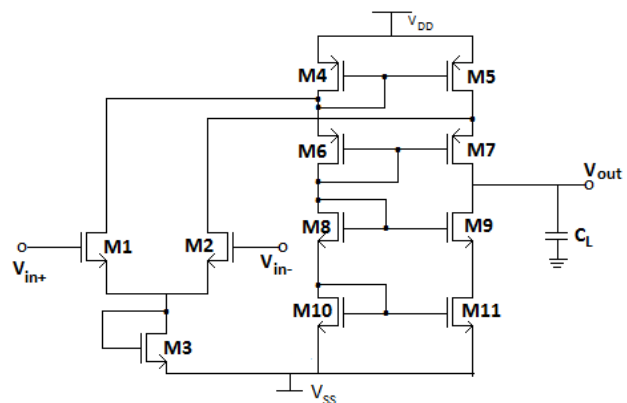


Figure-2. Folded-cascode op-amp using NMOS input device.

**(a) Gain**

the open-loop voltage gain is given by

$$A_v = g_{m1} R_{out} \left[\frac{2+k}{2+2k} \right]$$

$$R_{out} = g_{m9} r_{ds9} r_{ds4} // [g_{m7} r_{ds7} (r_{ds2} // r_{ds5})]$$

$$R_9 = g_{m9} r_{ds2} r_{ds11}$$

$$k = \frac{R_9 (g_{ds2} + g_{ds5})}{g_{m7} r_{ds7}}$$

Where $g(g_{m7} \text{ } g_{m9})$ is the transconductance of transistors ($M7$ and $M9$) and g_{ds} is the output conductance and r_{ds} is the resistance of the corresponding transistor.

(b) Unit gain bandwidth

The unity-gain bandwidth is given by the expression

$$GBW = \frac{gm1}{C_L}$$

Where C_L is the Load capacitance.

(c) Phase margin The phase margin of operational amplifier depends on the sum of phase shifts, at the unity-gain frequency, contributed by the non-dominant poles ($p1$, $p2$ and $p3$)

$$PM = \pm 180 - \tan^{-1} \left(\frac{GBW}{p1} \right) - \tan^{-1} \left(\frac{GBW}{p2} \right) - \tan^{-1} \left(\frac{GBW}{p3} \right)$$

$$\text{Where } P_1 = \frac{gm6}{c_a}, P_2 = \frac{gm7}{c_b} \text{ and } P_3 = \frac{gm10}{c_6}$$

(d) Slew rate For this operational amplifier, the slew rate is given by

$$SR = \frac{I_3}{C_c}$$

Where I_3 is the current that flows through transistor $M3$.

(e) Power consumption

the power consumption is given by

$$P = (V_{DD} - V_{SS})(I_3 + I_9 + I_{10})$$

(f) Area The area A of the operational amplifier is given by the sum of transistors and capacitors areas:

$$\text{Area} = \sum_{i=1}^{11} W_i \cdot L_i$$

2.3 Telescopic cascode Op-amp

Telescopic cascode op-amp, typically has higher frequency capability and consumes less power than the other topologies. All transistor $M1$ - $M2$, $M7$ - $M8$ and the tail current source $M9$ must have atleast V_{ds} , sat to offer good common-mode rejection, frequency response and gain.

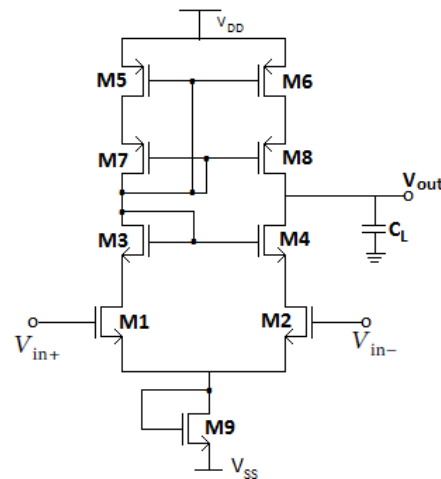


Figure-3. Telescopic amplifier topology.

(a) Gain the open-loop voltage gain is given by

$$A_v = g_{m9} r_{ds9} r_{ds4} // [g_{m7} r_{ds7} (r_{ds2} // r_{ds5})]$$

Where $g(g_{m7} \text{ } g_{m9})$ is the trans conductance of transistors ($M7$ and $M9$) and r_{ds} is the output resistance of the corresponding transistor.

(b) Unit gain bandwidth

The unity-gain bandwidth is given by the expression

$$GBW = \frac{gm1}{C_L}$$

Where C_L is the load capacitance.

(c) Phase margin The phase margin of operational amplifier depends on the sum of phase shifts, at the unity-gain frequency, contributed by the non-dominant poles ($p1$ and $p2$) and zeros (z)

$$PM = \frac{gm6}{GBW \cdot C_L}$$

(d) Slew rate For this operational amplifier, the slew rate is given by

$$SR = \frac{I_9}{C_L}$$

Where I_5 is the current that flows through transistor $M5$.

(e) Power consumption

power consumption is given by

$$P = (V_{DD} - V_{SS})(I_9)$$

(f) Area The area A of the operational amplifier is given by

$$\text{Area} = \sum_{i=1}^9 W_i \cdot L_i$$



3. OPTIMIZATION METHODOLOGY

When only one objective function involves in the problem, it is called single objective optimization, however in most real world problems more than one objective function is required to be optimized, like device sizing of an op-amp and therefore these problems are named multi-objective optimization. And appropriate algorithms are to be used according to the problem in order to get the optimized solutions. Multi Objective Genetic Algorithm (MOGA) is used for this kind of problems as the requirements of many objectives have to be optimized.

MOGA is an extension of the classical GA. The main difference between a conventional GA and a MOGA lies in the assignment of fitness to an individual. The rest of the algorithm is the same as that in a classical GA. In a MOGA, first, each solution is checked for its domination in the population.

Therefore, the use of multiple-objective optimization algorithms is of a great importance to the automatic design of operational amplifier. Accuracy, ease of use, generality, robustness, and reasonable run-time are necessary for a circuit synthesis solution to gain acceptance by using optimization methods. This method uses a program based on multi objective optimization using a genetic algorithm to calculate the optimal transistors dimensions i.e. length and width of an operational amplifier which is used as part of an electronic front-end for signal shaping stage. The method which handles a wide variety of specifications and constraints is extremely fast and results in globally optimal designs. The aim of this work is to design and optimize an operational amplifier circuit in sight of a front-end electronics.

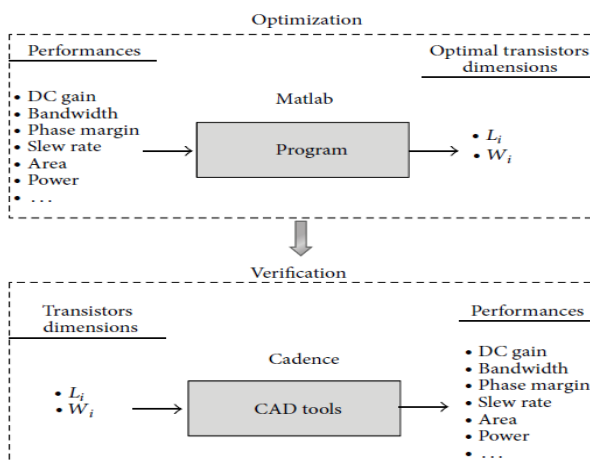


Figure-4. Design flow.

Here is how the design process goes, initially the specifications of the design are considered and taken as the key parameters. These are used in the optimization tool box and a code is running in the backend of the tool. Once the tool box completed running the output will be the transistor optimized dimensions i.e. width and length of each transistor in the circuit.

Here MATLAB is used to develop the optimization algorithm. Genetic algorithms start with an initial population of randomly generated individuals. Each individual in the population represents a possible solution to the problem of the study. Individuals evolve through successive iterations, called generations. In every generation, each individual in the population is evaluated using a measure of fitness. To pass from one generation k to generation $k + 1$, the following operations are performed. The population is reproduced by good selection where individuals with the best evaluations tend to reproduce more often than those with bad evaluations. Then, the population of the next generation is created by genetic operators.

This population is applied to cross pairs of individuals (parents) of a certain proportion of the population using crossover operator to produce new children. A mutation operator is applied to a certain proportion of the population. Finally, the new individuals are evaluated and incorporated into the population of the next generation and the procedure continues until the stop condition is satisfied several stopping criteria of the algorithm are possible: the number of generations can be fixed a priori or the algorithm can be stopped when the population does not evolve fast enough. Steps involved in solving and designing procedure of Multi Objective Genetic Algorithm.

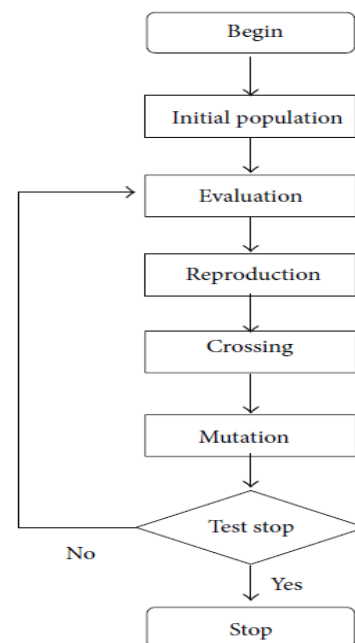


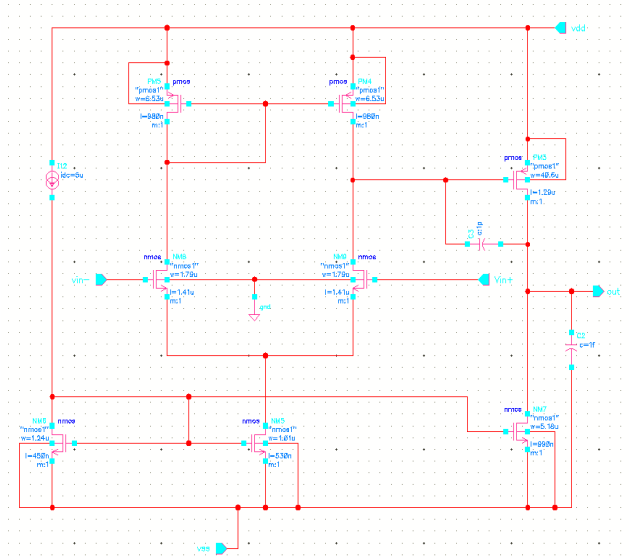
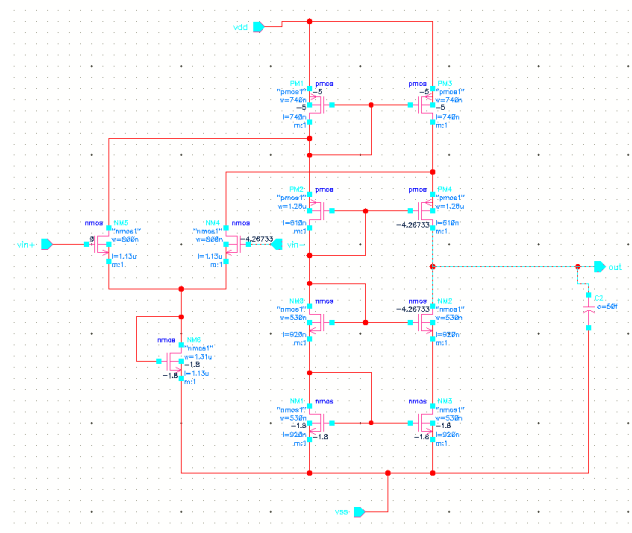
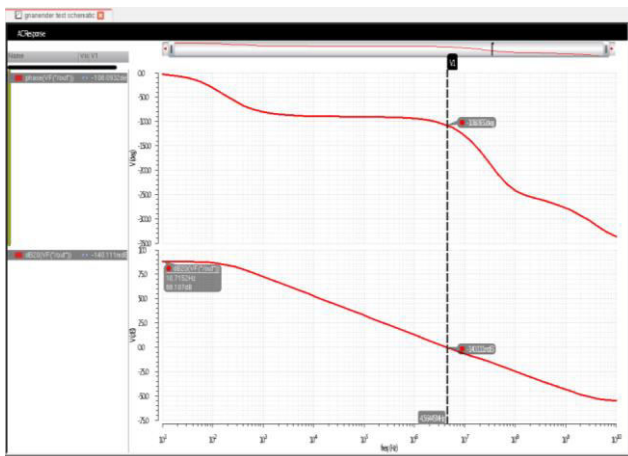
Figure-5. Flow chart of GA.

4. MEASUREMENT RESULT

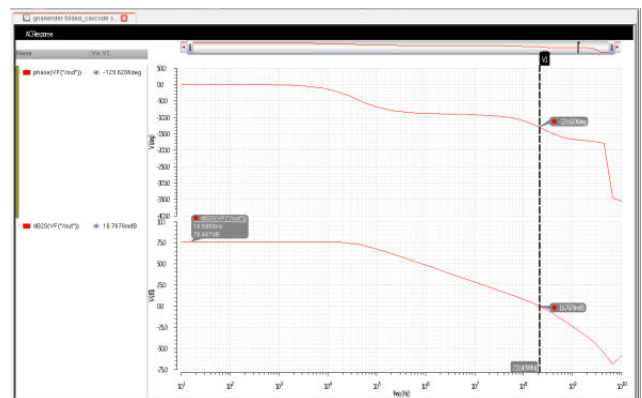
Overall output of optimization Algorithm for each topology is tabulated in Table-1 with respect to their input specifications. These transistor dimensions are used in the EDA tools to verify the parameters. In this work Cadence Virtuoso is used for simulation.

**Table-1.** Transistor dimensions of each topology.

| Two stage Op-amp | | Folded cascode Op-amp | | Telescopic Op-amp | |
|--|---|---|--|--|---|
| Width | Length | Width | Length | Width | Length |
| W1=1.79 W2=1.79 W3=6.53 W4=6.53 W5=1.01 W6=40.6 W7=5.18 W8=1.24 | L1=1.41 L2=1.4 L3=0.98 L4=0.98 L5=0.53 L6=1.29 L7=0.99 L8=0.45 | W1=0.8 W2=0.8 W3=1.31 W4=0.7 W5=0.74 W6=1.28 W7=1.28 W8=0.53 W9=0.53 W10=0.53 W11=0.53 | L1=1.13 L2=1.13 L3=1.13 L4=0.74 L5=0.74 L6=0.61 L7=0.61 L8=0.92 L9=0.92 L10=0.92 L11=0.92 | W1=1.04 W2=1.0 W3=1.38 W4=1.38 W5=1.28 W6=1.28 W7=1.04 W8=1.04 W9=1.10 | L1=0.74 L2=0.74 L3=0.49 L4=0.49 L5=0.45 L6=0.45 L7=1.16 L8=1.16 L9=0.89 |

**Figure-6.** Schematic of two stage Op-amp.**Figure-8.** Schematic of folded cascode Op-amp.**Figure-7.** Simulation result of gain, phase margin and UGF for two stage Op-amp.

From the magnitude and phase plot shown in Figure-7 it can be seen that Gain is 88.05dB, Phase Margin and UGF are calculated at 0dB of Gain which are read as 61.5deg i.e. $180 - 118.5$ (from plot) = 61.5deg and 4.56MHz.

**Figure-9.** Simulation result of gain, phase margin and UGF for folded cascode Op-amp.

From the magnitude and phase plot shown in Figure-9 it can be seen that Gain is 76.47dB, Phase Margin and UGF are calculated at 0dB of Gain which are read as 52deg i.e. $180 - 129.6$ (from plot) = 52deg and 213.905MHz.

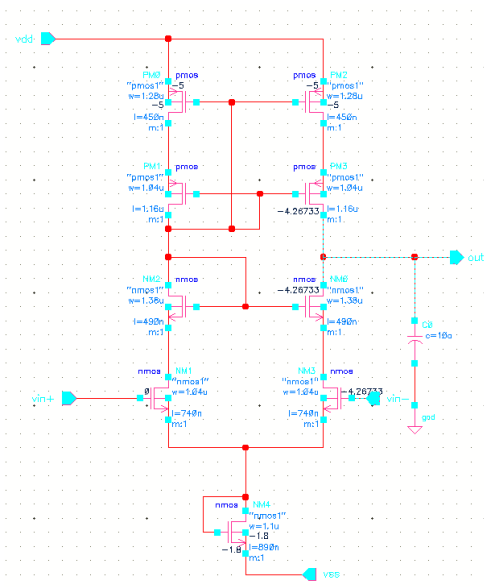


Figure-10. Schematic of telescopic cascode Op-amp.

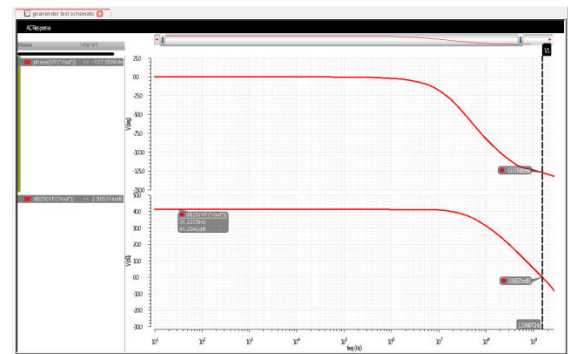


Figure-11. Simulation result of gain, phase margin and UGF for Telescopic Op-amp.

From the magnitude and phase plot shown in Figure-11 it can be seen that Gain is 41.20dB, Phase Margin and UGF are calculated at 0dB of Gain which are read as 53deg i.e. $180 - 127(\text{from plot}) = 53\text{deg}$ and 1.53GHz.

Table-2. Comparison of input specifications and final simulation results of three topologies.

| Topology | Two stage Opamp | | Folded cascode Opamp | | Telescopic Opamp | |
|----------------------|---------------------------------|----------------------------|---------------------------------|-------------------------------|---------------------------------|------------------------------|
| Performances | Specifications in MOGA (MATLAB) | Spectre (Cadence) | Specifications in MOGA (MATLAB) | Spectre (Cadence) | Specifications in MOGA (MATLAB) | Spectre (Cadence) |
| Gain | 80dB | 88.05Db | 60dB | 76.47dB | 50dB | 41.2dB |
| Unity Gain Frequency | 5MHz | 4.65MHz | 100MHz | 213.9MHz | 1000MHz | 1.53GHz |
| Slew rate | $>5\text{V}/\mu\text{s}$ | $7.37\text{v}/\mu\text{s}$ | $>100\text{V}/\mu\text{s}$ | $258.345\text{v}/\mu\text{s}$ | $>100\text{V}/\mu\text{s}$ | $425.53\text{v}/\mu\text{s}$ |
| Phase Margin | 60deg | 61.5deg | 60deg | 62deg | 60deg | 53deg |
| Power Consumption | $\leq 50\mu\text{W}$ | $26.89\mu\text{W}$ | $\leq 100\mu\text{W}$ | $90.1\mu\text{W}$ | $\leq 100\mu\text{W}$ | $80.26\mu\text{W}$ |
| Area | $100\mu\text{m}^2$ | $76.442\mu\text{m}^2$ | $100\mu\text{m}^2$ | $7.895\mu\text{m}^2$ | $100\mu\text{m}^2$ | $7.435\mu\text{m}^2$ |
| CMRR | NA | 89.15dB | NA | 85.53dB | NA | 44.09dB |

4. CONCLUSIONS

A Multi-Objective optimization methodology is proposed to optimize the performances of three op-amp topologies (i.e. two-stage op-amp, folded cascode op-amp, telescopic op-amp) have been analysed. it has been verified that The automatic tool produced results competitive with human designed topologies and ,in some cases, followed standard micro power strategies used in transistor biasing.circuits with low power consumption and with acceptable valuefor Gain ,Gain Bandwidth(GBW), Phase Margin (PM) and Area have been synthesised. the results prove the effectiveness of the approach in the analog design where the design space is too complicated to be done with the classical methods within a short time .it can be concluded that the proposed approach is efficient and gives promising results for circuits design and optimization problems. The continuation of work involves tackling larger analog

circuits, including noise as one as one of the objectives and use this algorithm for communication application, in which a good balance between speed and power consumption has to be achieved.

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REFERENCES

- [1] Abdelghani Dendouga, slimane Oussalah, Damien Thienpont, and Abdenour Lounis. 2014. Multiobjective Genetic Algorithms Program for the Optimization of an OTA for Front-End Electronics. Hindawi Publishing Corporation Advances in Electrical Engineering. Vol. 2014.
- [2] Samir BARRA, Brahim LAKEHAL, Abdelgh NIDENDOUGA, Souhil KOUDA, Nour-Eddine BOUGUECHAL. 2013. Optimization of Fully-Differential Folded Cascode Amplifier via Multi-Objective Genetic Algorithms. The International Conference on Electronics & Oil: From Theory to Applications, Ouargla, Algeria.
- [3] Maria del Mar Hershenson, Stephen P. Boyd, fellow, IEEE, and Thomas H. Lee. 2001. Optimal Design of a CMOS Op-Amp via Geometric Programming. IEEE Transactions on computer-aided design of integrated circuits and systems. 20(1).
- [4] Lucas Compassive Severo, Alessandro Girardi. Simulation-Based Evolutionary Heuristic to Sizing Analog Integrated Circuits. Federal University of Pampa-UNIPAMPA Alegrete-RS-Brazil.
- [5] Priyanka Kakoty. 2011. Design of a high frequency low voltage CMOS operational amplifier. VLSICS. 2(1).
- [6] Haresh S. Chaudhari, Nilesh D. Patel and Jaydip H. Chaudhari. 2013. Optimization and Simulation of Two Stage Operational Amplifier Using 180nm and 250nm Technology. IJETTCS. 2(2).
- [7] M. A. Aguirre, J. Chávez, A. Torralba, and L. G. Franquelo. 1994. Analog design optimization by means of a tabu search approach. in Proc. IEEE Int. Symp. Circuits Syst. 1: 375-378.
- [8] B. K. Ahuja. 1983. An improved frequency compensation technique for CMOS operational amplifiers. IEEE J. Solid-State Circuits. 18: 629-633.
- [9] P. E. Allen and D. R. Holberg. 1987. CMOS Analog Circuit Design, 1st ed, U.K.: Oxford.
- [10] J. Tao, X. Chen, and Y. Zhu. 2010. Constraint multi-objective automated synthesis for CMOS operational amplifier. in Life System Modeling and Intelligent Computing, vol. 6329 of Lecture Notes in Computer Science. pp. 120-127.
- [11] M. Takhti, A. Beirami, and H. Shamsi. 2009. Multi-objective design automation of the folded-cascode OP-AMP using nsga-II strategy. in Proceedings of the International Symposium on Signals, Circuits and Systems (ISSCS '09), pp. 1-4, Iasi, Romania.
- [12] M. Kubař, J. Jakovenko. 2010. Novel Analog Synthesis Tool Implemented to the Cadence Design Environment, Proc. of SM2ACD.
- [13] H.D. Dammak, S. Bensalem, S. Zouari, and M. Loulou. 2008. Design of folded cascade OTA in different regions of operation through gm/ID methodology. International Journal of Electrical and Electronics Engineering. pp. 178-183.
- [14] M. G. R. Degrauwe, O. Nys, E. Dijkstra *et al.* 1987. IDAC: an interactive design tool for analog CMOS circuits. IEEE Journal of Solid-State Circuits. SC-22(6): 1106-1116.
- [15] M. D.M. Hershenson, S.P. Boyd, and T.H. Lee. 1998. GPCAD: a tool for CMOS operational amplifier synthesis. in Proceedings of the IEEE/ACM International Conference on Computer-Aided Design (ICCAD '98), pp. 296-303, San Jose, Calif, USA.
- [16] J. Tao, X. Chen, and Y. Zhu. 2010. Constraint multi-objective automated synthesis for CMOS operational amplifier. in Life System Modeling and Intelligent Computing, vol. 6329 of Lecture Notes in Computer Science. pp. 120-127.
- [17] P. Jianhai Yu and Z. Mao. 2007. Automated design method for parameters optimization of CMOS analog circuits based on adaptive genetic algorithm. in Proceedings of the 7th International Conference on ASIC (ASICON '07), pp. 1217-1220, Guilin, China.
- [18] P. P. Kumar and K. Duraiswamy. 2012. An optimized device sizing of analog circuits using particle swarm optimization. Journal of Computer Science. 8(6): 930-935.
- [19] D. Nageshwarrao, S. Venkata C. and V. Malleswara R. 2010. Gain Boosted Telescopic OTA with 110dB Gain and 1.8GHz UGF. International Journal of Electronic Engineering Research. 2(2): 159-166.
- [20] M. Fakhfakh. 2009. A novel Alienor-based heuristic for the optimal design of analog circuits. Microelectronics Journal. 40: 141-148.



- [21] A. Somani, P.P. Chakrabarti, A. Patra. 2007. An Evolutionary Algorithm-Based Approach to Automated Design of Analog and RF Circuits Using Adaptive Normalized Cost Functions. IEEE Transactions on Evolutionary Computation. 11: 336-353.