VOL. 12, NO. 16, AUGUST 2017 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

WELDING POWER SUPPLY WITH IMPROVED POWER QUALITY

Srividya A. S., S. Malathi and J. Jayachandran
Department of Electrical and Electronics Engineering, SASTRA University, India

ABSTRACT

A switched mode power supply for Manual Metal Arc Welding (MMAW) is proposed in this paper. This is done as a comparative study, using two different converters at the front end - namely, Zeta converter and Canonical Switching Cell converter. Both the converters operate in discontinuous inductor current mode (DICM) to accomplish inherent Power Factor Correction (PFC). This mode of operation reduces the intricacy of control and provides considerable dc-voltage regulation. A pulse width modulated (PWM) isolated full bridge dc-dc converter is used at the load side, for both the designs to provide high frequency isolation. A closed loop control is being envisaged to incorporate dc voltage regulation at the output and to provide over current protection, so that the designs are suitable for the intended application. The designs have been simulated and the results obtained show how these two designs satisfy the requirement of the power supply for arc welding process. The performance of the two power supplies have been evaluated on the basis of power supply current, dynamic characteristics, power factor and voltage regulation.

Keywords: cell converter, canonical switching, voltage regulation, pulse width modulation.

1. INTRODUCTION

Welding is one of the most important process in manufacturing industries. There are several welding techniques, among which, arc welding is the most commonly used in fabrication processes. Several industries like the automotive, construction, chemical, power generation etc immensely depend on this process and a major amount of electrical power is consumed by these power supplies. There are two major forms of arc welding power supply - one with dc output, and another with dc output. A dc power supply has current and voltage at a steady polarity. This gives a stable arc and a smooth weld in comparison to the power supply with an ac output. An ac output power supply does not have a steady polarity voltage or current, which is suitable only for aluminium welding [1].

The quality of the weld essentially relies on the power supply deployed. The power supplies for the Welding process can be designed using several configurations of circuits. A general dc Arc Welding Power Supply (AWPS) employs an uncontrolled diode bridge rectifier, which is trailed by a large dc-link capacitor, at the front end. The power quality indices were measured for the conventional power supply (power factor, total harmonic distortion of the input current) and it was observed that the existing power supplies have a low power factor (PF) and large harmonic currents. This causes increased losses in the utility side. Subsequent works led to development of Power Factor Correction based AWPS with better power quality [2], [3]. The Welding Power Supplies must yield a low value of THD and a high PF as per IEC 61000-3-2 and IEEE 519-1992 standards [4]. As far as the AWPS is concerned, fast dynamic response and short circuit/over current protection are the most mandatory features.

The AWPS is designed based on it overcurrent response, arc stability, etc. For satisfactory weld performance, a welding power supply with a constant arc length, constant output voltage and current is chosen, as mentioned above [5]. However, the foremost feature of the welding power supply is to provide output voltage regulation and to limit the output current, so as to provide a high quality weld. Several topologies can be used for designing a power supply for welding application.

A power supply designed with a boost converter has certain drawbacks, like high current at start-up. It also has not output current limiting capability. The key factors of welding power supply are not complied. A buck converter is also proposed in [6], but again here, the capacitors used are of large value. The switches used in these conventional converters are switched at a high frequency, causing voltage stress across the switch and also increases switching losses. Moreover, it does not match the high frequency commutation current. This drawback hampers the use of power supplies designed based on half/full bridge inverters. Next up, buck-boost converters offer better performance than the above mentioned converters. Various single stage isolated PFC configurations can be compared with two stage converters. Among the several topologies, the Zeta and CSC offer better power factor correction.

The above mentioned problems are taken care of in the proposed configuration. In case the inductor is designed to operate continuously, i.e., in Continuous Conduction Mode (CCM) as presented in [7], an additional input current sensing is required to imbibe power factor correction. Moreover, operating the converters in DICM mode has eradicated the extra current sensing feature, which adds to the complexity of the design. To offer a wide range of operation, the DICM is found to be suitable by using reduced number of components and sensing circuitry etc. Further, a feedback circuitry has been incorporated to handle overcurrent in the power supply. This helps in achieving an improved weld quality. In short, the converter can be used to control several parameters, like the welding current, voltage, trigger pulse duty cycle, limit of overload current, and so on. The performance of the two converters has been verified by modelling the design in MATLAB/Simulink environment. The simulated results are found to confirm

the practical usability of the converter, with the various power quality factors, conforming to the standards.

2. ZETA CONVERTER BASED AWPS CIRCUIT CONFIGURATION

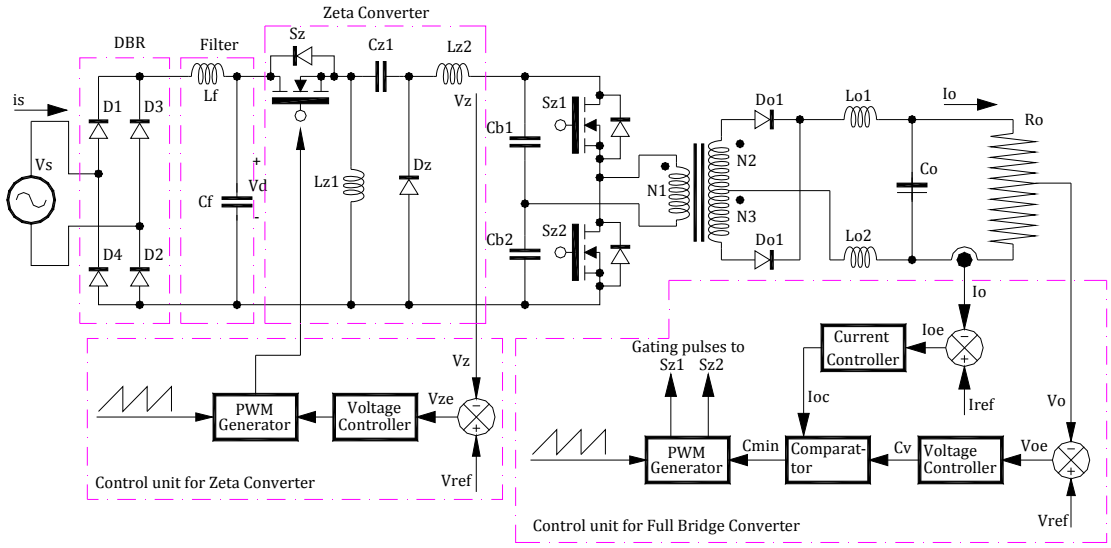


Figure-1. Schematic of Zeta converter based AWPS.

A Diode Bridge Rectifier (DBR) with a LC filter is connected to the input side of a non-isolated Zeta converter. This contains two inductors L_{z1} and L_{z2}, an intermediate capacitor C_1, a high frequency switch S_z and a diode D_z. The voltage obtained at the converter is terminated at the isolated converter, containing two capacitors of equal value, two transistor switches and a high frequency transformer (HFT). The voltage output from the HFT is connected to LC filters before it terminated to electrical load.

The AC mains input voltage is rectified using the diode bridge rectifier as indicated in the above figure. The DC voltage is connected to a LC filter circuit to narrow down the ripples. The PFC Zeta converter receives the filtered DC voltage, which regulates the obtained DC output voltage and makes the circuit to draw a sinusoidal current from the AC mains at unity power factor. The three different operating conditions - DCM conditions (input inductor operating in DCM, capacitor operating in DCM and the output inductor operating in DCM) are analyzed to fix the best operating mode for the PFC converter at the front-end. When the output inductor is operating in DCM, it is observed that the THD obtained is lowest. The DC output voltage so obtained from the Zeta converter is connected to the isolated converter to achieve a DC voltage at the output. Two transistor switches present in the isolated converter are operated at a high frequency, so that an AC voltage is obtained, which is then given to the high frequency transformer (HFT). A full wave bridge configuration is configured for best core utilization. LC Filters are provided in each output winding to decrease the ripples present in the output voltage and output current. The isolated converter is operated in CCM, to reduce the component stresses.

OPERATING PRINCIPLE

To understand the whole operation of the power supply, the different Discontinuous Conduction Modes (DCM)of operations are deliberated, i.e., the input inductor (L_1) operating in DCM, the intermediate capacitor (C_1) operating in DCM and the output inductor (L_2) operating in DCM.

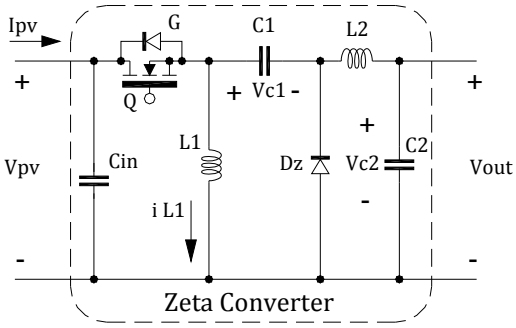


Figure-2. Zeta converter.

The Zeta converter is analysed for Discontinuous Conduction Mode in all the three components (input inductor L1, intermediate capacitor C1 and output inductor L2). The converter has better performance when the inductor L2 has discontinuous current compared to that when the rest two components have discontinuous current. The circuit is analysed in this scenario and is explained below.

The operation of the PFC converter with output inductor in working in DCM. The waveforms of the various components of the Zeta converter during the

output inductor operating in DCM are indicated for one switching cycle.

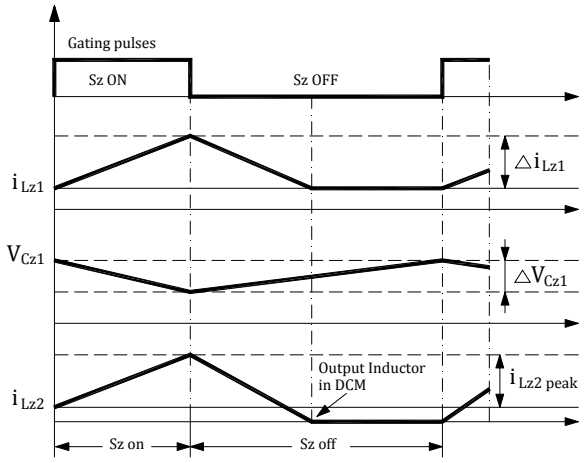


Figure-3. Waveforms of various components. (L_{z2} in DCM).

DESIGN

The design of the circuit is based on the switch on and switch off period, i.e., change in the inductor current in this phase. The characteristics of the transistor switches and the diodes are considered to be ideal. The transistor switching frequency is much higher than the AC power line frequency.

Duty ratio of the PFC Zeta converter is given by,

$$D(t) = \frac{V_{dc}}{V_{in}(t) + V_{dc}}. \quad (1)$$

where, D(t) is the duty ratio of the Zeta converter, V_{dc} is the output voltage of the Zeta converter and V_{in} is the input voltage from AC power lines.

a. Selection of the value of input inductor

The critical inductance value is given by

$$L_{z1\min} = \frac{D(t)TV_{in}(t)}{\Delta i_{in}(t)} = \frac{V_{in}(t)T}{\Delta i_{in}(t)}\left[\frac{V_{dc}}{V_{in}(t) + V_{dc}}\right]$$

$$L_{z1\min} = \frac{1.414\times170\times50\mu S}{0.5\times2.05\times1.414}\left[\frac{300}{(1.414\times170)+300}\right] = 4.6mH \quad (2)$$

where D(t) is the duty ratio, V_{in} and I_{in} are the input voltage and current drawn respectively, from the AC mains supply and T is the total switching time in one switching cycle. The value of the inductor is estimated to be *0.92 mH* and is proportional to the rms value of AC supply voltage.

Minimum value of inductor for DCM operation = 0.2 mH
Minimum value of inductor for CCM operation = 4.6 mH

b. Selection of the value of output inductor

The critical inductance value estimated by,

$$L_{z2\min} = \frac{(1-D(t))TV_{dc}(t)}{2I_{dc}} = \frac{V_{dc}DT}{2I_{in}(t)} = \frac{R_{in}V_{dc}D(t)T}{2V_{in}(t)}$$

$$= \frac{V_d{}^2TV_{dc}}{2V_{in}(t)P_{in}}\left[\frac{V_{dc}}{V_{in}(t)+V_{dc}}\right]$$

$$L_{z2\min} = \frac{(153.1)^2\times50\mu S\times300}{2\times350\times1.414\times170}\left[\frac{300}{(1.414\times170)+300}\right] = 1.15mH \quad (3)$$

where V_{dc} and I_{dc} are the output voltage and current of the PFC Zeta converter, respectively.

The value of the inductor is estimated to be 1.15 *mH* and the value is also proportional to the rms value of supply voltage.

Minimum value of the output inductor for DCM operation = 0.7 mH
Minimum value of the output inductor for CCM operation = 5.75 mH

c. Selection of the value of intermediate capacitor

The value of the capacitor for CCM operation is given by,

$$C_1 = \frac{D(t)TV_{dc}R_{dc}}{2V_{c1}} = \frac{TV_{dc}}{2\{\Delta(V_{dc}+V_{in}(t))\}\left[\frac{V_{dc}{}^2}{P_{in}}\right]}\times\frac{V_{dc}}{V_{dc}+V_{in}(t)}$$

$$= \frac{TP_{in}}{2\left(\Delta(V_{dc}+V_{in}(t))\right)\times(V_{dc}+V_{in}(t))}$$

$$C_1 = \frac{50\mu S\times350}{2\left(0.3(300+270(1.414))\right)\times(300+270(1.414))} = 0.0628\mu F \quad (4)$$

where Δ is the permissible ripple in the voltage across the intermediate capacitor, P_{in} is the input power and V_{C1} is the voltage across the intermediate capacitor.

The value of the capacitor is estimated to be *0.0628 μF*.

Hence, the practical value of the Capacitor value selected = 0.066 μF.

d. Selection of the output capacitor

The working of the output capacitor is inline with the operation of the input capacitor of the isolated converter. The value of the output capacitor is selected in a manner so as to eradicate the second order harmonic voltage.

$$C_h = \frac{I_{dc}}{2\omega\Delta V_{dc}} \quad (5)$$

For a 9 V ripple, the value estimated = *400 μF*.

e. Design of filter

The filter is important in keeping the harmonic distortion at the AC input mains power supply at a low

value. The value of the inductor and capacitor constituting the filer section, are calculated as,

$$C_{\max} = \frac{I_p \tan\theta}{2\pi f V_p} \quad (6)$$

where θ is assumed as 1° for maintaining a high power factor, V_p and I_p are the peak input voltage and input current. The maximum value of capacitor is estimated as *0.4 μF*.

$$L_d = \frac{1}{4\pi^2 f_c^2 C_d} \quad (7)$$

Here f_c is the cut-off frequency. The value of the same is selected such that it is much more than the AC power supply line frequency (f = 50Hz) and less than the transistor switching frequency (f_s = 20kHz). Cut-off frequency is considered as 2 kHz. The corresponding value of inductor is estimated to be *3.1 mH.*

The transistor switches present at the primary side of the HFT are operated at *60 kHz.*

CONTROL

There are two self-regulating controllers provided to control the output voltages of the Zeta converter and the isolated converter. The front-end (Zeta) converter is controlled using the voltage follower approach and the back end (isolated) converter uses the average current control technique.

a. Control of the PFC converter

The control circuit of the front-end converter produces pulses in accordance with the output voltage error. The error is the difference in voltage between the desired level of voltage and the measured voltage.

The voltage error at an instant *n* is given by the expression,

$$V_e(n) = V_{dcref} - V_{dc}(n) \quad (8)$$

The voltage error V_e is supplied to the proportional-integral (PI) controller to produce a controlled output voltage (V_{co}).

$$V_{co}(n) = V_{co}(n-1) + k_p V_e(n) - V_e(n-1) + k_i V_e(n) \quad (9)$$

where k_p and k_i are the proportional gain and integral gain to be set for the PI controller.

The output signal from the PI controller is then compared to a high-frequency saw-tooth signal (S_t) to produce the PWM pulses required to trigger the transistor switches.

When $S_t < V_{co}$, then S = ON, else S = OFF, S represents the switching signal output from the PWM generator, to trigger for the transistor switch. If the output voltage varies, the output voltage V_{co} also changes to adjust the duty cycle. Thus, the on and off time (width) of PWM pulses changes suitably to maintain the output DC voltage at a constant value.

b. Control of the isolated converter

To control the output voltages of the isolated converter, average current control method is used. For control, the output voltage obtained V_o is measured and compared to a reference voltage V_{ref}, to generate a voltage error which is the input to the PI controller.

The output of the PI controller is compared to a saw-tooth wave signal to produce the switching pulses to make both the transistor switches on and off alternately in each half cycle of one PWM period with sufficient dead time to avoid shoot-through. The width of the pulses changes as per the voltage error output of the comparator. By modifying the duty cycle of the PWM pulses, the control of the isolated converter is able to respond to other output voltage variations.

The estimated values of all the components are tabulated in Table-1.

Table-1. Specifications for Zeta converter based Awps.

Component	Calculated value	Selected value
Inductor, L_{z1}	4.6 mH	5 mH
Inductor, L_{z2}	1.15 mH	0.7 mH
Capacitor, C_z	0.062 μF	66 nF
Capacitor, C_{b1}, C_{b2}	630 μF	660 μF

SIMULATION RESULTS

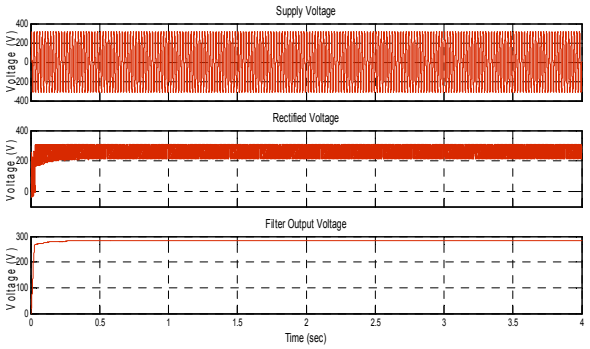


Figure-4. Input voltage - 220V, rectified voltage and the filtered input voltage.

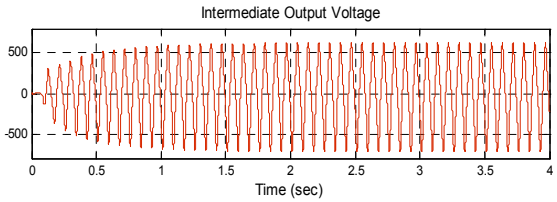


Figure-5. Voltage at the primary side of HFT.

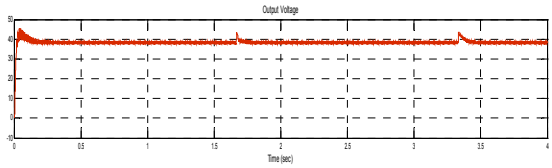


Figure-6. Load voltage - 45V.

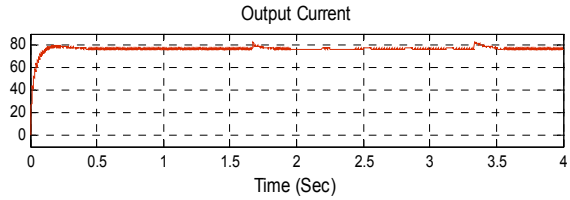


Figure-7. Load current - 75 A.

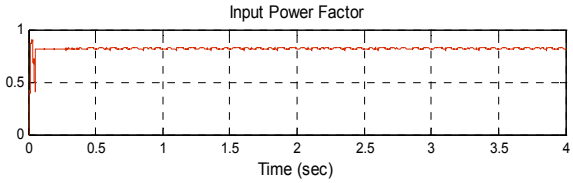


Figure-8. Input power factor - 0.7.

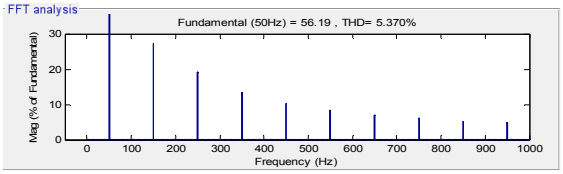


Figure-9. Input current THD - 5.37%.

OPERATION

The operating principle of the converters has been elaborately explained in this section. Certain assumptions have been made to explain the working of the welding power supply:

a) all semiconductor devices have been considered ideal;
b) the capacitors C_{bo} and C_o were of large value to maintain constant output voltages V_{co} and V_o without any ripple for one switching period;
c) as the switching frequency (f_s) >> the line frequency (f), the supply voltage has been considered constant for one switching frequency cycle.

3. CSC CONVERTER BASED AWPS

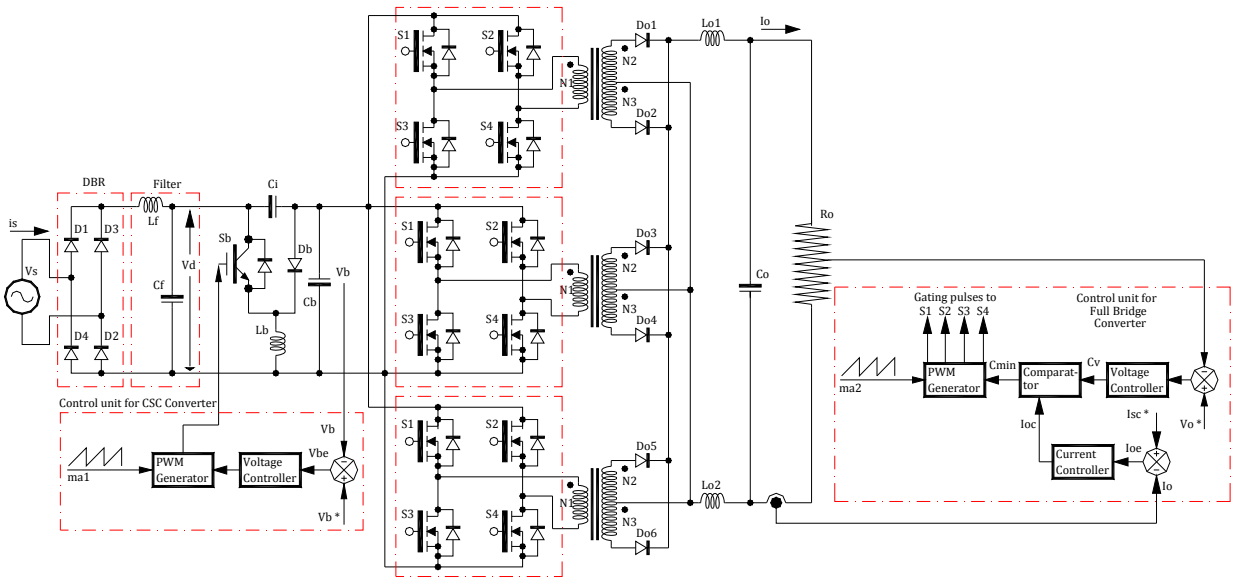
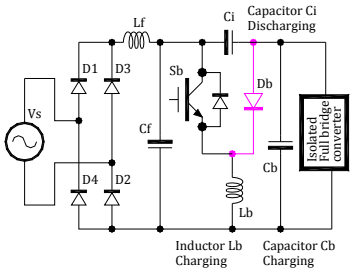
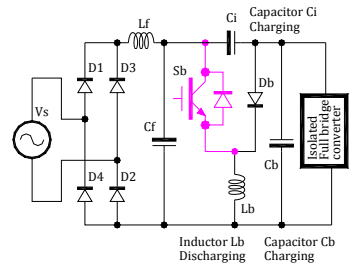


Figure-10. Schematic of CSC converter based AWPS.

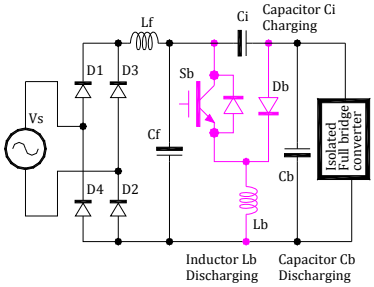
MODES OF OPERATION OF CSC CONVERTER



(a) Mode-I



(b) Mode-II



(c) Mode-III

Figure-11. Operating modes of CSC converter.

The CSC converter operates in a similar manner as that of a standard Cuk converter, though the latter uses two inductors as compared to one in the former. The operating modes have been shown in Figure-11. The input to the CSC converter is given from the supply through the Diode Bridge Rectifier. When the CSC converter operates in DICM, three intermediate operating modes are described for every switching cycle, which involves the charging/discharging of the capacitors/inductor, due to the turn on and off of the switch and the diode. This is discussed in detail:

Mode I: In this mode, the switch S_c is on and the diode D_c is in reverse biased state. During this period, the inductor L_c is charged through both the supply and the capacitor C_c. This is shown in Figure-11a. This causes the capacitor C_c to discharge through the inductor Lb and the dc-link capacitor *Cb*, which leads to decrease in voltage across the capacitor C_c. Hence, the capacitor value should be large as to maintain a continuous voltage during this interval.

Mode II: This mode begins when the switch is turned off and the diode is forward biased. Here, the energy stored in the inductor L_c is transferred to the capacitor C_c and the dc-link capacitor C_{co}. These capacitors start charging and the voltages across them starts increasing. However, the inductor current decreases. This stage is shown in Figure-11b.

Mode III: The DICM mode of operation of the converter starts in this mode, when the inductor current i_{Lco} becomes zero. The capacitor keeps charging through the supply. The current to the converter is given by the dc-link capacitor, as the diode is reverse biased. This is shown in Figure-11c. This completes one switching cycle. The inductor current remains zero until the switch is turned on to continue the switching sequence.

MODES OF OPERATION OF FULL BRIDGE CONVERTER

The isolated full bridge converter is fed by the controlled output of the CSC converter. It is designed as a buck converter, as it is required to step down the dc-link voltage to a required level. To reduce the switching device rating and to extend the range of output power rating, three FB converters are connected in parallel. The FB converters operate in Continuous Conduction Mode. The operating modes are explained.

Mode I: In this mode, the switches S1 and S4 are triggered and the dc-link capacitor voltage appears across the primary winding of the high-frequency transformer (HFT). The diodes connected to the first half of the secondary winding are forward biased. The inductors connected at the output (L_{o1} and L_{o2}) start storing energy, causing the inductor current to increase. However, the output filter capacitor C_o discharges through the load.

Mode II: This mode is begins when all the switches S1, S2, S3 and S4 are turned off and all the diodes connected on the secondary winding of the transformer act as freewheeling diodes. The energy in the inductors is discharged to the output capacitor C_o and the load. This causes the current of the inductor to decrease linearly.

Mode III: This mode is similar to Mode I, switch pair S2 and S3 is triggered to shift the energy to the load. Again, the diodes Do1, Do3 and Do5 remain reverse biased and the output capacitor Co discharges through the load.

Mode IV: Modes II and IV are analogous as well. None of the switch pairs conduct and all the output rectifier diodes freewheel the energy piled up in the inductors. The output capacitor C_o is charged by the energy released by the inductors. This mode ceases when the switches S1 and S4 are triggered again and the operation repeats in successive switching cycles.

DESIGN OF CSC CONVERTER BASED AWPS

The AWPS has been simulated for a power rating of 1.5kW. It has been seen that the power supply is highly effective for welding purposes. The switching frequency of both the front end and isolated converters is much higher than the line frequency. Hence, the supply voltage is supposed to be a constant during one switching cycle.

A) Design of input filter

The output obtained at the DBR is given to the filter circuit consisting of an inductor and capacitor. This smoothens the input current harmonics of higher order. The filter components have been designed to obtain lower harmonic content in the current. The capacitance value is calculated as,

$$C_{\max} = \frac{I_p \tan\theta}{2\pi f V_p} \tag{10}$$

where V_p and I_p are the peak ac input voltage and current, respectively, and f is the fundamental frequency. Θ is assumed as 1°, so as to attain high power factor. The maximum value of the capacitance is approximated to 0.4 μF.

The inductor is also designed to obtain a lower harmonic content in the input current, whose value is estimated as,

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \tag{11}$$

where fc is the cut-off frequency (here, assumed as 3 kHz).

B) Design of CSC converter

The CSC converter is intended to supply a dc-link voltage of 360V at a switching frequency of 30 kHz. The inductor L_{co} has been discussed to be operating in DICM, so the current is discontinuous during a switching period. However, the capacitor voltage C_c remains continuous, unlike in the inductor. The input supply voltage (V_s) being assumed as 220 V, the rectified output of DBR (V_r) is estimated as,

$$V_r = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2}(220)}{\pi} \approx 198V \tag{12}$$

The output voltage V_c of the CSC converter is expressed by,

$$V_c = \frac{D_c}{1-D_c} V_r \tag{13}$$

where Dc is the duty ratio of the switch Sc.

The duty ratio is chosen at an optimal value for Discontinuous Operating Mode, which is given by,

$$D_{co} = \sqrt{2} M \sqrt{K_a} \tag{14}$$

where

$$M = \frac{V_c}{V_m} = \frac{360}{311} = 1.157 \tag{15}$$

and K_a is the conduction parameter.

For DICM operation,

$$K_a < \frac{1}{2(M+|\sin\omega t|)^2} \tag{16}$$

The conduction parameter for the CSC converter to operate in Discontinuous Conduction Mode is,

$$K_{a|\omega t=90^\circ} < \frac{1}{2(M+1)^2} < 0.107 \tag{17}$$

The value of duty ratio D_{cn} for the CSC converter is obtained by substituting these values in (14).

D_{cn}=0.271

A. Design of input inductors (L_c): The inductor in the CSC converter is designed to have discontinuous inductor current in every switching cycle. The nominal value of L_c is,

$$L_{cn} = \frac{V_d D_{cn}}{2 f_{sc} I_d} = \frac{198 \times 0.271}{2 \times 30000 \times 6.13} = 145.89 \mu H \tag{18}$$

where f_{sc} is the switching frequency of the CSC converter. The value of the inductor L_{co} must be less than the critical value for proper operation of the inductor in Discontinuous Conduction Mode.

B. Design of capacitor (C_c): This capacitor is designed such that the voltage across it is continuous throughout a switching period. The voltage ripple limit that is permitted is assumed to be 10% of V_{Cc}.

$$C_i = \frac{V_{co} D_{bn}}{\Delta V_{Ci} f_{sb} R_b} = \frac{P_i D_{bn}}{\Delta V_{Ci} f_{sb} V_{co}} = \frac{1500 \times 0.271}{56 \times 30000 \times 360} = 0.672 \mu F \tag{19}$$

C. Design of DC-Link capacitor (C_{co}): The value of this capacitor relies on the voltage ripple ΔV_{co} in the dc-link voltage. Assuming the output voltage ripple to be 5% of the dc-link voltage, the capacitor value is calculated as,

$$C_b = \frac{P_o}{2\pi f_L V_{co} \Delta V_{co}} = \frac{1500}{2\pi \times 50 \times 360 \times 18} = 736.8 \mu F \tag{20}$$

where f_L is the line frequency, and ΔV_{co} is the output voltage ripple. The capacitor value is chosen as 940μF to reduce output voltage ripple.

C) Design of full bridge buck converter

Full bridge converters are used in the second stage of the AWPS. Since the required voltage required at the output is much less than that obtained at the CSC converter, the full bridge converter is a buck converter, connected in a modular manner. Hence, the devices used in each of them are of lower power rating. The input to this full bridge buck converter is the output of the CSC converter. This second stage achieves isolation by operating at a switching frequency of 100 kHz and it signifies the regular welding power supply. For simple explanation, a single module of the FB converter is considered here for analysis.

A. Design of turns ratio of HFT: The net change in the inductor current over one switching cycle is zero, for an isolated full bridge buck converter. The ratio of input to output voltage is given by,

$$\left\{V_d\left(\frac{N_2}{N_1}\right)-V_o\right\}\left(\frac{t_{ON}}{T_s}\right)-\left\{V_o\left(\frac{t_{OFF}}{T_s}\right)\right\}=0 \quad (21)$$

where $T_s=1/f_s$ indicated the switching period of the FB converter. For the rated output voltage V_o, the duty ratio is calculated by,

$$D_f=\frac{V_oV_d}{V_o}\left(\frac{N_1}{N_2}\right). \quad (22)$$

The FB buck converter operates in CCM. Thus the turns ratio is calculated to obtain an output voltage of 60V, by reorganizing the above equation.

$$\left(\frac{N_1}{N_2}\right)=\frac{2D_fV_d}{V_o}=\frac{2\times0.4\times360}{60}=4.8 \quad (23)$$

B. Design of output inductors (L_{o1} and L_{o2}): The converter in the second stage of the power supply is designed to operate in CCM. Thus the currents through these inductors must be continuous in one switching cycle. To satisfy this condition, the inductor values must be large enough to maintain continuous current. The allowed ripple in the current Δi_{Lo}, is 10% of I_o. Hence, the output inductor values are expressed by,

$$L_{o1}=\frac{V_o(0.5-D_f)}{f_s(\Delta i_{Lo1})}=\frac{60\times(0.5-0.4)}{100000\times5}=12\mu H \quad (24)$$

C. Design of output capacitor (Co): This capacitor is deliberated to alleviate the ripples in the output voltage, which can be calculated by,

$$\Delta V_o=\frac{V_o(1-2D_f)}{32f_s^{\,2}L_{o1}C_o}. \quad (25)$$

Assuming the output voltage ripple to be 10%, the value of capacitor is given by,

$$C_o=\frac{V_o(1-D_f)}{8f_s^{\,2}L_{o1}(\Delta V_o)}=\frac{60\times(1-0.4)}{8\times100000^2\times15\mu\times6}\cong5\mu F \quad (26)$$

The above calculated values for the design of the power supply, along with the component requirement is tabulated in Table-2.

Table-2. Design specifications for the proposed welding power supply.

Converter	Component	Calculated value	Opted value
CSC Converter	Inductor, L	145.89μH	90μH
	Capacitor, C	0.672μF	0.66μF
	DC-link capacitor	736.8μF	940μF
FB Buck Converter	Turns ratio, N_1/N_2	4.8	5
	Output Inductors, L_{o1} and L_{o2}	12μH	15μH
	Output Capacitor, C_o	5μF	7μF

CONTROL OF THE WELDING POWER SUPPLY

The power supply for welding application is suitably designed with two separate controllers for each converter. Here, a voltage follower approach is implemented for the first converter, i.e., the front end CSC converter, so as to achieve near unity power factor at the utility side. For the second stage converter however, a dual-loop control scheme is implemented. A concise description of both the control strategies is described.

a) Control of the CSC converter

The CSC converter is designed to operate in DICM; the voltage follower method is used. The DICM operation of the inductor in the CSC converter inherently helps in achieving power factor correction by employing a voltage feedback control loop. This regulates the dc-link voltage V_{co} in spite of output current and output voltage variations. Here, the dc-link voltage is taken as feedback and is compared to a reference voltage V_{cref}. The error voltage produced V_{ce} at any instant is expressed as,

$$V_{ce}(n)=V_{cref}\ (n)-V_c(n) \quad (27)$$

Subsequently, this error to fed to a proportional and integral (PI) controller to get a controlled output voltage.

$$V_{co}(n) = V_{co}(n-1) + k_{pv}\{V_{ce}(n) - V_{ce}(n-1)\} + k_{iv}V_{ce}(n) \quad (28)$$

where k_{pv} and k_{iv} indicate the proportional and integral gains of the PI controller respectively.

Thereafter, the output of the PI voltage controller is compared to a high frequency saw-tooth waveform to derive the trigger pulses for the switch in the CSC converter.

If the magnitude of the saw tooth wave is less than the magnitude of the controlled output voltage V_{co} at any instant, then the switch S_c will be turned on; and if the magnitude of the saw tooth wave is greater than the magnitude of the controlled output voltage V_{co}, then the switch S_c will be turned off.

b) Control of the FB buck converter

This full bridge Buck converter is anticipated to deliver a constant dc output voltage. As an adjunct function, the converter should also have current limiting function during overload conditions, so as to guarantee a high-quality weld over a wide range of voltage variation. This is one of the most indispensable criterions, which must be incorporated in the design of power supply for welding purposes. A dual loop control scheme is adopted here. In addition to tracking the output voltage, the output current is also tracked. The voltage loop is used to control the output voltage, whereas the current loop limits the output load current during overload conditions. The output voltage V_o is measured and then compared to a reference voltage V_{ref} to generate an error signal, V_e. This error signal is then fed to the PI controller, as done in the control of CSC converter, to sustain the output voltage at the required value. The output of the PI voltage controller is given by,

$$C_V(k) = C_V(k-1) + k'_{pv}\{V_e(k) - V_e(k-1)\} + k'_{iv}V_e(k) \quad (29)$$

where k'_{pv} and k'_{iv} are the proportional and integral gains of the voltage controller, respectively.

In the second loop, the output current I_o is taken as feedback signal and compared to a current limit I_{lim}. It comprises of a PI controller, which processes the error signal to confine the output current within limits.

$$C_i(k) = C_i(k-1) + k'_{pi}\{I_e(k) - I_e(k-1)\} + k'_{ii}I_e(k) \quad (30)$$

where k'_{pi} and k'_{ii} represent the proportional and integral gain constants of the current controller, respectively. Thereafter, the comparator compares the outputs of both the current and voltage controllers, and the signal with the lower amplitude is fed to the pulse width-modulated generator. It produces the gating pulses required to trigger the devices and hence the duty cycle of the switches correspond to the changes in the output voltage and current.

SIMULATION RESULTS

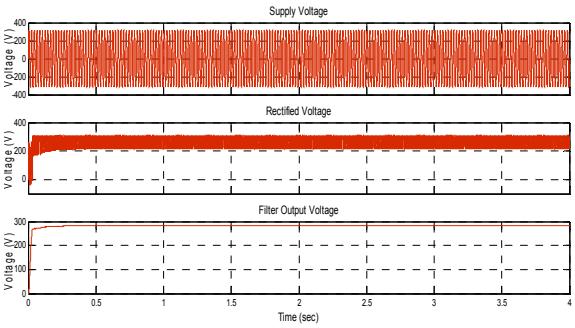


Figure-12. Supply voltage - 220V, Rectified voltage after DBR, Filtered output voltage.

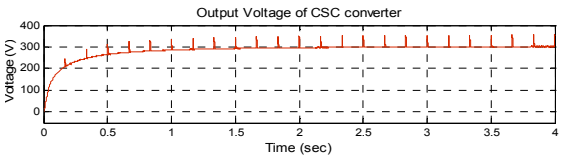


Figure-13. Voltage of the CSC converter.

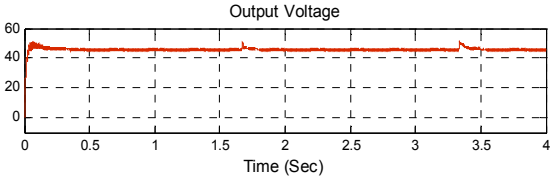


Figure-14. Load voltage - 45V.

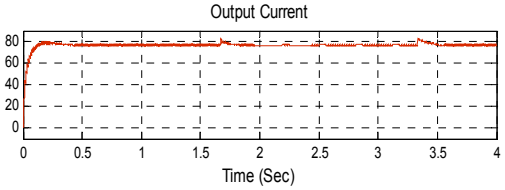


Figure-15. Load current - 75 A.

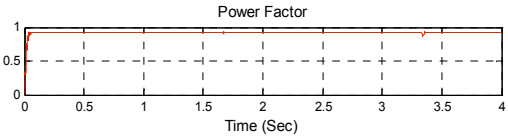


Figure-16. Input power factor - 0.9.

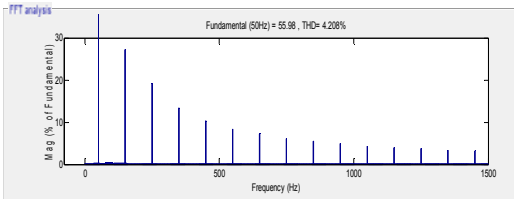


Figure-17. Input current THD = 4.20%.

4. VALIDATION OF THE AWPS WITH SIMULATION RESULTS

Table-3. Comparison of performances of the designed welding power supplies.

Parameter	Zeta based AWPS	CSC based AWPS
Input Voltage	220V	220V
Output Voltage	45V	45V
Output Current	75V	75V
Input Power Factor	0.75	0.9
Input Current THD	5.37%	4.20%

A. Steady state performance

The welding power supply is rated at 220 V supply voltage. The corresponding output voltage, output current is shown in the Figures 14, 15. The transitional results - like the CSC converter dc voltage and the current is presented in Figure-13. The output voltage is regulated to 45 V, while the dc voltage is retained at 300V. The voltage follower approach maintains a sinusoidal input current, which is in phase with the input voltage. The CSC inductor working in DICM and the continuous voltage across the intermediate capacitor is shown.

B. Comparative analysis

A comparative study was made by simulating both the designed converters and the results have been presented in Table-3. Clearly, from the tabulation, the Zeta converter has a low power factor. The power factor can be improvised by modifying the configuration, but the CSC converter provides satisfactory operation without any kind of modification. The initial cost and size of the Zeta converter is quite high compared to the CSC converter AWPS. On the basis of the observed results, it can be confirmed that the designed can be validated for the welding application and the CSC converter based AWPS achieves a better performance than the conventional welding power supplies and the Zeta converter based AWPS and can be used as a feasible solution for AWPS.

5. CONCLUSIONS

Two different configurations have been simulated in MATLAB/Simulink for the requirement of a power factor corrected power supply for welding application. The first configuration is one with a Zeta Converter in the front end. It was found to give appreciable performance in comparison with the conventional welding power suppl. The distortion in the input current has drastically decreased, along with a good input power factor. The performance was still improved with another configuration, namely a Canonical Switching Cell converter. This uses one inductor unlike the former and has been found to be performing better. The results obtained from the simulation prove the same. Better power quality is attained-with power quality indices with in specified limits. Thus the conventional power supply for welding can be replaced with the CSC converter based power supply.

REFERENCES

[1] K. Weman. 2003. Welding Process Handbook. Cambridge, MA, USA: Woodhead. pp. 13-25.

[2] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad. 2011. Comprehensive study of single phase AC-DC power factor corrected converters with high frequency isolation. IEEE Trans. Ind. Informat. 7(4): 540-556.

[3] J.-M. Wang and S.-T. Wu. 2015. A novel inverter for arc welding machines. IEEE Trans. Ind. Electron. 62(3): 1431-1439.

[4] 20004. Limits for Harmonic Emissions. International Electro Technical Commission Standard 61000-3-2.

[5] Q. F. Teng, W. Z. Zhang, J. G. Zhu, and Y.G. Guo. 2011. Modeling of arc welding power supply. in Proc. Int. Conf. *Appl.* Supercond. Electromagn. Devices. pp. 228-231.

[6] K. Mahmoodi, M. Jafari and Z. Malekjamshidi. 2012. Operation of a Fuzzy controlled half-bridge DC-converter as a welding current-source. Indonesian J. Elect. Eng. 10(1): 17-24.

[7] D. Murthy-Bellur and M. K. Kazimierczuk. 2011. Isolated two-transistor Zeta converter with reduced transistor voltage stress. IEEE Trans. Circuits Syst. I, Reg. Papers. 58(1): 41-45.