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RELAXED TIMING ISSUE IN GLOBAL FEEDBACK PATHS OF UNITY-STF SMASH SIGMA DELTA MODULATOR ARCHITECTURE

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ABSTRACT

This Paper presents a practical way to improve signal bandwidth and resolution in a Sturdy Multi-Stage Noise-Shaping (SMASH) sigma delta modulator. In this way, the processing timing issue in the critical paths of the proposed architecture has been relaxed due to the shifting delay of the modulator loop filter of each stage to the its feedback path. The proposed Unity-STF SMASH architecture, which is realized with several efficient techniques, would be robust to circuit non-idealities such as finite op-amp DC gain. Furthermore the topology can be implemented by a fewer active blocks, suitable it for low power, high operation speed applications.

Keywords: sigma delta modulator, SMASH, Unity STF, low-distortion topology.

1. INTRODUCTION

Sigma-Delta Modulators (SDMs) are suitable for high-resolution applications because of their inherent immunity to circuit non-idealities [1]. Nowadays, there is an increasing demand for higher speed and resolution without any expanding the power consumption too much. Since Over-Sampling Ratio (OSR) must be reduced in wideband applications, the modulator's accuracy decreases. A usual choice to design a SDM for required performance is employing single-stage high-order architecture with a multi-bit quantizer in the loop filter of the modulator. However, it is prone to instability.

Another choice is Multi-Stage Noise-Shaping (MASH) SDM that circumvent the stability problem related to the high-order single-stage counterparts. However, MASH modulators are sensitive to quantization noise leakage caused by mismatches between the analog and digital signal processing blocks and therefore, they need higher op-amp gain to decrease this mismatch [2]. MASH modulators usually require integrators with higher accuracy than their single-stage counterparts to limit the noise leakage effect. However, the power consumption would be increased.

An alternative SDM architecture for MASH one's that reduces the sensitivity to noise leakage of conventional MASH modulators has been introduced in [3] and called Sturdy MASH (SMASH) SDM. In this topology, the digital error cancelation logic used in conventional MASH modulators replaces by the own analog noise filtering of the modulators stages and a digital summation block in the modulator output. In this method, the own analog filtering is achieved by feeding back the output of the second-stage to the first-stage output and subtract from it in digital domain [3].

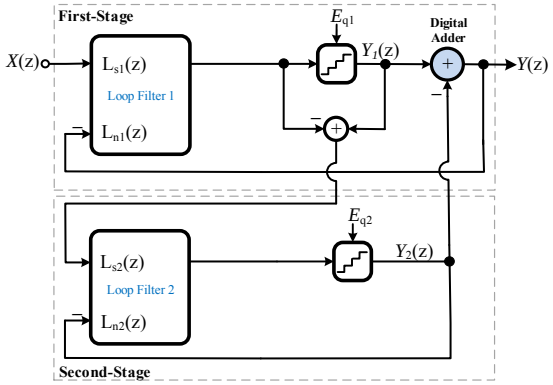
The advantage of this architecture are lower op-amp dc gain and less coefficient mismatching error. However, the main problem of SMASH modulator is that the quantization error of the first-stage is not cancelled completely at the modulator output and so degraded the Signal-to-Quantization Noise Ratio (SQNR). Unity Signal Transfer Function (Unity-STF) [4] and Delay-based noise cancelling SMASH [5] were introduced to cancelling the first-stage quantization error, but these structures have timing constraints in circuit implementation.

To overcome mentioned problem, a novel SMASH SDM is proposed in this paper to remove the first-stage quantization error from the modulator output and relax the critical timing in the feedback paths just by employing improved low-distortion topology in each stage. The conventional and proposed architecture is explained in next section. System level simulation and results are described in section 3 and Section 4 concludes the results.

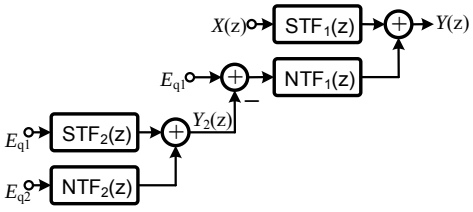
2. SYSTEM-LEVEL DESIGN DESCRIPTION

2.1 Conventional SMASH Architecture

Figure-1.a shows the conventional SMASH SDM architecture [3]. L_{si} and L_{ni} are the signal and noise loop filter of each stage, *i*.



(a)



(b)

Figure-1. a) Block diagram of conventional SMASH architecture [3] b) conceptual model.

Regarding to the conceptual model of the SMASH architecture, which illustrated in Figure-1.b, the SDM output is given by:

$$Y(z) = \mathrm{STF}_1.X(z) - \mathrm{NTF}_1.\mathrm{NTF}_2.E_{q2}(z) + \mathrm{NTF}_1(1\text{-}\mathrm{STF}_2)E_{q1}(z) \quad (1)$$

Where STFi and NTFi are the signal and noise transfer function of the stage *i* in the *Z*-Transform Domain respectively. Also E_{q1} and E_{q2} denote the first-stage and second-stage quantization error.

As mentioned in (1), the E_{q2} is filtered by overall NTF of the modulator similar to that given by MASH ones. However there is an extra term in (1) demonstrated that the first-stage quantization error, E_{q1} is not cancelled at the output, Y(z) but it is filtered by $\mathrm{NTF}_1(1\text{-}\mathrm{STF}_2)$. This increases noise power at the modulator output.

Selecting $\mathrm{NTF}_2=(1\text{-}\mathrm{STF}_2)$ causes E_{q1} can be shaped by the same order as E_{q2} was shaped. This means that the number of bits in the first-stage quantizer cannot be less than the second-stage in order to prevent performance degradation and stability margin of the modulator. It is possible to cancel E_{q1} at the output by choosing $\mathrm{STF}_2=1$ [4]. As shown in Figure-2, low-distortion architecture [2] with unity STF is applied to the each stage of the SMASH SDM. Therefore the modulator output become

$$Y(z) = X(z) - (1 - z^{-1})^4 E_{q2}(z) \quad (2)$$

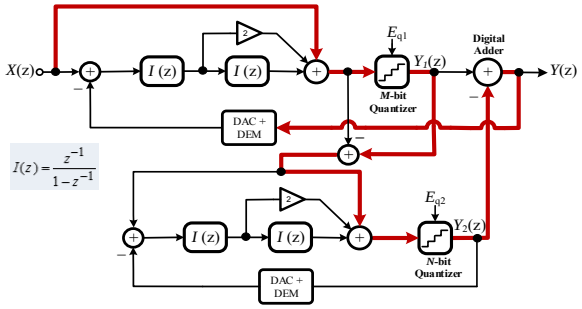


Figure-2. Block diagram of Unity-STF SMASH [4].

Note that conventional Low-distortion architecture, illustrated in Figure-3, causes reduction of the signal swing in the loop-filter blocks and reduces the required op-amp dc gain [2].

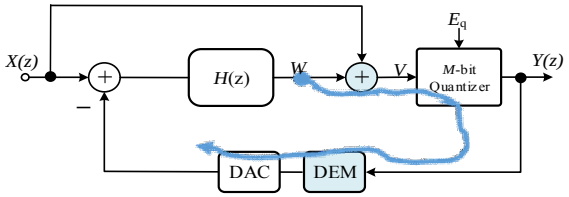


Figure-3. The conventional Low-distortion SDM topology [2].

For broadband applications, multi-bit quantizer is preferred to compensate the OSR reduction. The DAC block in the global feedback path of the modulator requires a dynamic element matching (DEM) algorithm, because the Multi-bit DACs have a nonlinear behavior. Therefore, the processing time available for DAC linearization is reduced (the delay free path shown in Figure-3). Another major issue related to low-distortion topology is the need of the adder at the quantizer input which often implemented by a delay-free power-hungry active block. Thus, the *N*-order low-distortion SDM needs *N*+1 active block. This block, also, restricts the conversion speed of the quantizer [7].

The Unity-STF SMASH SDM provides similar noise shaping to that of a conventional MASH SDM. Equation (2) confirms the above sentence. This topology also preserves the features of the SMASH modulators likes robustness to the noise leakage and low output swing and gain of the amplifiers. However, it may not practically be feasible to extract E_{q1}, feed it to the second stage for processing and subtract the second stage output from the first-stage without any delay [5]. The bold line in Figure-2 highlights the critical delay-free path.

Modifying the second-stage of the modulator in Figure-2 to a non-Unity-STF with a delay in the critical path has been selected as a solution in [6]. Referring to that, the benefit of Unity-STF is ignored to compensate the mentioned problem. But the E_{q1} is appeared at the output of the modulator.

Delay-based noise cancelling SMASH architecture, which introduced in [5], is another solution

for cancelling the E_{q1}. To do this, a unit-delay block has been added to the output of the first-stage quantizer. So, the overall output of the modulator, Y(z), for a DNC S-MASH 2-2 topology that illustrated in Figure-4 obtain by:

$$Y(z) = z^{-1}\ \mathrm{STF}_1.X(z) - \mathrm{NTF}_1.\mathrm{NTF}_2.E_{q2}(z) + (z^{-1}\ \mathrm{NTF}_1 - \mathrm{STF}_2(1-\mathrm{STF}_1))\,E_{q1}(z) \quad (3)$$

For cancelling the E_{q1} at the output, STF_1 and STF_2 must be chosen as follow:

$$\mathrm{STF}_1 = 1 - \mathrm{NTF}_1,\ \mathrm{STF}_2 = z^{-1} \quad (4)$$

Although the E_{q1} cancelling is achieved at the modulator output by considering (4), however this method restricts the STF and NTF selection especially for the first-stage architecture. In addition, any stage of the SDM cannot employ the Unity-STF architecture.

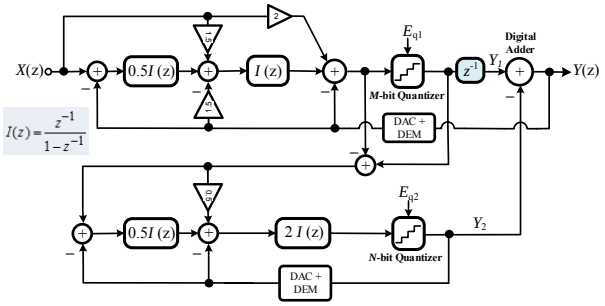


Figure-4. Block diagram of DNC SMASH 2-2 SDM [5].

2.2 Proposed SMASH Architecture

To alleviate the mentioned problem associated with cancelling E_{q1} and timing signal processing in the critical path, an improved Unity-STF SMASH2-2 SDM is proposed in Figure-5. The SDM topology uses low-distortion second-order architecture in both stages. A shifted loop delay technique [7], which moves the last integrator delay to the feedback path, is applied to each stage. This relaxes the DAC and DEM signal processing timing in the feedback path. The bold line in Figure-5 highlights the critical path, which has a unit-delay before DAC-DEM block.

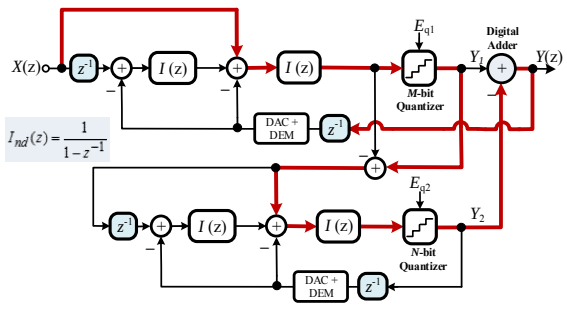


Figure-5. Block diagram of proposed unity-STF SMASH 2-2 ΣΔM topology.

Also, to preserve the low-distortion property for each stage of the proposed SDM, the analog adder block in front of the quantizer is moved to the input of last integrator with an extra feedback path in the modulator loop. Therefore, any stage of the proposed SDM needs only two active blocks. It means that the active blocks of each stage are reduced by one.

The proposed SDM, which names improved-Unity-STF SMASH, circumvents the drawbacks of the conventional unity-STF SMASH [4, 8] and preserves features of implementing unity-STF such as relaxed output swing of the loop-filter integrators and overload level of the modulator input. Most importantly, the digital adder and DEM-DAC blocks in the first-stage of the modulator have enough time for signal processing. Therefore, the bandwidth of the sigma-delta modulator can be increased. The modulator output in Figure-5 can be shown at z-domain transform as follow:

$$Y(z) = X(z) - \frac{1}{d}(1-z^{-1})^4 E_{q2}(z) \quad (5)$$

Where $X(z)$ and E_{q2} are input signal and second-stage quantization error respectively. Note that the first-stage quantization error E_{q1} is cancelled and hence the first-stage quantizer can be implemented simpler, with fewer output bit, unlike traditional SMASH architectures [5]. Furthermore, the number of active blocks in the proposed unity-STF SMASH 2-2 is reduced two units contrary to the conventional unity-STF SMASH 2-2 [4], which results into lower area and power consumption. Also In (3), if scaling factor d is considered as a power of 2, the quantization noise power of E_{q2} will be reduced more at the modulator output.

3. SIMULATION RESULTS

The improved unity-STF SMASH 2-2 ΣΔM shown in Figure-5 along with the traditional MASH and SMASH 2-2 [3], unity-STF SMASH 2-2 [4] and Delay-Based Noise-canceling SMASH [5] ΣΔMs are simulated using MATLAB and Simulink [9]. For all architectures, the number of quantization bits for first and second stages are 4. The assumed OSR is 16. The simulated signal-to-noise and distortion ratio (SNDR) is shown in Figure-6 against the input level when considering the ideal situations. Note that the overload level of the proposed ΣΔM is larger than all architectures except Delay-Based Noise-canceling SMASH one however; it achieves a larger SNDR or resolution because of low-distortion architecture implementation.

Figure-7 shows the op-amp dc gain requirement of the integrators for a -6 dBFS input level in the above-mentioned structures. To achieve a 90 dB SNDR, the required op-amp dc gain in the traditional MASH, SMASH and Delay-Based Noise-canceling and unity-STF SMASH 2-2 are about 45, 40, 35 and 20 dB respectively. For the improved unity-STF SMASH, this value is about 18 dB. Note that these values have been obtained by considering the other parameters ideal.

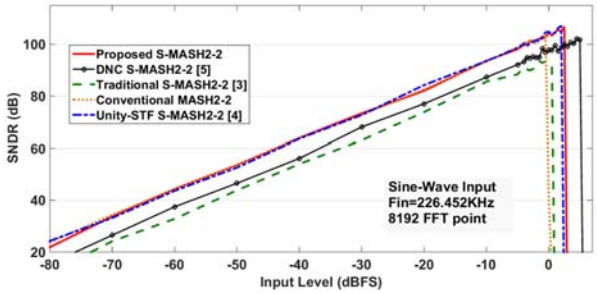


Figure-6. SNDR against input level.

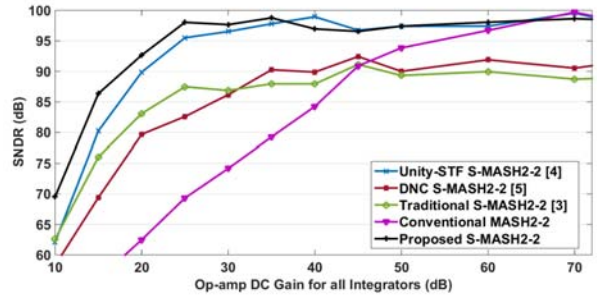


Figure-7. SNDR against Op-amp DC gain for all integrators.

Figure-8 shows the output power spectrum density (PSD) of the proposed SDM with input signal amplitude -6 dBFS and input frequency fin=195.31KHz. The Sampling frequency is 64MS/s. For the ideal conditions and considering the finite Op-amp DC gain, the SNDR of the modulator are 99 dB and 91.4dB respectively.

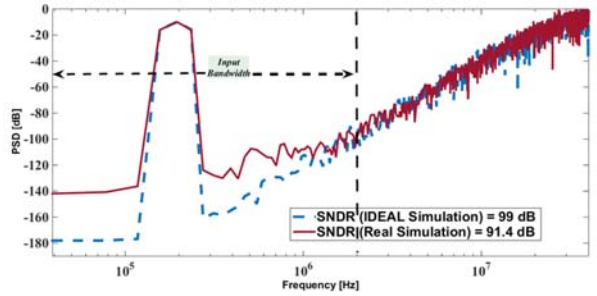


Figure-8. The output Power Spectrum Density for the ideal conditions and considering finite Op-amp DC gain (20 dB) in the modulator.

The sensitivity to circuit non-idealities due to mismatching, has been studied for a 50-run Monte-Carlo simulation by considering a standard deviation of 0.5% mismatch in all capacitors. Figure-9 illustrates the SNDR for capacitor mismatching up to 0.5 percent deviation. This simulation shows that the proposed modulator performance is not sensitive against capacitor mismatch non-idealities and totally, it has 3-dB performance degradation in return for maximum capacitor mismatching. The results show that the proposed unity-STF SMASH architecture obtains the same sensitivity like the conventional unity-STF SMASH one.

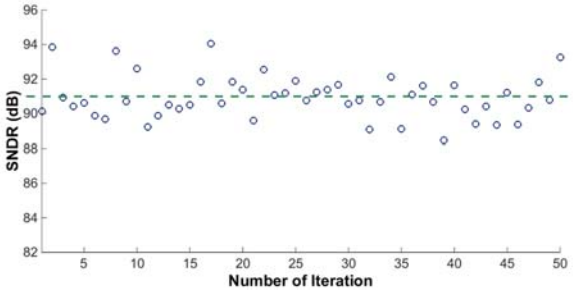


Figure-9. The Monte-Carlo analysis for capacitor mismatch.

To investigate the stability problem of each architecture, the levels of the first-stage quantizer have been varied from two to 16 in system level simulation. Although the E_{q1} is cancelled at the modulator output, but decreasing the quantizer-level has a significant effect on the stability issue of the loop-filter of the modulator. Moreover, the quantization noise power in the loop-filter of the first-stage is increased, so the probability of saturation in the output swing of the integrators is enhanced. Therefore, the stability margin is reduced.

The SNDR versus first-stage quantizer-level is illustrated in Figure-10. This shows that the proposed SMASH and Delay-Based Noise-canceling SMASH [5] architectures have a good stability response. However, for the same conditions, the proposed SMASH have a better SNDR performance. Lowering the quantizer-level of the traditional SMASH is expected to decrease the SNDR, because the E_{q1} in not cancelled at the output of the modulator.

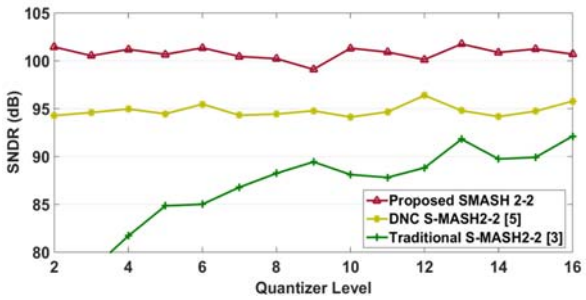


Figure-10. The SNDR versus first-stage quantizer-level.

By modeling each of circuit non-idealities, as descripted in [9], the proposed SMASH2-2 sigma delta modulator has been simulated at behavioral level. Table-1 shows the effects of these non-idealities on the SNDR individually. The result of SNDR is 89.4 dB including all of the non-idealities shown in Table-1. In these simulations, the input signal is a 195.31 kHz, -4 dBFS sinusoidal waveform.

Table-1. Circuit non-idealities of the SMASH sigma delta modulator.

Loop-filter non-idealities	**SNDR** (dB)
Ideal case	99
Switches thermal noise (*Cs*=1.5 pF@ first integrator)	91
Input referred op-amp thermal noise (Vn=7μVrms)	97
Capacitor mismatching (0.5% Max.)	92.4
Finite dc gain of all integrator (A_0=20 dB)	91.4
Slow Rate (SR=200 V/us)	95.6
Unity-Gain Bandwidth (UGBW=400MHz)	96
DAC nonlinearity	96.7
Including all of non-idealities	89.4

Regarding the simulation results, the proposed topology has a better stability than conventional SMASHs, lower op-amp DC gain and simplicity of the circuit implementation [10]. Practically it can be a good candidate for low-power and broadband application compared to conventional structures like unity-STF SMASH.

CONCLUSIONS

In this paper, a new topology of the SMASH ΣΔM is presented and simulated. By applying improved low-distortion architecture in both stages of the modulator, the first-stage quantization error at the modulator output is removed. The proposed Unity-STF SMASH architecture would be robust to circuit non-idealities such as finite op-amp DC gain. In addition, the processing timing issue in the critical paths of the proposed architecture has been relaxed due to shifting the delay of the modulator loop filter to its feedback path. Moreover, the modulator has enough time to extract quantization error of the first-stage (E_{q1}), processes it in the second-stage and finally delivers to the first-stage for filtering and cancelling at the modulator output. Behavioral simulations show that the proposed architecture capable to achieve larger SNDR at a lower op-amp gain requirement. This makes the proposed unity-STF SMASH architecture suitable for low-power and broadband applications.

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