VOL. 12, NO. 17, SEPTEMBER 2017 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

DESIGN AND ANALYSIS OF NOVEL HIGH PERFORMANCE CMOS DOMINO-LOGIC FOR HIGH SPEED APPLICATIONS

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ABSTRACT

Dynamic logic style is popular due to its fast processing speed and less power dissipation in high performance circuit design as compared to static complementary metal-oxide-semiconductor (CMOS) logic style. However, dynamic logic has less noise tolerance and charge sharing problems and hence it is not widely accepted for all high speed applications. As a consequence, a domino logic circuit is proposed for applications such as high-speed adder, comparator and arithmetic and logic unit (ALU) design. Furthermore, the proposed domino logic circuit provides multi standard advantages such as less propagation delay, less power dissipation and high fan out capability. The proposed circuit is simulated and tested in T SPICE with 45 nm technology. Moreover, it is compared with other domino logic circuits in terms of power dissipation and propagation delay.

Keywords: dynamic logic, CMOS logic, ALU processor, high fans out.

1. INTRODUCTION

It is well known that static logic is having features such as very low static power dissipation, high noise margins, low output impedance, high input impedance and comparable rise and fall times. Conversely, static CMOS is better energy-efficient and robust but it is very slow to be used in critical and massive designs. Due to these aforesaid issues, we consider the dynamic logic functions for high speed application like digital signal processor (DSP) processor, high speed adder, comparator, ALU reconfigurable processor and real-time operation associated with internet of things (IOT) applications. Moreover, dynamic CMOS logic circuit [1, 2] provides more advantages such as free from output glitch and small parasitic capacitance as compared to static logic circuit.

Moreover, the dynamic logic circuit contains a pull-down network (PDN), which is utilized for desired logic functions. Conversely, the dynamic logic circuit will pre-charge at every clock cycle due to this pre-charging operation dynamic logic circuit produces some extra amount power dissipation [3, 4]. When very high frequency signal is applied to circuit, it introduces a lot of noise and consumes some extra power, as a result of which circuit gets slow down [5, 6]. Additionally, dynamic logic circuits are more sensitive to noise and produce timing errors during its operating time [7]. Similarly, domino logic is affected by charge sharing problems [8], which are occurred due to some charge stored at the output node during the pre-charge phase and are shared among the junction capacitance of transistors during the evaluation phase [9].

In this paper, novel high performance domino logic has been implemented for footed logic circuit. Using this logic, unwanted pulses at the dynamic node are generated during pre-charge period and are prevented to pass to the output node as in conventional case. As a consequence, more power is saved in the proposed approaches compared to other domino gates presented in literatures [10, 11]. This logic is again modified using keeper and some footer transistors to get a better power-efficient, robust and high speed logic. This logic circuit can be employed for an extensive limit of logic gates. The proposed logic is analyzed with T SPICE with 45 nm technology and compared with the same circuit designed using other logic styles.

2. RELATED WORKS

This section discusses about the implementation of different domino logic styles. Figure-1 illustrates a standard domino logic style for OR gate. When the applied clock pulse is low, the output node will be pre-charged to VDD through the PMOS transistor and this is defined as the pre-charge phase.

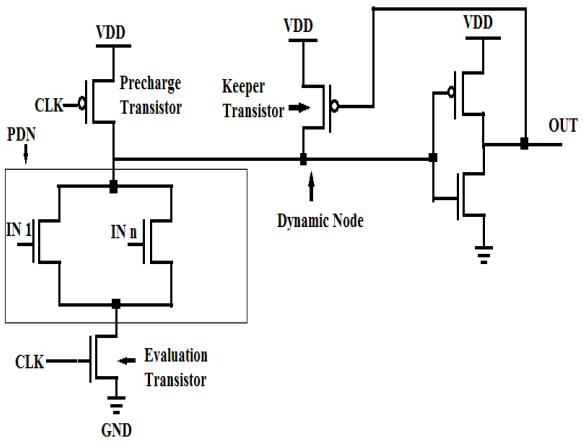


Figure-1. Standard domino OR gate.

Similarly, when the clock pulse is high, the evaluation transistor will be ON and the pre-charge transistor will be OFF. However, during the evaluation phase, when clock pulse goes high the keeper transistor will be maintained at logic high and due to that there will be charge leakage in the PDN. Additionally, in the evaluation phase the dynamic node is turned to be discharged through the PDN and the evaluation transistor.

Accordingly, the output inverter tends to switch between zero as well as one and the keeper transistor tends to turn OFF. Thus, there will be static power dissipation from the VDD to Gnd.

Figure-2 represents the diode footed domino [12]. The footed transistor is an NMOS transistor (M3), which is connected in the PDN by applying clock pulse to its gate and the drain of this transistor is connected to the M1 transistor.

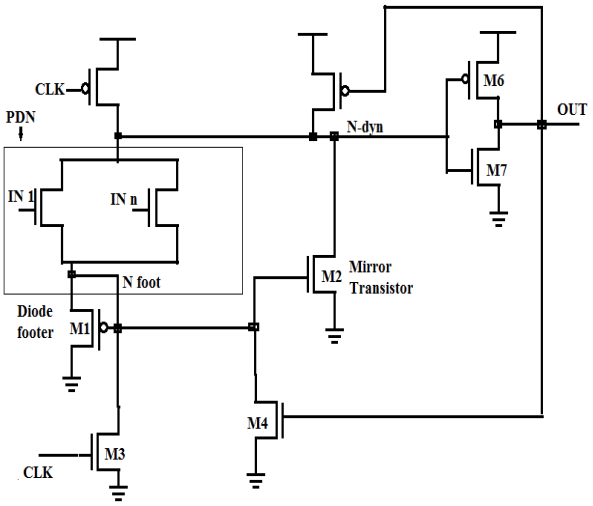


Figure-2. Diode footed domino logic.

This design expands the leakage immunity by considering the footed transistor in the diode design technique and then enhances the performance by utilizing the current mirror technique in the network. The current mirror circuit is designed as a replica of current through one device by managing the current in the other device, while the output current is kept constant without considering the loading. The replica of current from one device can be a signal varying current. The voltage drop across the diode footed transistor is because of the leakage in the evaluation phase. The voltage drop across the diode footed transistor forms the gate to source voltage of the OFF evaluation transistor as negative creating the scale down of the sub-threshold leakage current. However, this costs the performance breakdown. This can be stable by utilizing the mirror transistor. The use of this mirror transistor is to reflect the evaluation current. Hence it develops the performance by the draining current out of the dynamic node.

Figure-3 represents one of the domino styles. This circuit technique had been proposed in [13]. During the start of the evaluation phase, the node C is considered to be at zero volts. The increment in the sub-threshold current increases the charge of the node C. During this procedure, the gate to source voltage of the dynamic NMOS reduces and the sub-threshold leakage current also decreases exponentially.

Figure-4 represents the proposed domino circuit scheme in [14]. In this circuit, M1 transistor is considered in the form of diode. The gate to source voltage in the pull down network of the NMOS transistor decreases (stacking effect [15]), because of the voltage drop across the M1 transistor. Due to the additional evaluation of M5 transistor with gate connected to clock, the proposed circuit acts differently from the diode footed domino circuit [12].

The presence of the noise signal across M1 transistor causes voltage drop and the M2 transistor starts leaking that causes the power dissipation of the circuit. M5 transistor in this proposed design circuit causes the stacking effect and forms the gate to source voltage of M2 transistor less conductive. This leads to the reduction in the leakage of the power consumption. Due to the stacking effect in the mirror current path, the performance of the circuit degrades. The performance of the circuit is increased through making M2 transistor more conductive.

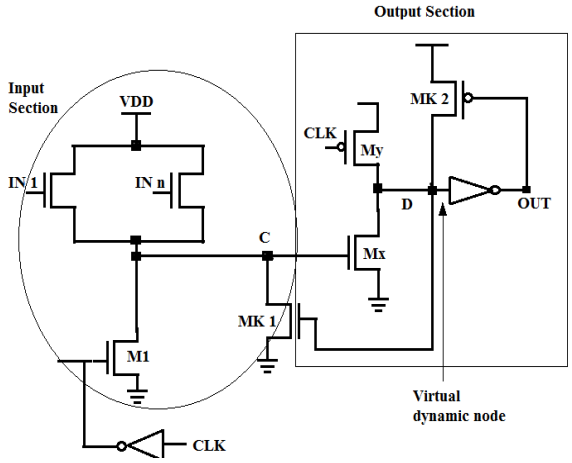


Figure-3. Domino style proposed in [13].

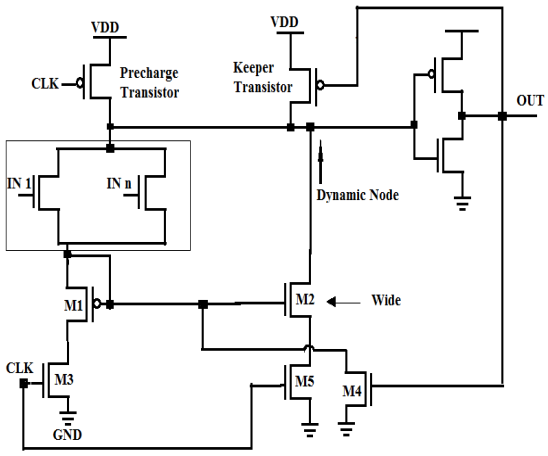


Figure-4. Domino circuit proposed in [1].

3. PROPOSED DESIGN

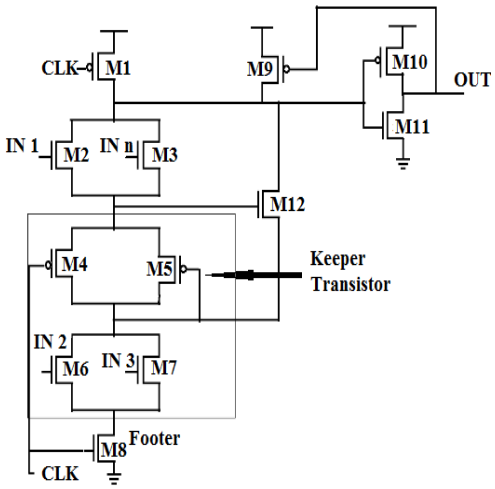


Figure-5. Proposed domino design.

The proposed domino circuit is shown in Figure-5. The M1 transistor is discarded in this figure when compared with the recent proposed circuit [14] and it is replaced by the two parallel NMOS and PMOS transistors [16]. In this proposed domino circuit, M5 transistor is also discarded and due to which there is no stacking effect (i.e. no change in the voltage at the source of the transistor). The proposed circuit alters from the other recent proposals with an additional of two parallel NMOS and PMOS transistors.

As different types of unwanted capacitors are associated with input node, output node and interconnection point of the circuit, the operating point of the circuit is dependent on the charging and discharging rate of above capacitors. The additional parallel combinations of NMOS and PMOS can enhance the charging and discharging rate of capacitor current as well as increase the current carrying capability of circuit. The PMOS transistor dissipates the power in low output state. If the CMOS gate switches faster the more power it dissipates, so there will be a trade-off between the speed and power. The CMOS gate only dissipates power when it is in changing state. As there is no M1 transistor, there is no voltage drop across it. Hence the proposed circuit consumes less leakage power and has less delay when compared with the recent proposed designs. The size of M2 transistor can be widened for more conduction.

4. SIMULATION RESULTS AND ANALYSIS

The circuits are implemented using tanner tools T-SPICE in 45 nm technology. The width and the length of the transistors are considered as 2.5um and 0.25um respectively. The supply voltage Vdd is taken as 1 V. The simulations have been performed using different domino logic circuits along with the proposed one and are compared with consideration of parameters such as delay and power.

Table-1. Comparison of power and delay of different domino styles along with the proposed design.

Designs	Power in watts	Delay
Standard domino OR gate	power consumed -> 5.151321e-009	5.6122ps
Diode footed domino	power consumed -> 1.628913e-008	3.2906ps
Domino style [5]	power consumed -> 2.678991e-008	4.1385ps
Domino scheme [1]	power consumed -> 3.183036e-008	2.5086ps
Proposed design	power consumed -> 1.910957e-008	1.8875ps

The keeper transistor will maintain the logic high when the clock goes high, i.e. in the evaluation phase throughout all the circuits. Figure-6(a) describes about the delay where x axis is taken as time (picoseconds) and y axis as volts (mv). From 0ps it reaches the 0.7mv and then decreases to 66ps of the standard domino OR gate and figure 6(b) describes about the power dissipation where x axis is taken as time (Pico seconds) and y axis as power (mw). It is observed from the figure that initially the power is fluctuating up to 0.78ps. Then the power starts to increase at 0.8psandbecomes steady at 10ps.

Figure-7(a) describes about the delay where x axis is taken as time (Pico seconds) and y axis as volts (mv). From 0ps it reaches towards 0.62mv and then decreases towards 30ps of the diode footed domino. Figure 7(b) describes about the power where x axis is taken as time (Pico seconds) and y axis as volts (mw). Similarly, at 0ps power is fluctuating because of transient behaviour of circuit and from 10ps it starts triggering. However, it reaches steady-state point after 70ps. Figure-8(a) describes about the delay where x axis is taken as time (Pico seconds) and y axis as volts (mv). From 0ps it reaches towards 0.58mv and then decreases towards 50ps and finally it is kept constant [5]. Figure-8(b) describes about the power where x axis is taken as time (picoseconds) and y axis as volts (mw).Some oscillations are existing at the initial stage as seen through the figure. It is also shown that the triggering action has been started from 10ps and steady state point is achieved at 80ps.

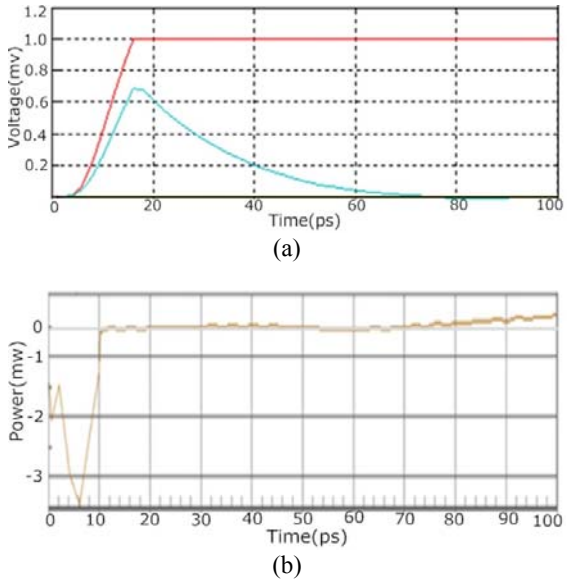


Figure-6. (a) Delay output and (b) Power waveform of standard domino OR gate.

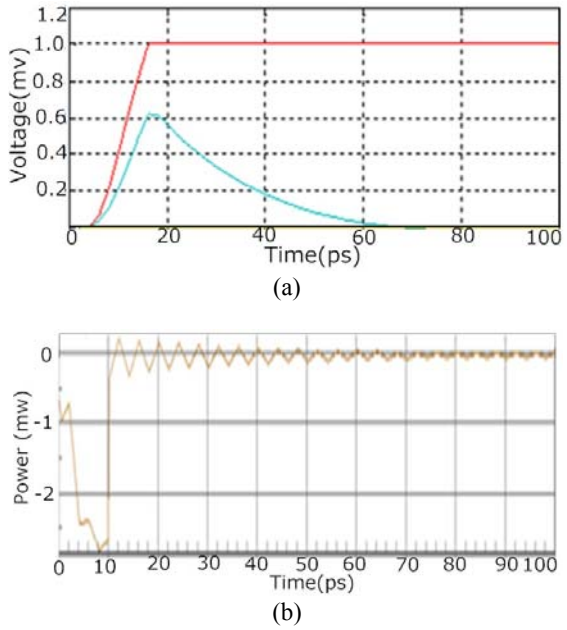


Figure-7. (a) Delay output and (b) Power output waveform of diode footed domino [4].

Figure-9(a) describes about the delay where the x axis is taken as time (picoseconds) and the y axis as volts (mv). From 0ps it reaches towards 0.68mv and then decreases towards 35ps and later becomes constant [1]. Figure-9(b) describes about the power where x axis is taken as time (picoseconds) and y axis as volts (mw). From the figure, it can be noted that some power oscillations are produced at initial stage. Moreover, it is seen that triggering action has been started from 10ps and steady state point is attained at 70ps.

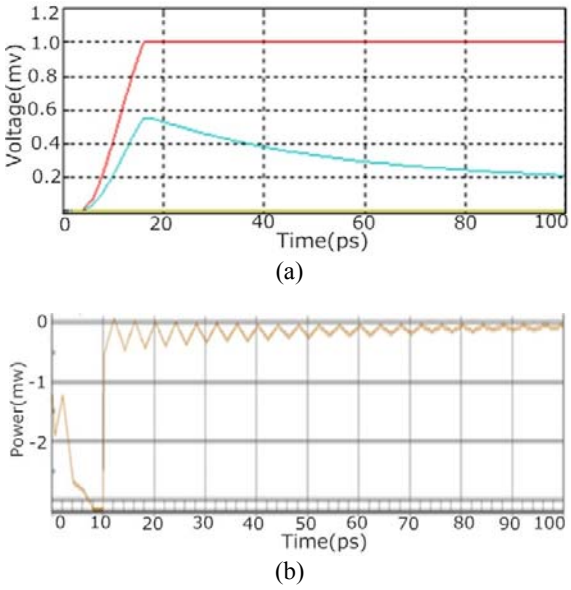


Figure-8. (a) Delay output and (b) Power output of domino style proposed in [5].

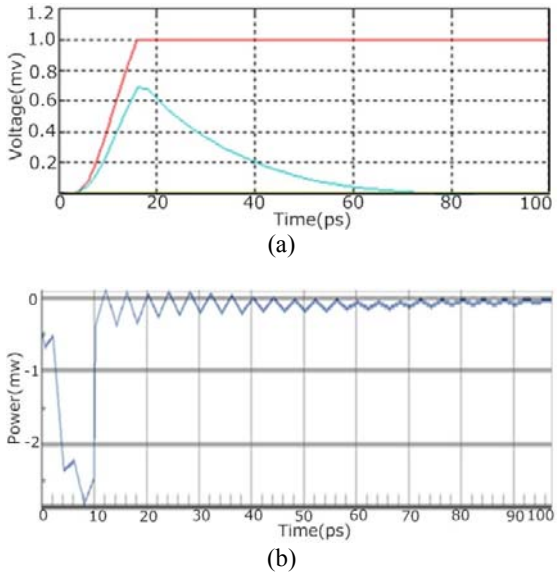
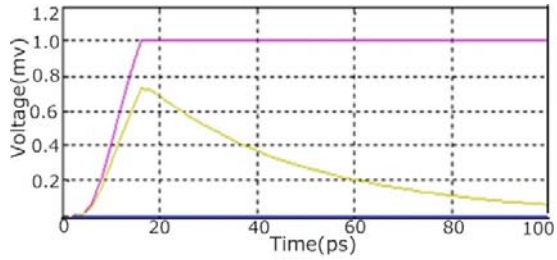


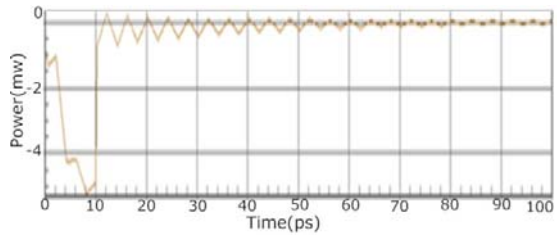
Figure-9. (a) Delay output and (b) Power output of proposed circuit scheme [1].

Figure-10(a) describes about the delay where x axis is taken as time (picoseconds) and y axis as volts (mv). From 0ps it reaches towards 0.76mv and then decreases towards 50ps of the proposed diode footed domino logic. Figure-10(b) designates the power where x axis is taken as time (picoseconds) and y axis as volts (mw). It is analyzed from the figure that at initial stage some power oscillations are created. Then, triggering action is established at 10ps and steady state value is realized at 50ps. The proposed design in this paper has provided better results with the power and delay parameters when compared with the prior works. Table-1 shows the power and delay measurements for the various

domino styles. The delay is sequentially decreased when compared with the proposed design because of the high fan-out.



(a)



(b)

Figure-10. (a) Delay output and (b) Power output of proposed design.

5. CONCLUSIONS

In this paper, we have presented and validated a novel CMOS domino-logic circuit, which is provided with less power dissipation, less propagation delay and high fan out capability. Over an extensive view of design facts, this proposed logic is excellent as compared to domino and static CMOS logic and also some latest specific logic styles on a basis of power and delay measurement. At the same time, it is more robust than all logic styles. The proposed domino logic is implemented using the T-SPICE.It is explored from the results that almost 50 to 80% of power reduction is achieved in the proposed approach as compared to conventional domino logic and also a reduction of40 to 60% of delay is attained in the proposed one as compared with static CMOS. As a consequence, this proposed logic design is efficient for the low power applications such as high-speed adder, comparator and ALU design.

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