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A COMPETENT REVERSIBLE LOGIC SIPO SERIAL TO PARALLEL CONVERTER IN QCA TECHNOLOGY

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ABSTRACT

A reversible logic based serial to parallel converter is developed using Quantum cellular automata (QCA). Nowadays reversible logic is a vital area of research due to its aptness to reduce the power dissipation and circuit complexity. The output functions uniquely expound by the input logical states in reversible logical functions. The foremost aim of designing the reversible circuits are to reduce the number of gates, number of garbage outputs, delay, quantum cost, number of quantum cells and device complexity. The reversible logic circuits do not fail to keep the information and unique types of outputs are taken. In this paper a proposed new 4*4 reversible gate is designed using quantum cellular automata and it is being used to realize the D Flip Flop with reduced number of quantum cells. Also a 4 bit reversible SIPO serial to parallel converter has been realized using the proposed D Flip Flop. It uses reduced number of gates and quantum cells so it occupies less area.

Keywords: reversible logic, serial to parallel converter, CMOS, QCA.

1. INTRODUCTION

The quantum-dot cellular automaton (QCA) is a representation which is inspiring not only for its simple and formal view of structure, but also for its "physical" impression. Quantum dot cellular automata can shack light on the performance of physical systems, because they were attracted physically, and they hold the hope of providing outstanding physical implementation of quantum computation.

Reversible logics were the leading cause for increasing desire for the lower power devices. The normal logic gates such as AND, OR and EXOR are irreversible because they have multiple input value and we can get single output. Reversible logic has a one to one mapping between its inputs and their corresponding outputs [6]. Thus there may be no information loss during the computation process. A reversible logic gates must have equal number of inputs and their respected outputs, and there must be a unique set of output pattern that is generated from each input values, they will not be repeated [8]. In a n*n reversible gate function, the input number is equal to the no of output values that we get. The unused outputs are kept to maintain the reversibility of circuits that are known as garbage output values. In QCA synthesis technique, using a reversible gate and they should have the features like reduced number of cells, less use of constants and garbage generation. Reduction of area is the desired design focus.

Reduction of the area is an essential goal in the VLSI circuit design. The normal gates that designed produce more energy loss, it occupies more area due to the information lose and large cells during the design process. To avoid power dissipation and circuit complexity, reversible logic gate circuits must be designed in QCA with reduced number of cells. Future technology has to move with reversible gates with QCA in order to reduce area.

2. QUANTUM CELLULAR AUTOMATA

QCA not only utilized by the shifting of electrons, also by the adjustment of electrons in a small cell in a finite area of few square in nanometer size. Quantum cellular automata are implemented by quadratic cells, named as QCA cells. In the small squares, exactly four potential wells are places, one in each corners of the QCA cell shown in Figure-1. In a QCA cell, exactly two electrons are placed in the potential wells, and connected with the electron tunneling junction. They will be opened and closed under a particular condition for the electrons to travel through them, by a clock signal. The two electrons will try to separate from each other as far as possible, without any interaction from outside. The diagonal is the largest possible distance for them to reside so they will reside diagonally in the potential wells. Commonly in a square there are two diagonals, which means the electrons can reside in any of the two possible locations in the QCA cell [6]. Based on these two arrangements, they can be interpreted as a binary '0' and binary '1'. Each cell can be of in two states that is the state '0' and the state '1', as shown in Figure-2. As Boolean logic familiarly used in today's computer logics a high voltage is interpreted as binary '1' and a low voltage as binary '0'.

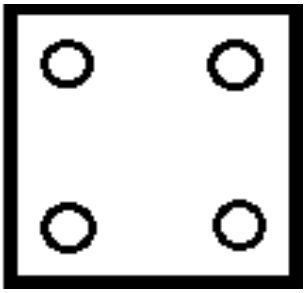


Figure-1. Structure of QCA cell.

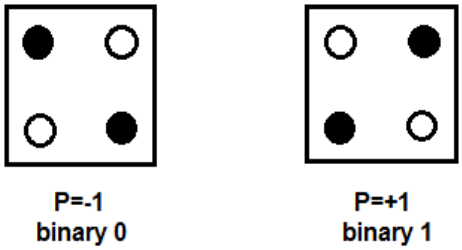
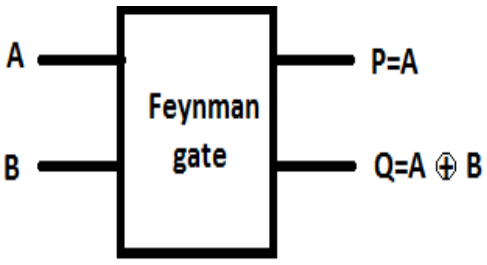


Figure-2. State '0' and the State '1' in QCA.

In order to propagate a QCA signal accurately, synchronization and energy restoration are essential which are obtained by applying a specific four-phased clocking scheme. Every QCA cell get polarized by the effects of adjacent cells during the two phases like Switch phase, and Hold phase. In order to maintain its polarization inter-dot barriers are raised to the maximum height. In the release phase, by losing its polarity the cell moves to un-polarized state by the reduction in the inter-dot barrier. Finally, in the Relax phase, the cell is un-polarized with negligible barrier. Because of the QCA synchronization issues, number of cells in a clock zone or synchronized flows arriving to a gate, must be considered during the design of a QCA-based circuit. Each QCA clock zone consists of at least two cells to preserve its influence on the subsequent clock zone.

3. REVERSIBLE LOGIC GATES IN QCA

In reversible operations reversible gates has been used in. It has equal number of inputs and outputs [4]. Some reversible Gates like Feynman gate, fredkin gate, toffoli gate, peres gate are used in many operations [6]. They are shown in Figures 3a to 3d. With their simulated design.



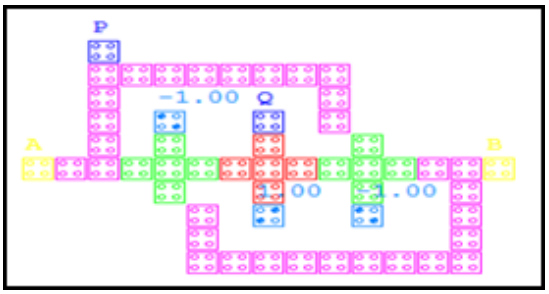
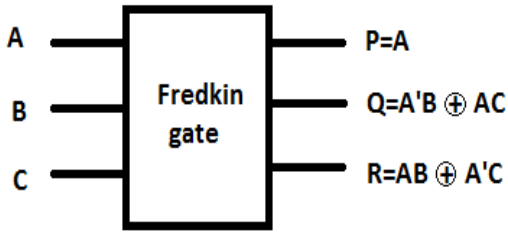


Figure-3(a). Feynman gate.



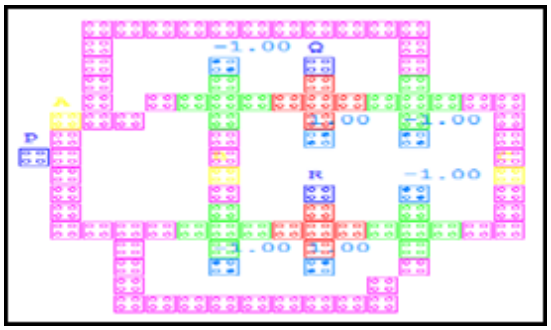
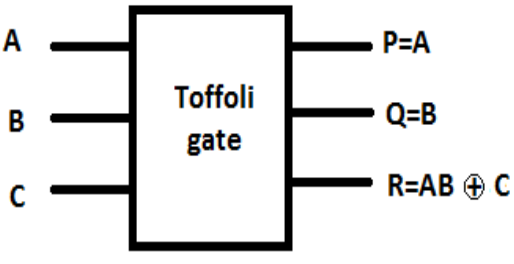


Figure-3(b). Fredkin gate.



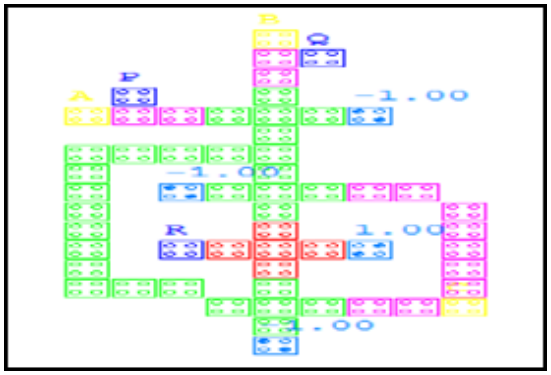
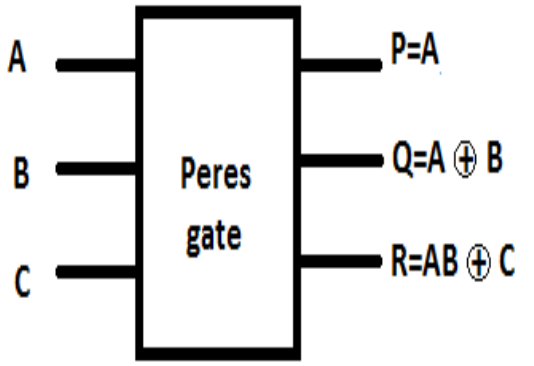


Figure-3(c). Toffoli gate.



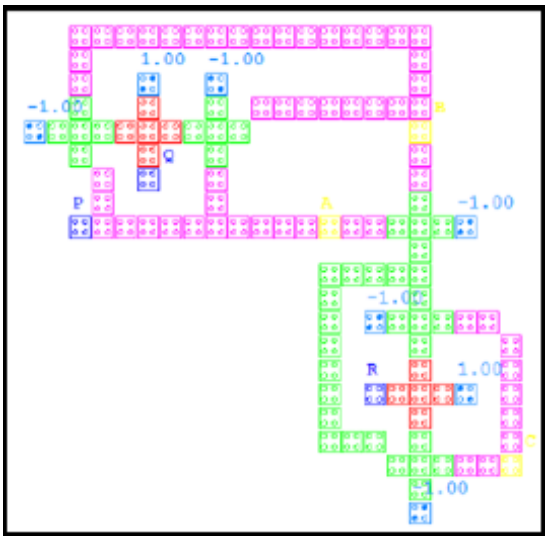


Figure-3(d). Peres gate.

4. PROPOSED REVERSIBLE GATE IN QCA

In this paper a new 4*4 reversible gate is formed and simulated in QCA. The inputs are given as (A,B,C,D) and output functions as (P,Q,R,S) which can be represented as P=A, Q=B', R=C(A+B)+A'B'C', S=A'B'D+(A+B)D'. The JR reversible gate with its QCA design (Figure 4a and 4b) and its truth table is tabulated in Table-1. The output functions can be verified using the truth table. This reversible gate is simulated in Quantum cellular automata.

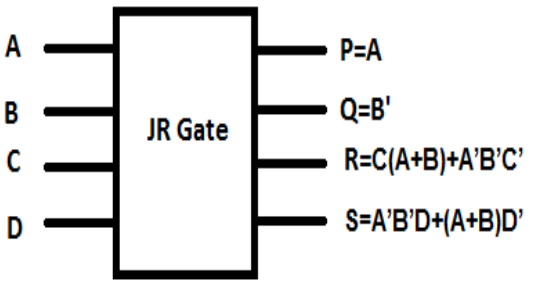


Figure-4(a). Proposed reversible JR gate.

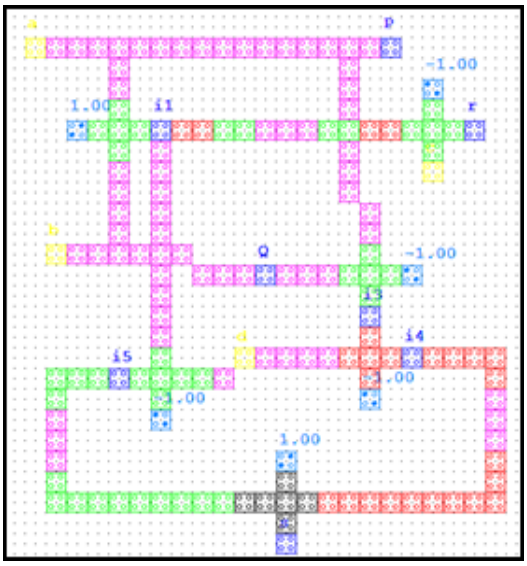


Figure-4(b). Proposed reversible JR gate in QCA.

Table-1. Truth table of proposed reversible JR gate.

A	B	C	D	P	Q	R	S
0	0	0	0	0	1	1	0
0	0	0	1	0	1	1	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

5. D-FLIP FLOP USING PROPOSED REVERSIBLE JR GATE IN QCA

In this section, the realization and simulated design of D-flip flop by proposed JR reversible gate is discussed. For this two Feynman gate is attached with the proposed JR gate to make the gate behave as the D-flipflop. This can be combined as shown in Figure-5.

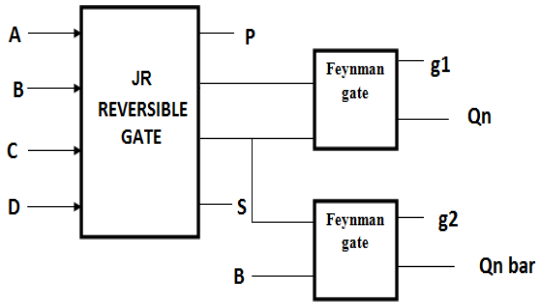


Figure-5. Proposed JR reversible gate based D-flip flop.

Table-2. Truth table of D Flip Flop.

Clk	D	Qn	Qn bar
0	0	0	1
0	1	1	0
1	0	0	1
1	1	1	0

In this realization JR gate is connected with 2 feynman gate. The input B of the JR gate acts as the clock value and the input value C acts as the D(delay) value. The output values Qn and Qn bar are observed. Other outputs are marked as garbage outputs. The garbage values are not used further. This can be checked by the truth Table tabulated in table 2 and its simulated QCA structure shown in Figure-6.

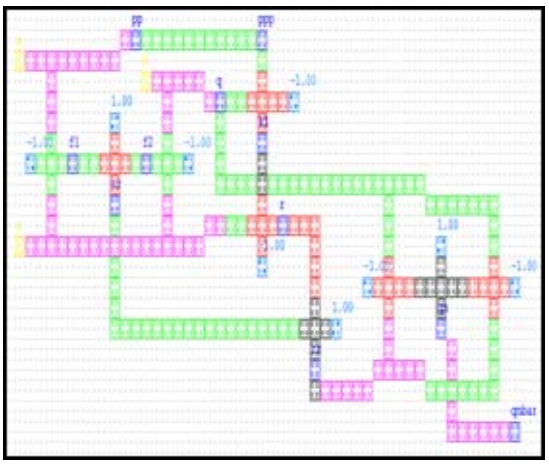


Figure-(6). D flip flop using JR gate in QCA.

6. SIPO USING PROPOSED REVERSIBLE JR GATE IN QCA

JR gate and Feynman gate is connected in series to form serial to parallel converter (shown Figure-7a). The input B act as the common clock for all the block and the input C(0) acts as the D(delay) value. This D value (i.e. c(0)) moves serially to each block and gives the required output. The output Qn and Qn bar values are observed and verified by the simulated design and output waveform.

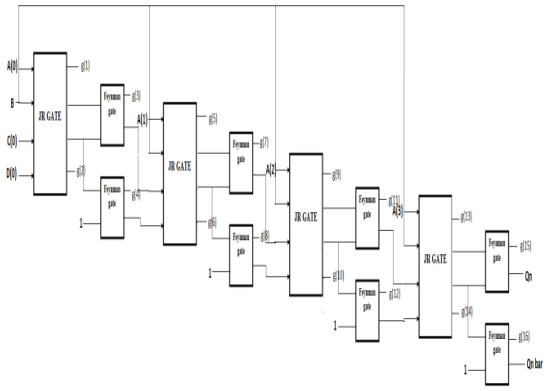


Figure-7(a). Proposed SIPO using reversible JR gate.

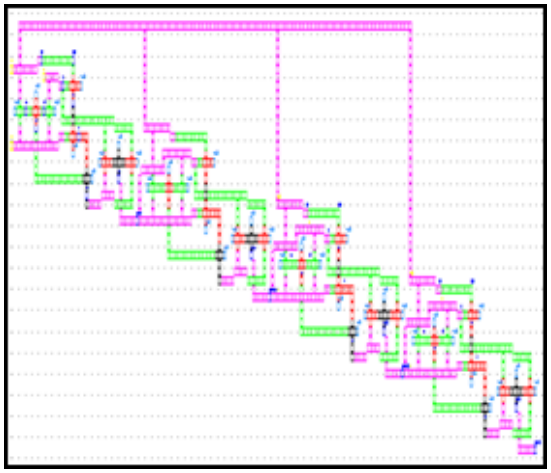


Figure-7(b). SIPO using Reversible JR gate in QCA.

The simulated design of the above circuit IN QCA is shown below in Figure-7b. It shows the serial to parallel converter operation with reversible gates. In this design reduced number of cells is used to form the serial to parallel converter.

7. RESULTS AND DISCUSSIONS

The simulation design of reversible JR gate in QCA is done and by this JR gate D Flip Flop and SIPO serial to parallel converter are developed. This simulation process is done by QCA designer tool 13.1 software.

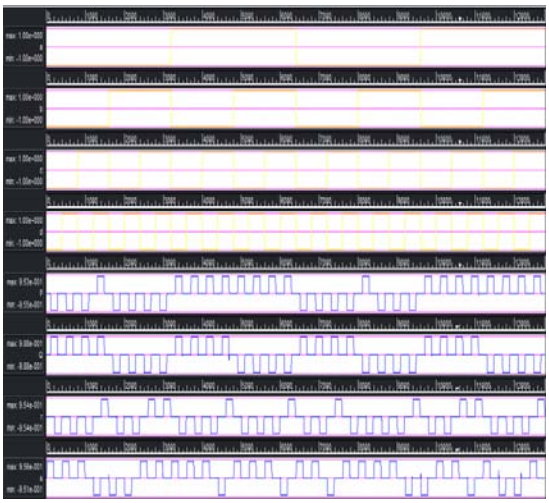


Figure-8. Output waveform of proposed reversible JR gate.

The simulated output waveform of reversible JR gate is shown in Figure-8, in this reversible JR gate it generates the output values and from this output we can predict the input values.

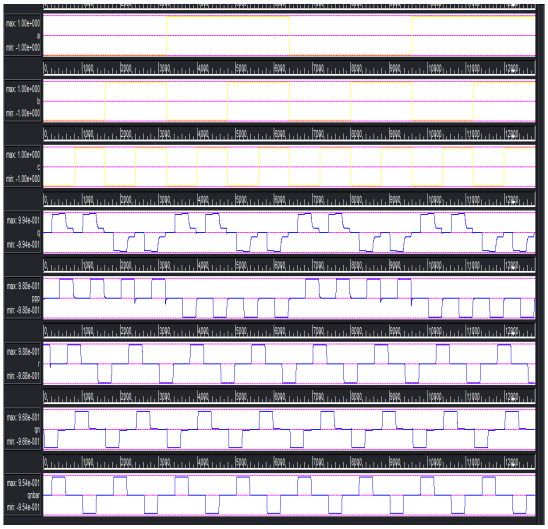


Figure-9. Output waveform of D Flip Flop using proposed reversible JR gate.

The simulated output waveform of D Flip Flop using reversible JR gate and Feynman gate is given in Figure-9. Based on clock values we get the D value. Here P is the garbage output. By this D flip flop SIPO serial to parallel converter is developed. The simulated output waveform is shown in Figure-10.

Figure-10. Output waveform of SIPO using proposed reversible JR gate.

Table-3. Comparison table of parameters with existing reversible D-Flip flop in QCA.

PARAMETERS	FREDKIN GATE	FREDKIN GATE-FEYNMAN GATE	JR GATE-FEYNMAN GATE
MVs	12	12	9
Clock Zone	4	4	4
No of Cells	595	482	232
Area	1.49um^2	1.20um^2	0.58um^2

The comparison table of reversible JR gate based D Flip Flop parameters with the existing reversible gate D Flip Flop is tabulated in Table-3. This shows that the number of cells used and the area is partially reduced in the proposed method.

8. CONCLUSIONS

The paper described about the realization and simulated design of JR reversible gate and the design of D flip flop using the proposed JR reversible gate in QCA. This reversible D Flip Flop uses only 50% of quantum cells compared to other combinations so the area of the design is reduced partially. Here 25% of MV's are reduced. The design of reversible logic based circuits gives less number of cells, so it reduces the overall area and complexity than that of a combinational circuit. So the proposed 4x4 JR reversible logic gate is efficient.

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