VOL. 12, NO. 19, OCTOBER 2017 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

# DESIGN AND PERFORMANCE EVALUATION OF HYBRID GDI LOGIC BASED ADDER CELLS

Suberna S.[1], Vanitha R.[1], Ravi T.[2] and Mathan N.[2]
[1]B.E Electronics and Communication Engineering, Sathyabama University, Chennai, India
[2]Department of Electronics and Communication Engineering, Sathyabama University, Chennai, India
E-Mail: subernashanmugham@gmail.com

**ABSTRACT**

This paper deals with the design of full adder using complementary metal oxide semi conductor (CMOS) logic, gate diffusion input (GDI) logic, modified GDI and transmission gate logic. These designs are implemented using H-Spice software. Performance parameters such as power dissipation and transistor counts are compared with the existing designs such as CMOS logic, GDI logic, and modified GDI logic. This design works efficiently with less transistor count and less power dissipation at 130nm technology.

**Keywords:** CMOS, GDI, modified GDI, power dissipation, transistor count.

## 1. INTRODUCTION

The most significant feature of current electronics is low power and energy efficient which are the important elements that give the ability in carrying out long lasting battery life systems. As there is a advancement in the technology there is an increased demand for the battery operated devices which is leading to the exponential growth of the electronic easily carried devices. Addition is the important arithmetic operation is used in many VLSI systems. The goal of VLSI design is to achieve high performance parameters such as power consumption and power delay product.

- **Full adders**

In digital arithmetic circuits, binary adder is an essential building block. It consists of an addition operation three binary inputs such as A, B, and C which generates sum and cout outputs values [5].

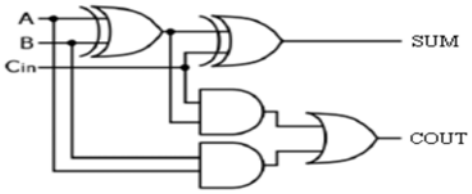


**Figure-1.** Logic circuit of full adder.

- **GDI technique**

The GDI cell is matching to a CMOS inverter structure. In a CMOS inverter the source of the PMOS is connected to Vdd and the source of NMOS is grounded. But in a GDI cell this might not certainly occur [7, 8]. There is some significant dissimilarity between the two. The three inputs in GDI are namely,

- G- inputs to the gate of NMOS and PMOS
- N- input to the source or drain of NNOS
- P- input to the source or drain of PMOS

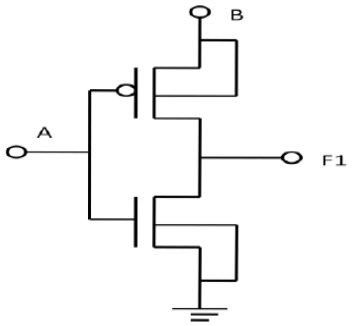


**Figure-2.** Basic GDI cell.

- **Modified GDI technique**

Power dissipation becomes most significant restriction in high performance applications. A high speed and multipurpose logic style for low power electronics design known as gate diffusion input(GDI) with reduced area and power necessities and proficient of implementing broad variety of logic suffers from some practical disadvantages like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These disadvantages can be overcome by modified gate diffusion input (m- GDI) logic style [9].

## 2. FULL ADDER CELLS

In existing full adder cells various techniques have been used namely CMOS logic, GDI logic, modified GDI logic and transmission gate logic. These techniques are used to form the full adder cells.

- **CMOS and GDI technique logic design**

This design uses CMOS logic and GDI logic. It consists of 30 transistors to generate the full adder. The CMOS logic generates the sum output and GDI logic generates carry output [2, 9].

ARPN Journal of Engineering and Applied Sciences



- **GDI and transmission gate logic design**

This design uses GDI logic and transmission gate logic. It consists of 12 transistors to generate a full adder. GDI logic generates the sum output and the transmission gate logic generates the carry output.

- **Modified GDI and transmission gate logic design**

This design uses modified GDI and transmission gate logic. It consists of 16 transistors to generate a full adder. Modified GDI logic generates the sum output and the transmission gate logic generates the carry output [5, 8].

- **Gate diffusion input logic design**

This design uses gate diffusion input technique. It consists of 23 transistors to generate a full adder. The gate diffusion input logic generates both the sum output and carry output.

- **CMOS logic and modified GDI logic**

This design uses CMOS logic and modified GDI technique. It consists of 34 transistors to generate the full adder. The CMOS logic generates the sum output and modified GDI technique generates the carry output.

## 3. PROPOSED FULL ADDERS

In the proposed adder cells, four techniques have been used namely, CMOS logic, GDI logic, modified GDI logic, transmission gate logic. For proposed full adder design 1 uses GDI and modified GDI logic and proposed full adder design 2 uses CMOS and transmission gate logic.

- **GDI and modified GDI logic design**

This design uses gate diffusion input(GDI) and modified gate diffusion input technique(modified GDI). It consists of transistors to generate the full adder. The GDI logic generates the sum output and the modified GDI logic produces the carry output.

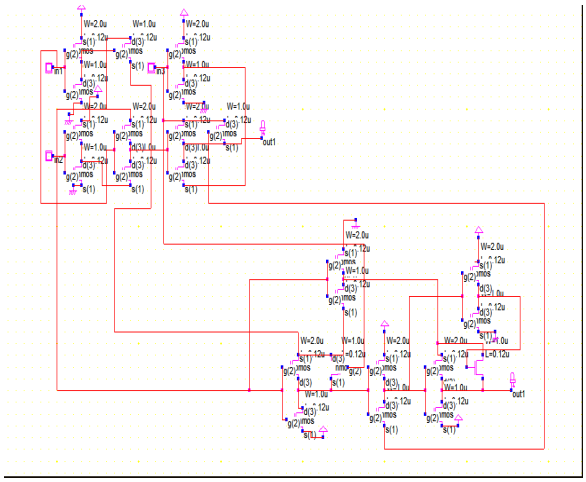

**Figure-3.** Proposed full adder cell design 1.

- **CMOS logic and transmission gate logic design**

This design uses CMOS logic and transmission gate logic. It consists of transistors to the generate the full adder. The CMOS logic generates the sum output and the transmission gate logic generates the carry output.

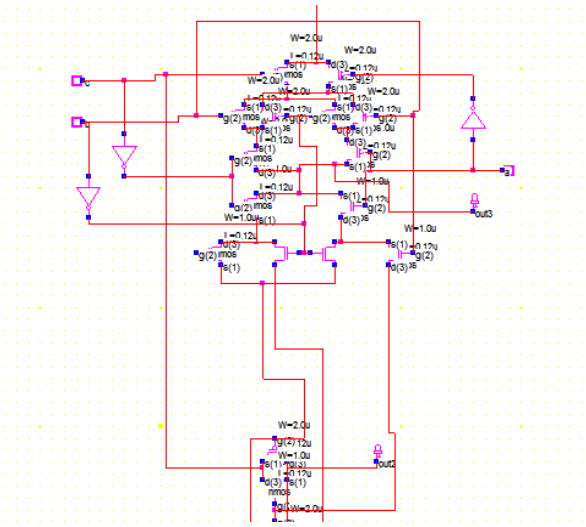

**Figure-4.** Proposed full adder cell design 2.

## 4. RESULTS AND DESCRIPTION

The results of existing full adder cells and proposed full adder cells have been discussed here.

- **Existing full adder cells**

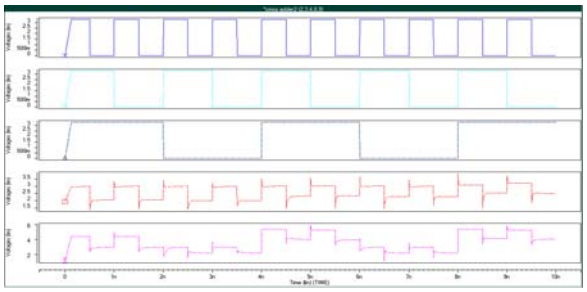

**Figure-5.** Simulation of CMOS and GDI technique logic design.

The Figure-5 uses CMOS logic and GDI logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

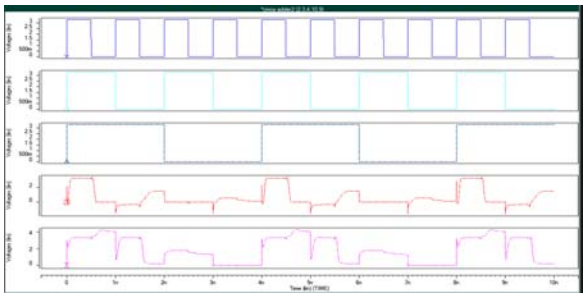

**Figure-6.** Simulation of GDI and transmission gate logic design.

The Figure-6 uses GDI and transmission gate logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

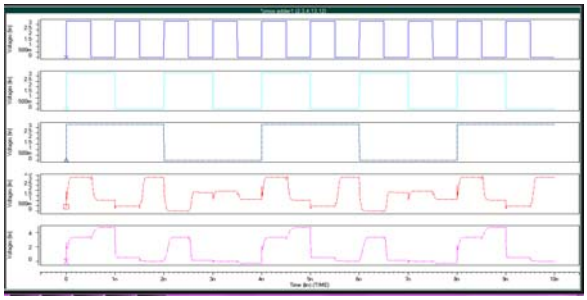

**Figure-7.** Simulation of modified GDI and transmission gate logic design.

The Figure-7 uses modified GDI and transmission gate logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

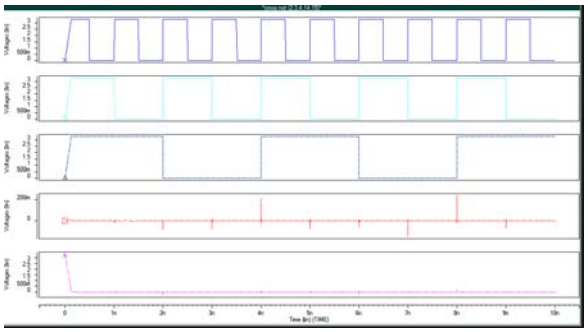

**Figure-8.** Simulation of gate diffusion input design logic.

The Figure-8 uses gate diffusion input (GDI) logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

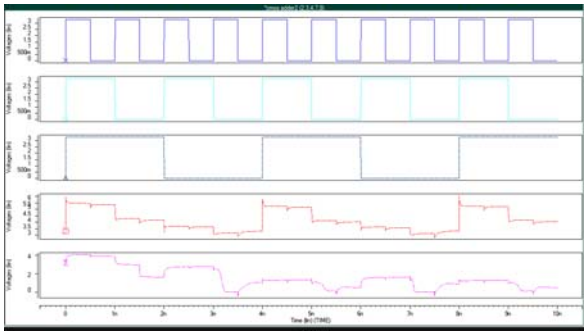

**Figure-9.** Simulation of CMOS logic and modified GDI logic design.

The Figure-9 uses CMOS logic and modified GDI logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

- **Proposed full adders**

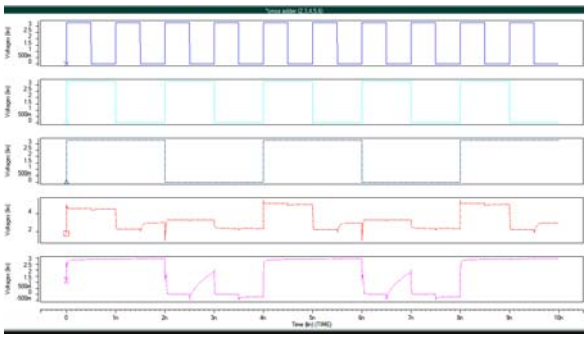

**Figure-10.** Simulation of GDI and modified GDI logic design.

The Figure-10 uses GDI and modified GDI logic design. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and waveform 5 is the carry.

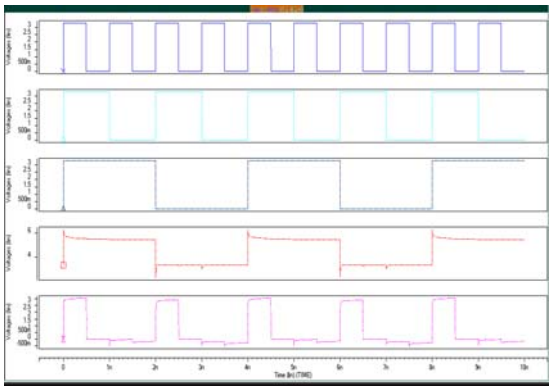

**Figure-11.** Simulation of CMOS and transmission gate logic design.

The Figure-11 uses CMOS logic and transmission gate logic. The waveform 1, 2, 3 is the input, the waveform 4 is the sum and the waveform 5 is the carry.

**Table-1.** Comparison of existing full adder cells.

| Design | Description | Average power (W) | Transistor counts |
|---|---|---|---|
| 1 | CMOS and GDI Technique logic design | 3.952e-05 | 30-T |
| 2 | GDI and TGL design | 1.517e-04 | 12-T |
| 3 | Modified GDI and TGL design | 1.863e-04 | 16-T |
| 4 | GDI logic design | 2.215e-03 | 23-T |
| 5 | CMOS and modified GDI design | 7.431e-04 | 34-T |

**Table-2.** Proposed full adder cells.

| Design | Description | Average power (W) | Transistor counts |
|---|---|---|---|
| 1 | GDI and modified GDI logic design | 1.048e-03 | 20-T |
| 2 | CMOS and TGL design | 4.127e-04 | 26-T |

## 5. CONCLUSIONS

In this paper, full adder circuits using alternative design logic has been proposed. The simulation was successfully implemented using H- Spice software with 130nm technology and compared with the standard designs like CMOS and GDI technique. Power dissipation is reduced in the case of GDI and modified GDI techniques also in CMOS and transmission gate logic (TGL) technique. Simulation result of existing full adder designs and proposed adder designs is compared and is better in terms of transistor counts and power dissipation.

## REFERENCES

[1] Suman Jhajharia and Manoj kumar. 2016. 1-bit full adder circuit using XOR-XNOR cells with power and area optimization. Journal of energy technologies and policy. 6(9), ISSN 2224.

[2] Shennu Rana. 2016. Optimized CMOS design of full adder using 45nm technology. International Journal of computer applications. 142(13): 21-24.

[3] Ruchi Gupta, Atul kumar Pathak, Gunakesh Sharma. 2016. Design of ultra low power 1-bit full adder cell using advane GDI 6T logic style. International Journal of Advanced Research in Computer Science and Software Engineering. 6(3): 794-798.

[4] M. Sivakumar, Dr.S. Omkumar. 2016. Integration of an Optimized GDI Logic based NOR Gate and Half adder into PASTA for the Low Power and Low Area Applications. International Journal of Applied Engineering Research. 11(4): 2629-2633.

[5] Ravi. T. 2016. 10-Nanometer carbon nano tube field effect transistor based high celerity transposed polyphase decimation filter. Materials Today: Proceedings. 3(6): 1799-1807.

[6] Shreedevi, Taranath H.B. 2016. The Design and Analysis of a Low Power High Speed hybrid Alternative Full adder circuits. International Journal of Science and Research. 5(5): 902-907.

[7] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar and Anup Dandapat. 2015. Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 23(10).

[8] M. Manoranjani and T. Ravi. 2015. Multithreshold CMOS sleep stack and logic stack technique for digital circuit design. ARPN Journal of Engineering and Applied Sciences. 10(10): 4550-4556.

[9] M. Micheal Priyanka and T. Ravi. 2015. Survey on role of Memristor in electronics. Proceedings of International Conference on Control Instrumentation Communication and Computational Technologies, ICCICCT 2015, pp. 738-744.

[10] D. Radhakrishnan. 2001. Low-voltage low-power CMOS full adder. IEE Proc.-Circuits Devices Syst. 148(1): 19-24.