COMPARISON OF TAGUCHI METHOD AND CENTRAL COMPOSITE DESIGN FOR OPTIMIZING PROCESS PARAMETERS IN VERTICAL DOUBLE GATE MOSFET

K. E. Kaharudin, F. Salehuddin, A. S. M. Zain and M. N. I. A. Aziz

Micro and Nanoelectronics Research Group, Centre for Telecommunication Research and Innovation (CeTRI), Universiti Teknikal Malaysia Melaka (UTeM), Durian Tunggal, Melaka, Malaysia E-Mail: khairilezwan@yahoo.com.my

ABSTRACT

As the MOSFETs becoming smaller, the process parameters of the MOSFET are difficult to be perfectly controlled which eventually leads to the statistical variation of many process variables. The statistical modeling is one of the approaches that can be implemented to control the process parameter variations, thereby optimizing the device characteristics. This paper presents a comparative study of Taguchi method and central composite design (CCD) for optimizing the process parameters in Vertical Double Gate MOSFET. The L_{27} orthogonal array of Taguchi method and CCD has been utilized to optimize six process parameters towards the device characteristics. The comparative analysis between Taguchi method and CCD for optimizing the process parameters in vertical double-gate MOSFET are performed in term of their efficiency and simplicity. The observation of the final results indicates that the Taguchi method is the most suitable statistical tools over the CCD for optimizing the process parameters in the device due to its simplicity (requires less experiment runs) and its efficiency (better in overall device characteristics).

Keywords: ANOVA, CCD, MOSFET, SNR, taguchi method.

INTRODUCTION

As the Metal-oxide-semiconductor Field Effect Transistor (MOSFET) is reduced in size, the number of atoms in the silicon substrate becomes fewer which results in the deterioration of the device characteristics of the MOSFET. This will lead to the erratic controls of the dopant numbers and placement in the MOSFET that eventually reduce the overall device performance [1]. The process parameters of the MOSFET which are not perfectly controlled may lead to the statistical variations [2]. In the fabrication of MOSFET, process parameters play a very important role in reducing the variation of the output responses (device characteristics). The process parameters contribute significant changes in the dopant profiles that would directly affect the device characteristics [3]. Hence, the suitable optimization approach is required to be implemented in order to minimize the statistical variations, thereby improving the device performance.

In context to any engineering problem, optimization refers to improving the performance of the system or process or product by applying several levels of multiple variables in different combinations to acquire the best possible results [4-6]. A lot of factors are required to be considered in order to select the best optimization approach for certain system or process. For instance, several factors such as the number of experiments, the number of process parameters, possibility of the interaction study between process parameters, cost, time, and complexity have to be considered before a certain optimization technique is deployed. Driven by the consideration of these factors, the design of experiment (DoE) is recognized as an important statistical tool for solving complex and multi-factor engineering problems [4].

The response surface methodology (RSM) is one of the statistical tools that utilize DoE to optimize multiple process parameters for the optimum results. The RSM consists of several different optimization techniques which are known as central composite design (CCD), D-optimal and Box-Bekhen [7-9]. However, these methods have the limitation of increased number of experiments if multiple process parameters were selected for the optimization. For example, the minimum number of experiments allowed if six process parameters are required to be investigated in CCD is 52 runs. With the involvement of multiple process parameters, these techniques are quite disadvantageous in term of the cost, time and the physical efforts. Hence, the simplified design strategy is required to apprehend these issues.

Taguchi method is one of the robust statistical tools which allows independent evaluation of the responses with minimum number of experiments [10, 11]. It utilizes a special orthogonal array (OA) for DoE and signal-to-noise ratio (SNR) analysis to predict the most optimal level settings of multiple process parameters [12]. With this method, the experimental results can be analyzed through the SNR and analysis of variance (ANOVA), thereby simultaneously determining the significance of the process parameters in term of their contribution to the device characteristics [13, 14].

Several works on the optimization of process parameters in MOSFET by using Taguchi method have been done as reported in [15-18]. Previous works based on the CCD are found in the literature [19-21] but which technique is the most appropriate for the optimization of process parameters in the vertical double-gate MOSFET is still not conclusive. Therefore, this study was planned to compare the effectiveness between the CCD and the Taguchi method in optimizing multiple process parameters

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of vertical double-gate MOSFET. The comparative analysis was focused on the efficiency, time and complexity. Six process parameters were involved in the experiment, which were known as substrate implant dose, V_{TH} implant dose; V_{TH} implant energy, halo implant dose, halo implant energy and halo implant tilt.

PROCESS SIMULATION

The process simulation was implemented through ATHENA module of Silvaco TCAD tools. The sample used in the process simulation was <100> orientation of p-type (boron doped) silicon substrate with concentration of 1 x 10¹⁴ atom/cm³. The silicon substrate was etched to form a silicon pillar that separates the two vertical poly-Si gates. The silicon substrate was oxidized for about 0.2 ms to ensure a thin oxide layer of 2nm was grown below the gates. The overall process flowchart of virtual fabrication for vertical double-gate MOSFET is depicted in Figure-1.

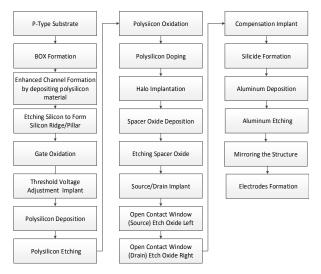


Figure-1. Vertical Double-gate MOSFET's process flowchart.

The aluminum layer was deposited on the top structure's surface and any unwanted aluminum was etched to develop the contacts [22, 23]. The final vertical double gate MOSFET device structure was completed by mirroring the right-hand side structure as illustrated in Figure-2. Once the device was built with ATHENA module, the completed device was characterized by ATLAS module to provide utilizing specific characteristics such as the I_D versus V_{GS} curve. The device characteristics such as threshold voltage (V_{TH}), drive current (I_{ON}), off-leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio and subthreshold swing (SS) were retrieved from the simulation. The device simulation condition is listed in Table-1.

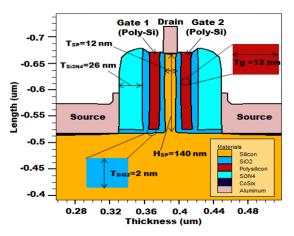


Figure-2. Vertical Double-gate MOSFET Structure.

Table-1. Device simulation's condition.

Device	Drain voltage, VD	Gate voltage, V _G (V)				
characteristics	(V)	V _{Initial}	V_{Step}	V_{Final}		
Threshold Voltage (V _{TH})	1.0	0	0.1	2.0		
Drive Current (I _{ON})	1.0	0	0.1	2.0		
Leakage Current (I _{OFF})	1.0	0	0.1	2.0		
Subthreshold Swing (SS)	1.0	0	0.1	2.0		

CENTRAL COMPOSITE DESIGN (CCD)

A second order design can be constructed efficiently with central composite designs (CCD) [24]. The CCD is the first-order (2^N) designs augmented by additional center and axial points to allow estimation of the tuning parameters of a second-order model. The CCD is able to be analyzed through State-Ease Design Expert software. State-Ease Design-Expert software offers an impressive array of design options and provides the flexibility to handle multiple factors and multiple responses. Table-2 shows a list of process parameters and their levels which have been studied in this work.

Each numeric factor is varied over five levels: plus and minus alpha (axial points), plus and minus 1 (factorial points) and the center point. The value of alpha (α) is determined by using Equation (1):

$$\alpha = 2^{\frac{q-1}{4}} \tag{1}$$

where q is the number of factors (process parameters). Experimental results are then analyzed by using response surface regression. The correlation between responses (device characteristics) and independent variables (process parameters) is obtained by fitting them into the second order polynomial equation as in Equation (2) [24]:

(CR)

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$$y = \beta_0 + \sum_{j=1}^k \beta_j x_j + \sum_{i < j} \sum \beta_{ij} x_i x_j + \sum_{j=1}^k \beta_{jj} x_j^2 + \in$$
(2)

where, *y* represents the responses, *k* is the total number independent factors, β_0 is an intercept, *i*, *ij*, *j*, and *jj* with β represents the coefficient values for linear, quadratics and the interaction effects, respectively. The *x_i*, and *x_j* indicate the coded levels of the independent variables [19]. The

analysis of a second order model is automatically executed via the State-Ease Design Expert software. The analysis of variance (ANOVA) for fitting the data to second order and contour plots will assist in characterizing the response surface. In this research, the ultimate goal is to fit the second order model for optimizing multiple responses by using central composite design (CCD).

Sym	Process parameter (Factor)	-1 Level	+1 Level	- Alpha (-α)	+ Alpha (+α)
А	Substrate Implant Dose (atom/ cm ³)	$1 x 10^{14}$	$1.06 x 10^{14}$	-2.37841	+2.37841
В	V _{TH} Implant Dose (Atom /cm ³)	9.81x10 ¹²	9.87x10 ¹²	-2.37841	+2.37841
С	V _{TH} Implant Energy (kev)	20	22	-2.37841	+2.37841
D	Halo Implant Dose (Atom /cm ³)	2.61x10 ¹³	2.67x10 ¹³	-2.37841	+2.37841
Е	Halo Implant Energy (kev)	170	174	-2.37841	+2.37841
F	Halo Implant Tilt (degree)	24	30	-2.37841	+2.37841

Table-2. Experimental setup for process parameters using RSM-CCD.

TAGUCHI METHOD

Taguchi method is an experimental approach which is modified and standardized based on a design of experiment (DOE). In other words, Taguchi method is a DOE that comprises a special orthogonal array (OA) table. The function of OA table of Taguchi method is to make the DOE becomes easier and consistence where it only requires a small number of experiments to study the entire process parameters space [25]. Hence, the time and the cost of the optimization process can be saved efficiently. The experimental results from the DOE are transformed into a signal-to-noise ratio (SNR) [26]. In general, there are three categories of quality characteristic in the analysis of SNR, i.e. the nominal-the-best, the lower-the-better and the higher-the-better [27]. The SNR (Nominal-the-best), η can be expressed as [28]:

$$\eta = 10 Log_{10} \left[\frac{\mu^2}{\sigma^2} \right]$$
(3)

whereas

$$\mu = \frac{Y_i + \dots + Y_n}{n} \tag{4}$$

and

$$\sigma^{2} = \frac{\sum_{i=1}^{n} (Y_{i} - \mu)^{2}}{n - l}$$
(5)

where, *n* is the number of tests and *Yi* is the experimental value of the threshold voltage, μ is mean and σ^2 is the variance. In the nominal-the best, there are two types of factor to determine which are dominant and adjustment factors. The higher the SNR of a certain level of process parameter indicates the better quality characteristics. Therefore, the optimal level of a process parameter is selected based on its highest SNR.

This current work focused on the optimization of six process parameters upon the threshold voltage (V_{TH}) value using L_{27} orthogonal array Taguchi method. The process parameters that were investigated by using the Taguchi method were similar to the previous CCD. The differences were only at the distribution levels of process parameters and the presence of noise factors as listed in Table-3 and Table-4, respectively.

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Factor	Units	Level 1	Level 2	Level 3
А	atom/cm ³	$1x10^{14}$	$1.03 x 10^{14}$	1.06×10^{14}
В	atom/cm ³	9.81x10 ¹²	9.84x10 ¹²	9.87x10 ¹²
С	kev	20	21	22
D	atom/cm ³	2.61x10 ¹³	2.64x10 ¹³	2.67x10 ¹³
Е	kev	170	172	174
F	degree	24	27	30

Table-3. Process parameters and their levels.

Symbol	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temperature	Co	920	923
V	Polysilicon Oxidation Temperature	Co	870	873

Table-4. Noise factors and their levels.

The analysis of variance (ANOVA) is performed to identify the most significant process parameters toward the desired value. The optimal combination level of process parameters can be predicted by performing both SNR analysis and ANOVA. Finally, a verification test is performed to verify the optimal process parameters.

RESULTS AND DISCUSSIONS

The results of the experiments are divided into three sections. The first section was the results retrieved from the Silvaco TCAD simulation (before optimization). The second section was the results retrieved after the optimization using the CCD method. The final section was the results retrieved after optimization using Taguchi method. After that, the experimental validation of the final results was performed to investigate which method was the most appropriate to be implemented in optimizing multiple process parameters in vertical double-gate MOSFET.

Device characterization

The device characteristics of the vertical doublegate MOSFET were retrieved from the simulation using an ATLAS module of Silvaco TCAD. Figure-3 displays the graph of the drain current (I_D) versus gate voltage (V_G) at drain voltage (V_D) = 0.05 V and V_D = 1.0 V for vertical double-gate MOSFET. The initial threshold voltage (V_{TH}) extracted from the graph was observed to be 0.405 V.

Figure-4 displays the graph of subthreshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05 V and V_D = 1.0 V for vertical double gate MOSFET device. From the graph, it was observed that the initial value of drive current (I_{ON}) was 728.4 μ A/ μ m. Meanwhile, the leakage current (I_{OFF}) was observed to be 1.075 E-15 A/ μ m.

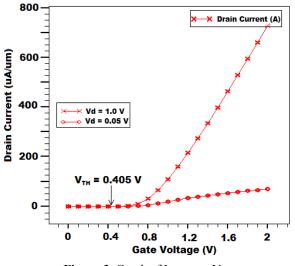


Figure-3. Graph of I_D versus V_G.

The subthreshold swing (SS) value was then extracted from the inverse slope of log_{10} I_D vs. V_{GS} characteristic. It shows how much change in the gate voltage is required to change the drain current by one decade as shown in Eq. (6) [29]:

$$SS = \left[\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right]^{-1}$$
(6)

The value of subthreshold swing (SS) was observed to be 63.54 mV/dec. The SS value is one of the crucial characteristics in MOSFET's device that determine the speed of switching transition from "ON" to "OFF" state or vice versa.

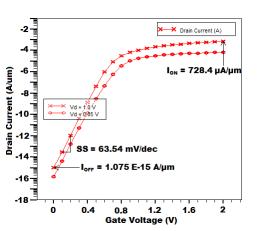


Figure-4. Graph of Subthreshold I_D versus V_G.

Optimization using Central Composite Design (CCD)

All the experiments for the process parameters were designed based on the Response Surface Methodology (RSM) using CCD with the aid of stat-ease design expert (version 7). The total 52 runs with 32 factorial, 12 axial points and 8 center points were suggested by Stat-ease design expert to optimize multiple responses. The impact of substrate implant dose, V_{TH} implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant dose, halo implant energy and halo implant tilt was investigated through the modeling stages.

In the CCD, four responses (device characteristics) were modeled separately, which were V_{TH} , I_{ON} , I_{OFF} and SS. The second-order response surface representing the V_{TH} , I_{ON} , I_{OFF} and SS were expressed as a function of substrate implant dose, V_{TH} implant dose, V_{TH}

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implant energy, halo implant dose, halo implant energy and halo implant tilt. Based on the observed data, the response functions for V_{TH} , I_{ON} , I_{OFF} and SS have been determined in the coded factor units as in Equation (7), (8), (9) and (10), respectively:

$$V_{TH} = 0.41 - 2.309E - 05 * A + 4.561E - 04 * B$$

- 7.732E - 03 * C + 0.014 * D + 2.911E - 03
- 0.043 * F (7)

$$I_{ON} = 703.72 - 1.06 * A - 1.50 * B + 1.46 * C - 11.01 * D - 1.55 * E + 19.19 * F$$
(8)

$$I_{OFF} = 3.060E - 15 + 2.852E - 18*A - 6.379E$$

-17*B+6.516E-16*C-1.120E-15*D
-8.486E-17*E+3.680E-15*F (9)

$$SS = 63.10 + 0.036 * A - 5.273E - 03 * B$$

-0.098 * C + 0.067 * D - 0.060 * E - 0.30 * F (10)

The analysis of variance (ANOVA) for V_{TH} , I_{ON} , I_{OFF} and SS were depicted in Tables 5, 6, 7 and 8 correspondingly. These analyses were carried out for the confidence's level that was not less than 95% as specified by CCD. The ANOVA of CCD consist of several parameters such as degree of freedom (DF), sum of square (SSQ), mean square (MS), F-value and P-value.

Source	Source SSQ		MS	F-value	P-value
Model 0.092		6	0.015	496.69	< 0.0001
А	2.309E-08	1	2.309E-08	7.467E-04	0.9783
В	9.012E-06	1	9.012E-06	0.29	0.5920
С	2.589E-03	1	2.589E-03	83.74	< 0.0001
D	8.422E-03	1	8.422E-03	272.37	< 0.0001
Е	3.670E-04	1	3.670E-04	11.87	0.0012
F	0.081	1	0.081	2611.87	< 0.0001
Residual	1.391E-03	45	3.092E-05		
Lack of fit	1.391E-03	38	3.662E-05		
Pure Error	0.000	7	0.000		
Cor Total	0.094	51			

Table-5. ANOVA table for V_{TH} (CCD).

Based on Table-5, the significance of the model is revealed in accordance of the F-value of 496.69. There was only a probability of 0.01% of noise in the "F-value model". If the values of "Probability > F" less than 5% (0.05), then the model terms were considered significant. In this case, factor C, D, E and F were significant model term due to their P-values less than 0.05. In contrast, factor A and B was considered insignificant model terms due to their P-value were greater that 0.1. The similar interpretation of the ANOVA table can be applied to the other responses (device characteristics) as summarized in Tables 6, 7 and 8.





Source	SSQ	DF	MS	F-value	P-value
Model 21541.05		6	3590.17	20.84	< 0.0001
А	49.07	1	49.07	0.28	0.5962
В	97.11	1	97.11	0.56	0.4566
С	91.86	1	91.86	0.53	0.4690
D	5246.72	1	5246.72	30.46	< 0.0001
Е	103.72	1	103.72	0.60	0.4418
F	15952.57	1	15952.57	92.61	< 0.0001
Residual	7751.18	45	172.25		
Lack of fit	3561.12	38	93.71	0.16	
Pure Error 4190.06		7	598.58		0.9999
Cor Total	29292.23	51			

Table-6. ANOVA table for I_{ON} (CCD).

Table-7. ANOVA table for I_{OFF} (CCD).

Source	Source SSQ		MS	F-value	P-value
Model	6.597E-28	6	1.100E-28	9.05	< 0.0001
А	3.522E-34	1	3.522E-34	2.899E-05	0.9957
В	1.763E-31	1	1.763E-31	0.015	0.9047
С	1.839E-29	1	1.839E-29	1.51	0.2250
D	5.434E-29	1	5.434E-29	4.47	0.0400
Е	3.119E-31	1	3.119E-31	0.026	0.8734
F	5.865E-28	1	5.865E-28	48.28	< 0.0001
Residual	5.467E-28	45	1.215E-29		
Lack of fit	5.467E-28	38	1.439E-29		
Pure Error	0.000	7	0.000		
Cor Total	1.206E-27	51			

Table-8. ANOVA table for SS (CCD).

Source	Source SSQ		MS	F-value	P-value
Model	4.66	6	0.78	5.71	0.0002
А	0.056	1	0.056	0.41	0.5245
В	1.204E-03	1	1.204E-03	8.850E-03	0.9255
С	0.42	1	0.42	3.06	0.0872
D	0.20	1	0.20	1.44	0.2365
Е	0.15	1	0.15	1.13	0.2929
F	3.84	1	3.84	28.19	< 0.0001
Residual	6.12	45	0.14		
Lack of fit	6.12	38	0.16		
Pure Error	0.000	7	0.000		
Cor Total	10.78	51			

Next, the optimization process was carried out by searching the desirability value. The importance level of

each process parameter and response can be set before the optimization process is done as shown in Table-9.

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Name	Goal	Lower limit	Upper limit	Importance
A-Substrate Implant Dose	is in range	1E14	1.06E14	3
B-V _{TH} Implant Dose	is in range	9.81E12	9.87E12	3
C-V _{TH} Implant Energy	is in range	20	22	3
D-Halo Implant Dose	is in range	2.61E013	2.67E13	3
E-Halo Implant Energy	is in range	170	174	3
F-Halo Implant Tilt	is in range	24	30	3
V _{TH}	is target $= 0.447$	0.44	0.45	5
I _{ON}	maximize	533	741.1	4
I _{OFF}	minimize	1.704E-16	2E-011	3
SS	minimize	58.49	63.78	3

Table-9. Desirability setting for optimization.

The maximum and the minimum level of importance that can set using the stat-ease expert design is level 5 and level 1 correspondingly. In this case, the level of importance of V_{TH} and I_{ON} was set to level 5 and level 4 respectively. Meanwhile, the level of importance of other parameters was set to level 3. This means that the value of V_{TH} and I_{ON} were prioritized before the others in finding the optimal solution. Furthermore, the goal of each response and process parameter can be set as desired. For instance, the goal of V_{TH} value was set to "is target = 0.447" and the goal of the I_{ON} were set to "maximize" as depicted in Table-9.

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Table-10 shows the best ten of the optimal results and the predicted value of responses respectively generated via the stat-ease design expert software. The best level setting for a process recipe of vertical doublegate MOSFET were selected by the highest desirability value. In this case, the highest desirability value was observed to be 0.530. Besides that, the predicted values of the responses (device characteristics) were also generated.

Therefore, solution no. 1 was selected to be the best combinational level setting for achieving the desired results. The overall desirability function of the device characteristics is represented in the form of bar graph as depicted in Figure-5. It can be observed that the desirability varied from 0 to 1 depending on the closeness of the device characteristic towards the goal. The verification test is conducted at the optimum level setting with the highest desirability and the results are recorded in Table-11. The percentage differences between the predicted value and the actual value for V_{TH} , I_{ON} , I_{OFF} and SS were 0.22%, 0.33%, 91.8% and 0.35% respectively.

Na	•	В	С	D	Е	F	Predicted value				Desinability
No.	Α	Б	C	D	E	r	VTH	Ion	Ioff	SS	Desirability
1	1E14	9.81E12	20.04	2.614E13	174	24.19	0.447	695	5.345E-17	63.32	0.530 (Selected)
2	1.01E14	9.82E12	21.65	2.63E13	174	24	0.447	687.7	2.611E-17	63.24	0.529
3	1E14	9.81E12	21.77	2.65E13	174	24.56	0.447	685.1	2.508E-17	63.2	0.529
4	1E14	9.84E12	20.46	2.63E13	174	24.57	0.447	689.9	4.411E-17	63.27	0.528
5	1E14	9.82E12	20.95	2.65E13	174	24.81	0.447	687.4	1.034E-17	63.24	0.528
6	1E14	9.87E12	20.88	2.63E13	173.97	24.45	0.447	687.6	6.381E-17	63.25	0.527
7	1E14	9.81E12	22	2.65E13	173.31	24.27	0.447	685.3	3.942E-17	63.22	0.526
8	1E14	9.81E12	20.32	2.66E13	174	25.48	0.447	687.2	4.248E-17	63.26	0.523
9	1.03E14	9.84E12	21.06	2.62E13	174	24	0.447	689.1	6.091E-17	63.29	0.522
10	1E14	9.85E12	22	2.64E13	173.01	24	0.447	684.7	1.201E-16	63.24	0.522

Table-10. A set of optimal solutions for desirability (V_{TH} , I_{ON} , I_{OFF} , SS).

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Response	Predicted	Actual value	Difference (%)
\mathbf{V}_{TH}	0.447	0.446	0.22
I _{ON}	695	692.7	0.33
I _{OFF}	5.345E-17	6.525E-16	91.8
SS	63.32	63.54	0.35

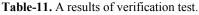




Figure-5. Bar graph of desirability for V_{TH}, I_{ON}, I_{OFF} and SS.

0.500

Optimization using L₂₇ Orthogonal Array of Taguchi Method

0.0870862

0.250

lon

SS

0.000

Combined

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The optimization of process parameters using Taguchi method mainly focuses on a single response, unlike the previous CCD method which involves multiple responses (device characteristics). The V_{TH} was the main device characteristic that had been investigated via L_{27} orthogonal array of Taguchi method. After 27 experiments

of the L_{27} orthogonal array Taguchi method has been performed, all the V_{TH} results were transformed into SNR. Since the value of V_{TH} was desired to be nominal, the SNR of the V_{TH} was categorized into nominal-the-best quality characteristic. The SNR for each row of experiments were computed and recorded in Table-12 by using Eq. (3), (4) and (5).

0.750

0.575638

0.5297

1.000

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Exp			Т	hreshold vo	oltage , V	⁷ тн (V)		
no.	V _{TH1}	V _{TH2}	V _{TH3}	V _{TH4}	Mean	Variance	SNR	SNR (Nominal-
	(U_1V_1)	(U_1V_2)	(U_2V_1)	(U_2V_2)		(x10 ⁻⁴)	(Mean)	the-Best)
1	0.405	0.417	0.424	0.439	0.421	2.02	-7.51	29.45
2	0.377	0.390	0.395	0.411	0.393	1.98	-8.11	28.94
3	0.324	0.336	0.342	0.357	0.340	1.88	-9.38	27.88
4	0.410	0.421	0.428	0.444	0.426	2.03	-7.42	29.51
5	0.381	0.394	0.4	0.416	0.398	2.11	-8.01	28.75
6	0.328	0.339	0.346	0.361	0.344	1.91	-9.28	27.91
7	0.420	0.432	0.439	0.454	0.436	2.02	-7.21	29.75
8	0.391	0.404	0.409	0.426	0.408	2.10	-7.80	28.99
9	0.337	0.348	0.355	0.370	0.353	1.91	-9.06	28.13
10	0.391	0.433	0.410	0.424	0.415	3.35	-7.65	27.10
11	0.339	0.350	0.357	0.372	0.355	1.91	-9.01	28.18
12	0.427	0.440	0.447	0.463	0.444	2.25	-7.05	29.43
13	0.359	0.401	0.378	0.392	0.383	3.35	-8.35	26.40
14	0.310	0.321	0.327	0.341	0.325	1.67	-9.77	28.01
15	0.395	0.407	0.414	0.429	0.411	2.02	-7.72	29.24
16	0.389	0.430	0.407	0.421	0.412	3.20	-7.71	27.25
17	0.337	0.348	0.355	0.370	0.353	1.91	-9.06	28.13
18	0.425	0.437	0.444	0.460	0.442	2.14	-7.10	29.60
19	0.321	0.332	0.338	0.352	0.336	1.67	-9.48	28.30
20	0.408	0.420	0.429	0.442	0.425	2.06	-7.44	29.42
21	0.379	0.391	0.398	0.413	0.395	2.02	-8.06	28.89
22	0.348	0.359	0.366	0.381	0.364	1.91	-8.79	28.40
23	0.438	0.450	0.459	0.472	0.455	2.06	-6.84	30.01
24	0.408	0.420	0.427	0.442	0.424	2.02	-7.45	29.51
25	0.313	0.324	0.330	0.344	0.328	1.67	-9.69	28.09
26	0.4	0.411	0.420	0.433	0.416	1.95	-7.62	29.47
27	0.371	0.383	0.390	0.405	0.387	2.02	-8.24	28.72

Table-12. SNR for V_{TH} in vertical double gate MOSFET.

Based on Table-12, the highest SNR for V_{TH} was recorded at experiment row 23 which was 30.01 dB. This implies that experiment row 23 had the best insensitivity for V_{TH} value. Since the design of experiment (DoE) was orthogonally constructed, the SNR of each process parameters can be separated out. The SNR (Nominal-thebest) was summarized in Table-13.

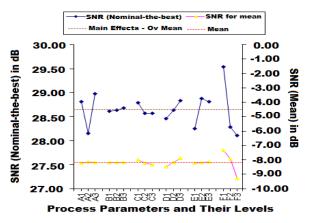
The SNR values for each level of process parameter are converted into the factor effect graph for SNR (Nominal-the-best) as depicted in Figure-6. The dashed horizontal lines in both graphs represent the overall mean of SNR (Nominal-the-best) and SNR (Mean) which were 28.55 dB and -8.20 dB. According to Figure 6, factor A_3 , B_3 , C_1 , D_3 , E_2 , and F_1 were selected as the optimum value for V_{TH} due to their highest value of SNR.

Table-13. SNR of process parameters.

Process	Signa	Overall			
parameters	Level 1	Level 2	Level 3	mean SNR	
А	28.81	28.15	28.98	28.65	
В	28.62	28.64	28.68		
С	28.80	28.57	28.57		
D	28.46	28.64	28.83		
Е	28.25	28.88	28.81		
F	29.54	28.28	28.11		



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Figure-6. Factor effect plot for SNR (Nominal-the-best) and SNR (Mean) for V_{TH} .

The ANOVA was then employed for the evaluation of the experimental results with the main aim was to determine the factor effect on SNR. The ANOVA computes parameters which are known as a sum of squares (SSQ), degree of freedom (DF), variance or mean square (MS), F-value and percentage of factor effect on SNR. The results of ANOVA for V_{TH} in the device are listed in Table-14.

Sym.	DF	SSQ	MS	F-value	Factor effects on SNR (%)	Factor effects on mean (%)
Α	2	3	2	8306	17	0
В	2	0	0	42	0	0
С	2	0	0	724	1	2
D	2	1	0	1476	3	8
Е	2	2	1	5168	10	0
F	2	11	5	26362	53	89

According to Table-14, the most dominant influence of process parameters towards the V_{TH} value were factor F (Halo Implant Tilt = 53%), factor A (Substrate Implant Dose = 17%) and factor E (Halo Implant Energy = 10%). Hence, these factors should be set at "best setting" and they were not recommended to be used as an adjustment factor. Factor B (V_{TH} Implant Dose = 0%) and factor C (V_{TH} Implant Energy = 1%) are considered as neutral factors as they did not contribute much to the factor effect on SNR. Meanwhile, factor D (Halo Implant Energy = 3%) was considered as an adjustment factor as due to its large effect on mean (8%) and small factor effect on SNR (3%) if compared to other neutral factors. The adjustment factor is specifically utilized to acquire the desired V_{TH} value. Therefore, the best combination level setting of process parameters after the optimization were: $A_3B_3C_1D_2E_2F_1$. Table-15 shows the overall best setting of process parameters for vertical double-gate MOSFET by using Taguchi method. The results of Taguchi analysis were shown in Table-16.

 Table-15. Best setting of process parameters (Taguchi method).

Sym.	Process parameter	Units	Best value
А	Substrate Implant Dose	atom/cm ³	1.06x10 ¹⁴
В	V_{TH} Implant Dose	atom/cm ³	9.87x10 ¹²
С	V _{TH} Implant Energy	kev	20
D	Halo Implant Dose	atom/cm ³	2.64x10 ¹³
Е	Halo Implant Energy	kev	172
F	Halo Implant Tilt	degree	24

After the optimization approaches, the SNR (Nominal-the-best) and SNR (Mean) of V_{TH} were observed to be 30.10 dB and -7.13 dB respectively. These values are well within the predicted range. For SNR (Nominal-the-best), 30.10 dB is within the predicted SNR range of 30.45 to 29.75 dB (30.10±0.35 dB). For SNR (Mean), -7.13dB is within the predicted SNR range of -7.06 to -7.20 dB (-7.50±0.07 dB). The SNR (Nominal-the-best), 30.10 dB is observed to be the highest value among the others in Table-12, which indicates the process parameter variations have been statistically optimized by Taguchi method. The closest value of V_{TH} upon ITRS 2013 prediction (0.447 V) for low power (LP) multi-gate (MG) technology was 0.445 V.

Table-16. Final Results of V_{TH} after optimization (Taguchi method).

Threshold voltage (V)			SNR (Mean)	SNR (Nominal-the-	
V _{TH1}	VTH2	V тнз	V _{TH4}	SINK (Mean)	best)
0.424	0.436	0.445	0.458	-7.13	30.10

Experimental validation

Experimental validation is the final step in the design of experiment (DoE) process. The main purpose of the experimental validation is to validate the results retrieved during analysis phase [28]. In this case, the experimental validation was performed by conducting an actual simulation test by using the overall best level setting of process parameters that have been previously predicted by the CCD and Taguchi method. The results retrieved from both CCD and Taguchi method were compared to the prediction of International Technology Roadmap Semiconductor 2013 (ITRS 2013) for low power (LP) multi-gate (MG) technology requirement in the year 2020 [30]. Table-18 shows the results of the experimental validation for both CCD and Taguchi method.

Based on the results in Table-17, the retrieved V_{TH} value using both CCD and Taguchi method was

within the predicted range. In terms of I_{ON}, the value produced by Taguchi method was only 0.39% lower than the value produced by CCD. However, there is a significant improvement in the IOFF. ION/IOFF ratio and SS value when the Taguchi method is applied. The IOFF value optimized by Taguchi method is 35.2% lower than the value optimized by RSM-CCD. The ION/IOFF ratio produced by Taguchi method was observed to be 34.9% higher than the value produced by CCD. The SS value retrieved via Taguchi method was 8.51% lower that the SS value retrieved through the CCD. Therefore, it can be concluded that the Taguchi method is more suitable to be applied as an optimization tool for vertical double-gate MOSFET than the CCD due to its simplicity (requires less experiment runs) and its efficiency (better in overall device characteristics).

Table-17. Results of experimental validation.

Device characteristics	Optimization using Taguchi method	Optimization using RSM-CCD	Difference (%)	ITRS 2013 prediction [25]
$V_{TH}(V)$	0.445	0.446	0.22	±12.7% of 0.447
$I_{ON}(\mu A/\mu m)$	690	692.7	0.39	≥ 533
I_{OFF} (A/µm)	4.227E-16	6.525E-16	35.2	$\leq 20p$
I _{ON} /I _{OFF} Ratio	1.632E12	1.062E12	34.9	-
SS (mV/dec)	58.13	63.54	8.51	-

CONCLUSIONS

This study was carried out to compare two optimization approaches which were central composite design and Taguchi method. Six process parameters which were known as substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant dose, halo implant energy and halo implant tilt were selected as a case study. Based on the study, the following points are drawn as conclusions:

- Taguchi method only utilizes 27 experiments for analyzing the process parameters while CCD suggests the minimum of 52 experiments.
- At optimized condition, Taguchi method produces better overall device characteristics over the CCD.
- Taguchi method only involves a single response to be analyzed while CCD involves all the four responses which requires a lot of time.
- Taguchi method offers the quantification of the contribution for each process parameters which is not possible with CCD.

Therefore, it can be concluded that Taguchi method can be considered as a robust statistical method for optimizing the process parameters for vertical double-gate MOSFET. The data analysis and the optimization of process parameters can be done by using the fewest number of experiments, less computation and a visual graph that is easy to read and interpret from. The optimized values obtained from both methods are in good agreement with the prediction of ITRS 2013 for low power (LP) multi-gate (MG) technology requirement in the year 2020. Thus, the Taguchi method can be regarded as an efficient optimization tool for the optimization of MOSFET device.

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REFERENCES

- Salehuddin F. *et al.* 2010. Impact of SALICIDE and Source/Drain Implants on Leakage Current and Sheet Resistance in 45nm NMOS Device. J. Telecommunication, Electronic and Computer Engineering. 2(1): 35-41.
- [2] Chen C. Y., Lin J. T. & Chiang M. H. 2013. Comparative study of process variations in junctionless and conventional double-gate MOSFETs. in IEEE Nanotechnol. Mater. Devices Conf. IEEE NMDC. pp. 1-2.
- [3] Kaharudin K. E., Hamidon A. H. & Salehuddin F. 2014. Design and Optimization Approaches in Double Gate Device Architecture. Int. J. Engineering and Technology. 6(5): 2070-2079.
- [4] Asghar A., Abdul Raman A. A. & Daud W. M. A. W. 2014. A comparison of central composite design and Taguchi method for optimizing Fenton process. Sci. World J. pp. 1-14.
- [5] Yussoff A. R., Suffian M. R. Z. M. & Taib M. Y. 2011. Literature Review of Optimization Techniques for Chatter Suppression in Machining. J. Mech. Eng. Sci. 1: 47-61.
- [6] Ghazali F. A., Manurung Y. H. P., Ackiel M., Alias S. K. & Abdullah S. 2015. Effects of Process Parameters on the Mechanical Properties and Failure Behaviour of Spot Welded Low Carbon Steel. J. Mech. Eng. Sci. 8: 1489-1497.
- [7] Azami M., Bahram M. & Nouri S. 2013. Central Composite Design for the Optimization of Removal of the Azo Dye, Methyed Red, from Waste Water using Fenton Reaction. Curr. Chem. Lett. 2: 57-68.
- [8] Hassan D. B., Aziz A. R. A. & Daud W. M. A. W. 2012. Using D-Optimal Experimental Design to optimize Remazol Black B Mineralization by Fentonlike Peroxidation. Environ. Technol. 33: 1111-1121.
- [9] Catalkaya E. C. & Kargi F. 2009. Response Surface Analysis of Photo-Fenton Oxidation of Simazine. Water Environ. Res. 81: 735-742.
- [10] Salehuddin F. *et al.* 2013. Comparison of 2k-Factorial and Taguchi Method for Optimization Approach in 32nm NMOS Device. in Mathematical Methods and

Optimization Techniques in Engineering. pp. 125-134.

- [11] Kaharudin K. E., Salehuddin F., Zain A. S. M., Aziz M. N. I. A. & Ahmad I. 2016. Optimization of process parameter variations on Threshold Voltage in Ultrathin Pillar Vertical Double Gate MOSFET Device. ARPN Journal of Engineering and Applied Sciences. 11(6): 3838-3848.
- [12] Mohammad N. et al. 2013. Characterization & Optimization of 32nm P-Channel MOSFET Device. J. Telecommunication, Electronic and Computer Engineering. 5(2): 49-54.
- [13] Kaharudin K. E., Salehuddin F., Zain A. S. M. & Aziz M. N. I. A. 2015. Optimization of Process Parameter Variations on Leakage Current in Silicon-on-insulator Vertical Double Gate Mosfet Device. J. Mechanical Engineering and Sciences. 9: 1614-1627.
- [14] Parate P. R. & Yarasu R. B. 2013. Application of Taguchi and ANOVA in Optimization of Process Parameters of Lapping Operation for Cast Iron. J. Mech. Eng. Sci. 4: 479-487.
- [15] Kaharudin K. E., Hamidon A. H. & Salehuddin F. 2014. Implementation of Taguchi Modeling for Higher Drive Current (ION) in Vertical DG-MOSFET Device. J. Telecommunication, Electronic and Computer Engineering. 6(2): 11-18.
- [16] A.H. Afifah Maheran, P.S. Menon, I. Ahmad, S. Shaari, H.A. Elgomati, F. Salehuddin. 2013. Design and Optimization of 22 nm Gate Length High-k/Metal gate NMOS Transistor. J. Physics Conference Series. 431: 1-9.
- [17] Salehuddin F., Kaharudin K. E., Zain A. S. M., Yamin A. K. M. & Ahmad I. 2014. Analysis of process parameter effect on DIBL in n-channel MOSFET device using L27 orthogonal array. in Int. Conf. Fundam. Appl. Sci. AIP Conf. Proc. 1621: 322-328.
- [18] Abdullah H Jurait J., Lennie A., Nopiah Z, M. & Ahmad I. 2009. Simulation of Fabrication Process VDMOSFET Transistor Using Silvaco Software. Eur. J. Sci. Res. 29: 461-470.
- [19] Ramakrishnan H., Shedabale S., Russell G. & Yakovlev A. 2008. Analysing the effect of process variation to reduce parametric yield loss. in Proc. -2008 IEEE Int. Conf. Integr. Circuit Des. Technol. ICICDT 171-175.



- [20] Williams S., Varahramyan K. & Maszara W. 1999. Statistical optimization and manufacturing sensitivity analysis of 0.18 m m SOI MOSFETs. Microelectron. Eng. 49: 245-261.
- [21] Williams S. & Varahramyan K. 2000. A New TCAD-Based Statistical Methodology for the Optimization and Sensitivity Analysis of Semiconductor Technologies. IEEE Trans. Semicond. Manuf. 13: 208-218.
- [22] Aziz M. N. I. A., Salehuddin F., Zain A. S. M. & Kaharudin K. E. 2016. Electrical Characteristics of PMOS Bulk MOSFET and PMOS Silicon-oninsulator (SOI) MOSFET Device. ARPN Journal of Engineering and Applied Sciences. 11(10): 6315-6318.
- [23] Salehuddin F. *et al.* 2011. Optimization of input process parameters variation on threshold voltage in 45 nm NMOS device. Int. J. Physical Sciences. 6(30): 7026-7034.
- [24] Myers R. H. & Montgomery D. C. 2001. Response Surface Methodology: Process and Product Optimization Using Designed Experiments.
- [25] Roy R. 1990. A primer on the Taguchi Method.
- [26] Kamaruddin S., Khan Z. A. & Foong S. H. 2010. Application of Taguchi Method in the Optimization of Injection Moulding Parameters for Manufacturing Products from Plastic Blend. Int. J. Eng. Technol. 14, 152-166.
- [27] Elgomati H. A. *et al.* 2011. Optimizing 35nm NMOS devices VTH and ILEAK by controlling active area and halo implantation dosage. In IEEE Regional Symposium on Micro and Nanoelectronics (RSM). pp. 286-290.
- [28] Phadke M. S. 2001. Quality Engineering Using Robust Design.
- [29] Yadav V. K. & Rana A. K. 2012. Impact of Channel Doping on DG-MOSFET Parameters in Nano Regime-TCAD Simulation. Int. J. Comput. Appl. 37: 36-41.
- [30] ITRS. 2013. International Technology Roadmap Semiconductor.