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DESIGN OF LOW POWER 16X16 SRAM ARRAY USING GDI LOGIC WITH DYNAMIC THRESHOLD TECHNIQUE

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ABSTRACT

The highlighted concept of this paper is to employing body bias concept in the design of 16 bit SRAM Array to operate the circuit for low voltage power supply and for achieving low power consumption and consequently reducing transistor count the GDI(Gate Diffusion Input) technique is adopted. By adopting GDI Technique design complexity levels also reduced. By utilizing Dynamic threshold logic and GDI Logic for SRAM cell design to effectively reduce static power dissipation and propagation delays compared to the resistive load inverter being used in previous designs. Peripheral components such as row decoder, precharge circuit, sense amplifier and column decoder has been designed and assembled to form SRAM array using Cadence (version 6.1.5) simulation tool. Standard UMC180 library is used for designing. Supply voltage of0.4V is considered. Transient responses for read and write operations for both logic-1 and logic-0 have been analysed with operating Frequency 25MHz and the access time for read and write operation is 10ns. Power consumption of 101uW is measured for complete SRAM array.

Keywords: sram, gdi logic, dynamic threshold, cadence.

INTRODUCTION

Design of 6T SRAM become new challenge in the storage requirement in the SOC (System on Chip) at Nano meter technology because of threshold voltage variations. Threshold voltage variations may affect the stability and read/write process in the SRAM. This paper is an extension of previous designs such as resistive load inverter based and CMOS logic [1]. While using CMOS logic the output voltage swing depends up on the V_{DD} it causes more power consumption and it takes more area because of pull up and pull down networks and using more number of PMOS transistors the power consumption increases. For reducing Leakage currents transistor scaling is the effective method. Including transistor scaling Supply voltage scaling is a well-known method to reduce the power consumption of a circuit. The leakage is reduced due to smaller voltage differences between the drain, source and body of a transistor [2] so in this paper the complete digital blocks in the memory architecture are designed with GDI (Gate Diffusion Input) logic is shown in Figure-1.

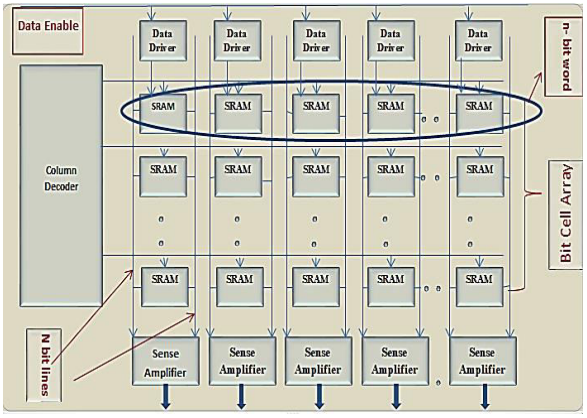

Figure-1. The block diagram of memory architecture.

The GDI cell contains three inputs: G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS) as shown in Figure-3. While maintaining low logic complexity design low power consumption achieved [3]. Another important concern is low voltage power supply, in this paper the total circuit is operated at 0.4V power supply we make this practical possible with the help of Dynamic Threshold logic. The technique behind the dynamic threshold MOS is that the input voltage Vbs is greater than Zero for NMOS and for PMOS it is negative and hence the threshold voltage can be reduced accordingly. The DTMOS structure uses both the gate and the body terminal to provide the signal input [4]. Since in DTMOS both the gate and the body terminal are shorted through resistive network which acts as voltage divider

$$V_{bS} = V_G(R1 // R2) \quad (1)$$

so the forward body bias and reverse body bias both happens at the body terminal with respect to gate input is shown in Figure-2 where R1 and R2 are Poly resistors.

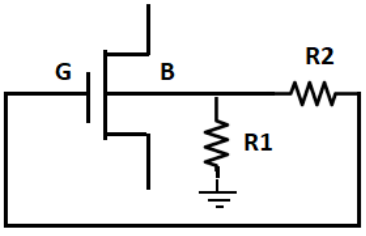

Figure-2. Dynamic threshold logic.

The relation between input signal and V_T is described using the following equation

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Considering body biasing, V_T is given as

$$Vt = Vto + \gamma\left(\sqrt{(\varphi s + Vbs)} - \sqrt{\varphi s}\right) \quad (2)$$

Where γis the body effect factor and V_t is threshold voltage due to body effect. From equation 1 threshold voltage variations can possible with respect to variable body bias without affecting the stability of the SRAM at low power supply [9].

This paper has five sections along with the current introductory Section. Section II covers brief introduction of working principle and performance parameters of SRAM. Section III discusses design and simulation of SRAM peripherals, i.e., Decoder and sense amplifier and 16X16 SRAM array. Section IV consists of all possible outcomes and their discussions. Finally, Section V summaries important conclusions of the research work carried out.

SRAM CELL

The basic SRAM cell is designed with back to back connected CMOS inverters to form a latch for storing 1 bit of data storage (either 0 or 1). In this paper CMOS inverters are replaced with GDI inverters with random threshold (V_t) variation as shown in the Figure-3. The advantage of Gate Diffusion Input is better logic swing and it is good advantage to data storage. Two pass gates are arranged to access the data this connects the latch to two complementary bit line column's (BL and BL_B) and the two pass gates are activated when word line asserted one(WL=1) as shown in Figure-5. When WL=0 the two pass gates are isolated to the latch and the previous data in the latch is unchanged.

During write/read process the threshold voltage of pass gates gradually decreases from the initially high value till when the WL=1. For non-destruction of data during read operation and modification of data during write operation the W/L ratios of pass gates are adjusted accordingly and Pull up and pull down network in GDI cell are maintained in the ratio of 2:1.The current equation for the conventional CMOS when it is in saturation

$$Id = K\frac{W}{L}(Vgs - Vt)^2 \quad (3)$$

Because of Dynamic threshold technique the above equation will becomes from equation (2)

$$Id = K\frac{W}{L}(Vgs - (Vto + \gamma\left(\sqrt{(\varphi s + Vbs)} - \sqrt{\varphi s}\right))^2 \quad (4)$$

From equation (1)

$$Id = K\frac{W}{L}(Vgs - (Vto + \gamma\left(\sqrt{(\varphi s + VG(R1//R2)}\right) - \sqrt{\varphi s}))^2 \quad (5)$$

If Vgs is more positive it will become forward body bias if Vgs is negative then it is a reverse bias the current equation 5 will become for the case of Dynamic Threshold technique

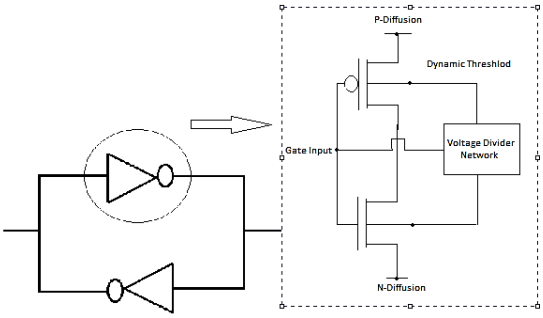

Figure-3. Schematic of GDI latch (GDI inverter with dynamic threshold).

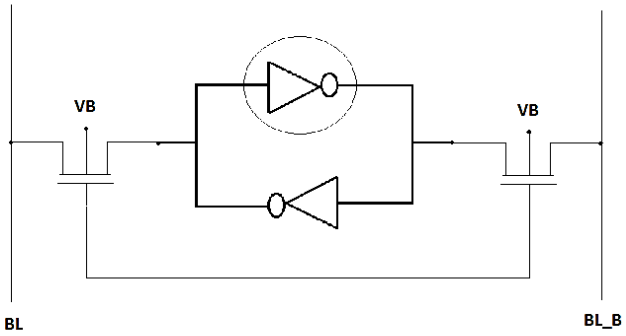

Figure-4. Schematic of 6T SRAM cell.

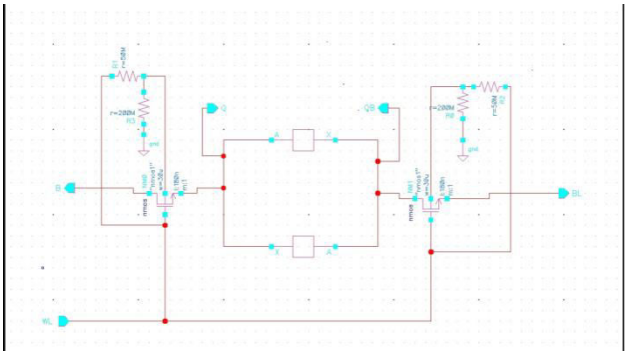

Figure-5. Schematic of 6T SRAM cell with dynamic threshold.

Write operation:

When WL=1 the two access transistors are activated the data to be written is fed to the bit lines during write operation. The variation in the bit lines desired data written in to the cell

Read operation:

During read operation the WL=1 and the bit lines are charges or discharges according to the data stored in the cell. Voltages on the bit lines are compared by the sense amplifier to determine the storage value

The dimensional parameters of PMOS and NMOS transistors in the GDI cell and access transistors are

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Table-1. Dimension parameters of GDI and PG transistors.

Parameters	GDI PMOS	GDI NMOS	Pass gate
Channel Length(L)	180nm	180nm	180nm
Channel Width(W)	720nm	360nm	30um

COLUMN/ROW DECODER AND SENSE AMPLIIFER

The one of important peripheral in the design of 16X16 SRAM array is decoder. A 4:16 decoder is required to access 16X16 SRAM array. The output of decoder is used to select the WL for each column/row of the SRAM array. The schematic of 4:16 decoder is shown in Figure-6.

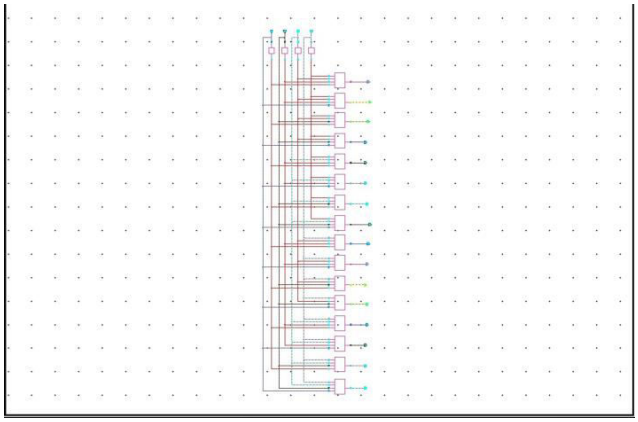

Figure-6. A 4:16 decoder.

AND Gate is essential cell in the design of decoder. The conventional CMOS AND gate requires six transistors but in this paper GDI AND gate is used in the design of 4:16 decoder which requires only two transistors similar to the inverter is shown in Figure-7. One of the input is fed through gate input and another input at N-diffusion. P-diffusion is connected to $V_{DD.}$

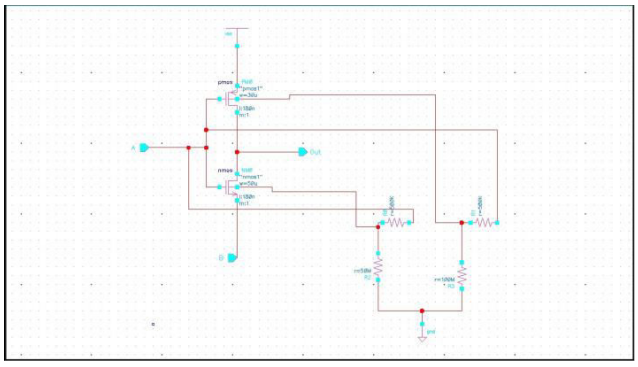

Figure-7. Schematic of GDI and D with dynamic threshold.

Table-1 shows the outputs of 4:16 decoder that select specific WL and RL for corresponding column and row of SRAM array

Table-2. Selection of word line.

Inputs				Output selection (WL/RL)
A	B	C	D	
0	0	0	0	WL0
0	0	0	1	WL1
0	0	1	0	WL2
0	0	1	1	WL3
0	1	0	0	WL4
0	1	0	1	WL5
0	1	1	0	WL6
0	1	1	1	WL7
1	0	0	0	WL8
1	0	0	1	WL9
1	0	1	0	WL10
1	0	1	1	WL11
1	1	0	0	WL12
1	1	0	1	WL13
1	1	1	0	WL14
1	1	1	1	WL15

Sense amplifier

Differential input sense amplifier is used in this paper as shown in the figure. During the read operation bit cell state inadvertently affected due to large chare stored on the bit line. So to detect correct value stored in the bit cell the differential input sense amplifier is required. It compares the small voltage differences in the bit line and bit line barand extracts the correct stored value it also helps from noise due common mode voltage variation.

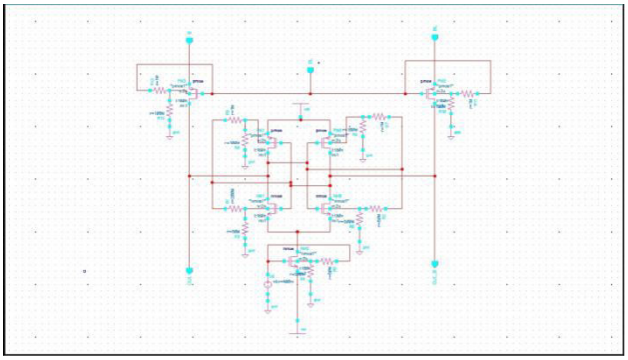

Figure-8. Schematic of differential sense amplifier.

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It consists of two back to back connected inverters (NM0 and PM0, NM1 and PM1) and a biasing current source NM2 is used to maintain a constant current in the circuit. Two inverter gate inputs are connected bit line and bit line bar lines which come from the SRAM cell. PM2 and PM3 transistors are a part of pre-charge unit is shown in the Figure-8.

Table-3. The dimensional parameters of PMOS and NMOS transistors in the differential sense amplifier.

Transistors	Channel length(L)	Channel width(W)
NM0	180nm	2um
PM0	180nm	2um
NM1	180nm	2um
PM1	180nm	2um
NM2	180nm	20um

SRAM array

In this paper 16X16 SRAM array is designed with the storage capability of 4KB (2^nX m) where n is the no of address lines and m is the no of storage cell and tested the same for 256 bits. It includes 16 differential sense amplifiers along with 16 pre charge circuits and 4:16 Write/Read decoder is used to select specific word/Read enable lines.

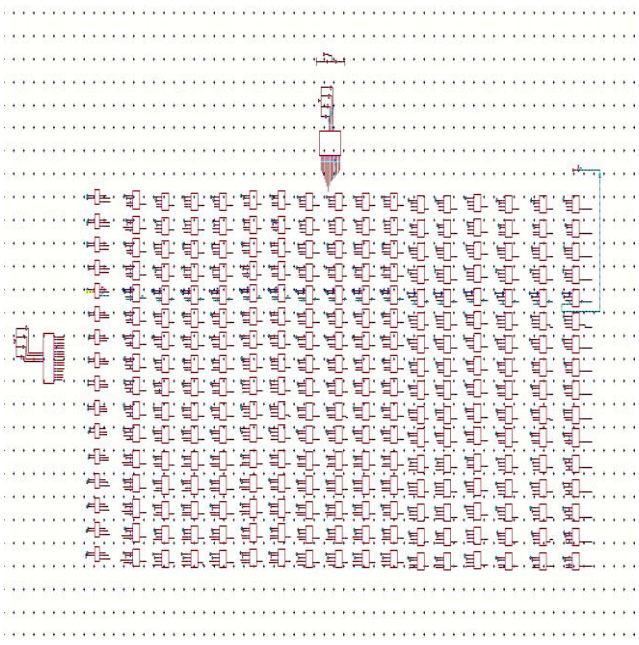

Figure-9. 16X16 SRAM array.

RESULTS

This section discuss the simulation results of 4:16 decoder and 16X16 memory array for write 1 and read 1 operation and write 0 and read 0 operations. The simulation tests are carried out using cadence standard UMC 180nm Technology. The transient response of decoder tested at with two input combinations. The first one is ABCD=0100 fourth output is selected is shown in Figure-10 and the second combination ABCD=1111 then the last line is selected is shown in Figure-11.

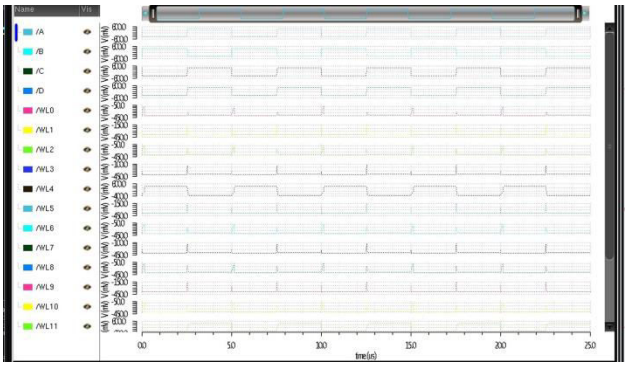

Figure-10. Transient response of 4:16 decoder for ABCD= 0100.

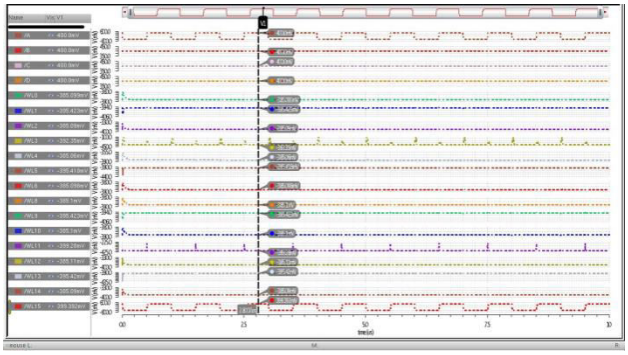

Figure-11. Transient response of 4:16 decoder for ABCD= 1111.

The transient responses of 16X16 SRAM Array for write 0 and read 0 operations. According to the output WL4 of decoder the corresponding PG of SRAM cell are enabled. Data input of write driver asserted low for write -0operations. This makes output q4 low and qb4 high. Thus logic 0 is written into the memory cell. For read-0 operation, sense enable signal is made high enabling corresponding sense amplifier. Specific sense amplifier reads logic 0 from memory cell.

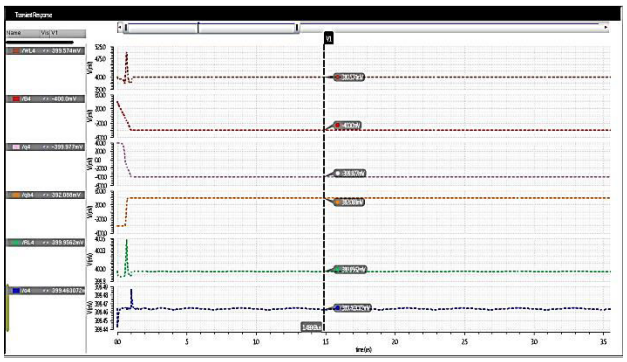

Figure-12. Transient response of SRAM array for write 0 and read 0 operations.

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The transient responses of 16X16 SRAM Array for write 1 and read 1 operation. According to the output WL4 of decoder the corresponding PG of SRAM cell are enabled. Data input of write driver asserted high for write -1 operation. This makes output q4 high and qb4 low. Thus logic 1 is written into the memory cell. For read-1 operation, sense enable signal is made high enabling corresponding sense amplifier. Specific sense amplifier reads logic 1 from memory cell.

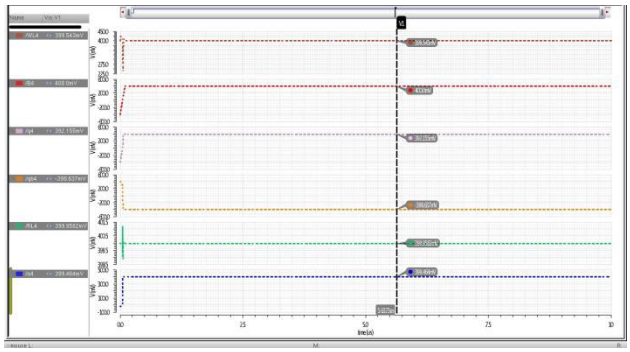

Figure-13. Transient response of SRAM array for write 1 and read 1 operation.

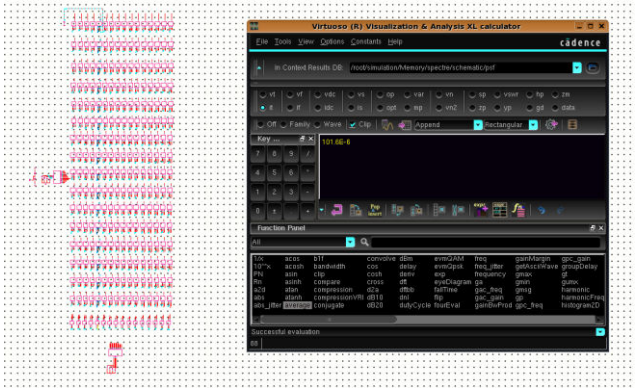

Figure-14. Power analysis of 16X16 SRAM array.

Table-4. Performance results.

PARAMETERS	RESULTS
Supply Voltage	0.4V rail to rail
Max Operating Frequency	25MHz
Total Current	250uA
Avg Power Consumption	101uW
Read Access Time	10nS
Write Access Time	10nS

CONCLUSIONS

A Low power 16X16 SRAM array is designed for storing 256 bits. Peripheral components such as row decoder, sense amplifier including precharge circuit and column decoder has been designed and assembled to form SRAM array. Differential type sense amplifier is used for noise reduction. GDI Logic SRAM storage cell is used to avoid static power dissipation. Pulse input signal with a peak to peak voltage of 0.4V (rail-rail) and Supply voltage of 0.4V is considered Transient responses for read and write operations for both logic -1 and logic -0 have been analyzed. Power consumption of 101.6 uW is measured for complete SRAM array. SRAM array is designed in Cadence tool (version 6.1.5) using Schematic editor Virtuoso. Standard UMC180 library (i.e., 180nm technology node) is used for designing. 25MHz operating frequency is achieved.

AUTHORS' CONTRIBUTIONS

The total work completed by the first author as a part of his research work. The basic idea behind the work suggested by the second author and complete work including results verification and analysis completed under the observation of third author.

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REFERENCES

[1] R. Bisht, P. Aggarwal, P. Karki and P. Pande. 2016. Low power and noise resistant 16×16 SRAM array design using CMOS logic and differential sense amplifier. 2016 International Conference on Computing, Communication and Automation (ICCCA), Noida. pp. 1474-1478.

[2] D. Ho, K. Iniewski, S. Kasnavi, A. Ivanov and S. Natarajan. 2006. Ultra-low power 90nm 6T SRAM cell for wireless sensor network applications. 2006 IEEE International Symposium on Circuits and Systems, Island of Kos. p. 4, doi: 10.1109/ISCAS.2006.169353.

[3] A. Morgenshtein, I. Shwartz and A. Fih. 2010. Gate Diffusion Input (GDI) logic in standard CMOS nanoscale process. 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, Eliat. pp. 000776-000780.doi: 10.1109/EEEI.2010.5662107.

[4] N. Lindert, T. Sugii, S. Tang and Chenming Hu. 1999. Dynamic threshold pass-transistor logic for improved delay at lower power supply voltages. in *IEEE* Journal of Solid-State Circuits. 34(1): 85-89, doi: 10.1109/4.736659.

[5] K. C. Shah, D. N. Gandhi and B. H. Nagpara. 2013. Design and Analysis of 256 Bit SRAM in Deep

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.

Submicron CMOS Technologies. Journal of Information, Knowledge and Research in Electronics and Communication Engineering. 2: 812-817.

[6] P.S. Bellerimath and R. M. Banakar. 2013. Implementation of 16X16 SRAM Memory Array using 180nm Technology. International Journal of Current Engineering and Technology. pp. 288-292.

[7] Kanika Kaur and AnuragArora. 2013. Performance of Low power SRAM Cells on SNM and Power Dissipation. International journal of emerging Trends & Technology in Computer Science (IJETTCS) ISSN 2278-6856, 2(2).

[8] Mr. Abishek Verma *et al.* 2014. Int. Journal of Engineering Research and Applications. Effect of Threshold Voltage on Various CMOS Performance parameter. ISSN: 2248-9622, 4(4): 21-28.

[9] Samira Ataei and james E. Stine @ A 64 kb Multi-Threshold SRAM Array with Novel Differential 8T Bitcell in 32 nm SOI CMOS Technology. 978-1-5090-4391-0/16/$31.00 ©2016 IEEE.