VOL. 12, NO. 23, DECEMBER 2017 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences
©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.
www.arpnjournals.com

# DESIGN AND IMPLEMENTATION OF EMBEDDED TRACKING SYSTEM USING SPATIAL PARALLELISM ON FPGA FOR ROBOTICS

Noor Aldeen A. Khalid and Muataz H. Salih
School of Computer and Communication Engineering, Universiti Malaysia Perlis (UniMAP) Perlis, Malaysia
E-Mail: nooraldeen4561@gmail.com

**ABSTRACT**

The robot tracking system is one type of utilization system on a mobile robot and generally utilized as a part of numerous perspectives, for example, security or military. In this project, we implemented an active robot tracking system used FPGA platform. The robot can identify and track objects by using Infrared long range (IR). Perception approach and motion planning is the most essential part in this project. We used Two long range IR sensors for the tracking process and to distinguish any moving object while, the DE0-Nano board is the project platform and the characteristic of FPGA offer programmability and makes it easier to implement on different mobile robot platforms. We integrated Sensors with the DE0-Nano board. In our project a structure VHDL coding is used for design the robot tracking system and Quartus II 13.0sp1 as a development CAD tool. The implementation of complex tracking system with FPGA platform (DE0-Nano) was possible because of the rich logic elements, a specific sensors characteristics testing and robot stability was carried out to master those sensors and robot. The result for this project that already got, shown the frequency for DE0-nano achieved up to 1.3 GHz, also the total logic elements we used for this project is 4,022 and shown the output reading voltage of the IR sensor is high reflectivity for the white colour object compared to another colours like blue and black, also the long detection distance.

**Keywords:** embedded system, tracking system, spatial parallelism, FPGA design.

## INTRODUCTION

The field of robotics was seeing a massive impact on daily life. The robots were invented for overcoming the problem related to insufficient resources. Moreover, they are able to accomplish the tasks which are highly risk for the humans. We designed and implemented the robot tracking system on FPGA. Nowadays, robotics has been widely applied in the areas of security, service etc. The robot tracking system helps us carry out several tasks successfully. On the other hand, some of the important problems in the robot tracking system include object discovery, path planning are explored. We used two long-range Infrared (IR) beams for tracking any type of object, using these sensors was able to resolve the object detection and the tracking issues. Furthermore, we selected the DE0 Nano board for mastering these sensors and controlling the robot motors through L293D chip to let the robot moved in different directions. The DE0 Nano refers to a compact-sized FPGA development platform; which is more suited for the portable designing projects like a robot. The configurable logic block used in the FPGA helps in updating the design easily. Also, the DE0 Nano platform consists of rich I/O pins, and enables it to simultaneously handle huge data volume and achieve higher data processing speeds with frequency up to 1.3GHz. The DE0 Nano platform solves the problems related to a low processing speed and I/O and resource limitation. We interfaced the DE0 Nano platform with the sensors and the robot. Thereafter, we used the VHDL and such Mega function modules for overcoming the design-based challenges. The Quartus II 13.0sp1 CAD tool software acted as the designing tool for simulating the VHDL coding or the block diagram for validating the performance of our design.

## RELATED WORK

The FPGAs are integrated circuits that can be customised by the user for implementing arbitrary digital functions. The modem FPGAs can combine the general logic resources with the microprocessors, programmable interconnections, multipliers, networking, memories, the delay/phase locked loops and such other cores for designing a more versatile System on Chip (SoC).

FPGA provides a highly flexible and integrated platform, it's processing fast, using FPGA to complete fixed function modules, such as filters or any other design, down-converter, a memory, co-processors has a very significant advantage [1].

**Table-1.** Comparison betweenFPGA and DSP[1].

| | **FPGA** | **DSP** |
|---|---|---|
| Power | Low | High |
| Difficulty Of Development | Hard | Easy |
| Volume | Small | Big |
| MAC Speed | Parallel Processing | Speed Limited |
| Parallel Processing | Parallel Processing | Serial Processing |
| Basic Development Language | V/A HDL And etc. | C, Assembler Language etc. |

FPGAs are very popular in all of the application domains. Initially, the FPGAs were used in the form of the digital glue logic or only for prototyping, however, today; they are generally applied as integral components of complex designs like communications, consumer electronics, space systems and military. The FPGAs are

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


becoming very popular not only due to a decreasing performance gap between the ASICs and the FPGAs but also due to better reconfiguration flexibility of the system that helps in product development, its maintenance and obtaining updates. They are one of the best and most popular hardware platforms for implementing and testing the digital designs and are regularly used by the educators and circuit designers. Furthermore, they are also used by the people who contribute towards the online design resources like Open source, who assess and justify their open source designs using the different FPGA chips. The validation and testing of designs using the FPGA chips improves the confidence and the product credibility of the design resources[2].

Robotics must possess the basic ability to track the objects if it has to work in different dynamic environments. Now, moving objects are the interacting subjects for the robot. Tracking and proper motion detection are the basic requirements of several mobile robot applications[3].

## TEMPORAL AND SPATIAL PARALLELISM

All the computational systems are made of interconnecting components, and based on their abstraction level at which these systems are studied; the components include gates, memories, transistors, arithmetic units, registers, or processors. At every abstraction level, there are 2 basic methods in which these components are composed for creating parallel computing structures, i.e., temporal parallelism and spatial parallelism.

To explain further, the task space is parallelised. The major difference between the spatial and the temporal parallelism is that the spatial parallelism consists of several tasks that are simultaneously executed[4]

Stream calculation through pipelining approach can gain the throughput without taking extra space from memory size. Its becomes a suitable for FPGA-based specific operation. In addition, specific operation in FPGA usually gave a high performance and less power consumption. On the other hand, FPGA manufacture with semiconductor parts has expanded the enforcement performance and efficiency because the on-chip integration and high response Input/ Output data. Spatial parallelismable to duplicate processing to make multiple tasks can be executed at the same time. as shown in Figure-1 [5].

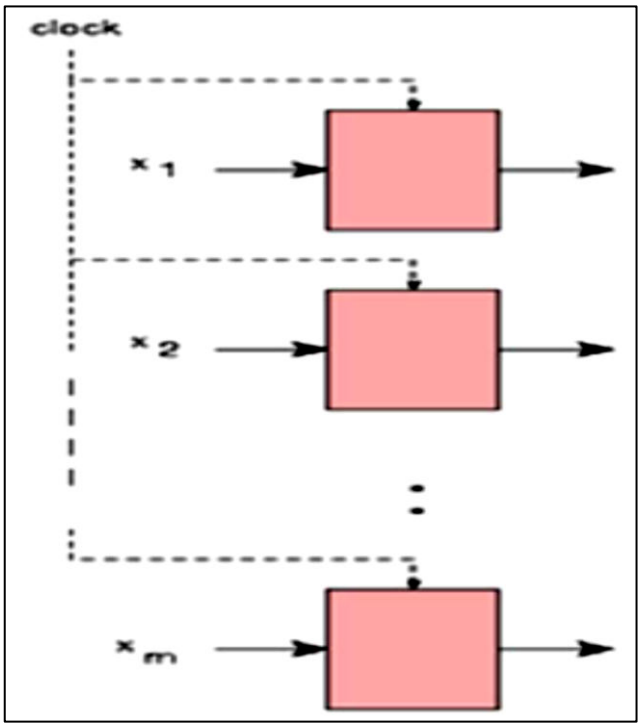


**Figure-1.** Spatial parallelism [5].

## METHODOLOGY

The DE0-Nano Board used in the FPGA platform has been implemented in many robots. Some of the features of this platform include an Altera Cyclone IV FPGA (having 22,320 logic elements), 2 Kb EEPROM, 32 MB SDRAM, and 64 Mb of a serial layout memory device along with the processor of 1.3 GHz. For attaching actual detectors, the DE0-Nano Board includes an 8-channel semiconductor with a 12-bit Analogue-to-digital converter also contains 13-bit Analogue Devices and a 3-axis (X, Y, Z) accelerometer device.

The DE0-Nano Board consists of a built-in USB Blaster for the programming of the FPGA platform, and the board can be turned on using an USB port or an external power source. The board also consists of developed headers which use many Terasic family cards or such similar appliances like engines and motors. The input and the output ports include 2 push-buttons, 8 user LEDs and 4 dip-switches. The DE0 Nano board was described in Figure-2 and 3[6].

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


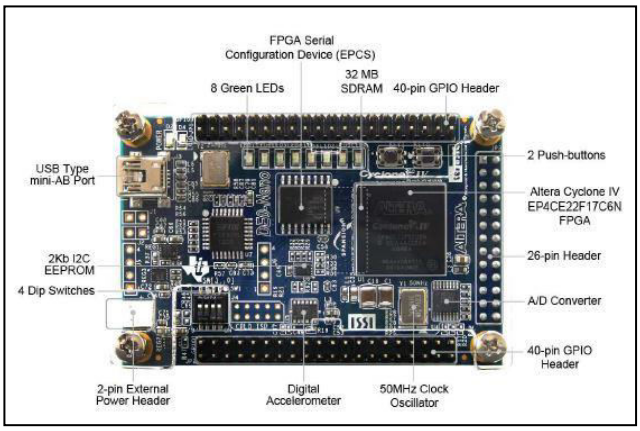


**Figure-2.** The top view of the DE0-Nano Board.

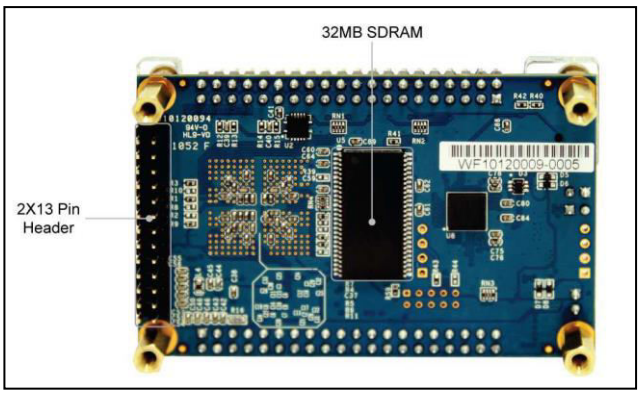


**Figure-3.** The bottom view of the DE0-Nano Board.

**X/Y/Z axis for the DE0-Nano accelerometer**

The accelerometer was tested (X, Y, Z) in the DE0-Nano Platform with the help of the Control Panel in the Terasic Source, as described in Figure-4.

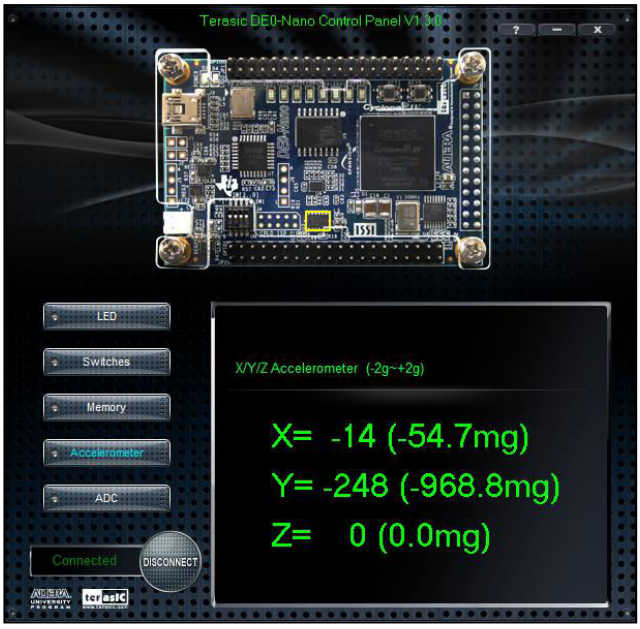


**Figure-4.** The output data of the accelerometer in the control panel.

The main task for special processing forgaininga high performance, less cost to efficiency ratio and low power consumption, also improved the capability. Spatial parallelism is duplicate processing to make multiple task can be executed at the same time.

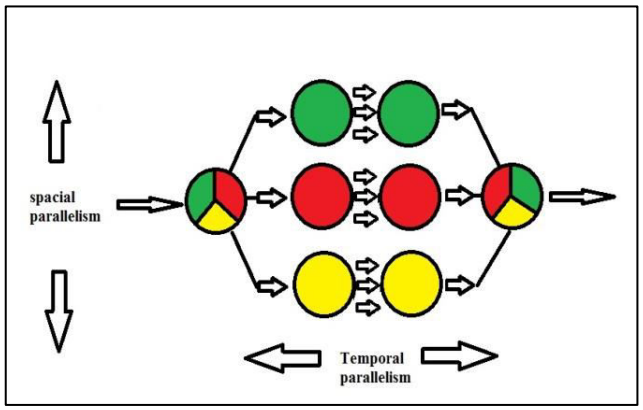


**Figure-5.** Spatial and temporal parallelism.

The signal received by the sensors was processed. After this processing, the data was transmitted to the main central computing unit of the FPGA controller, as the input data for initiating the action and then obtaining the output Figure-6 shown the top level design.

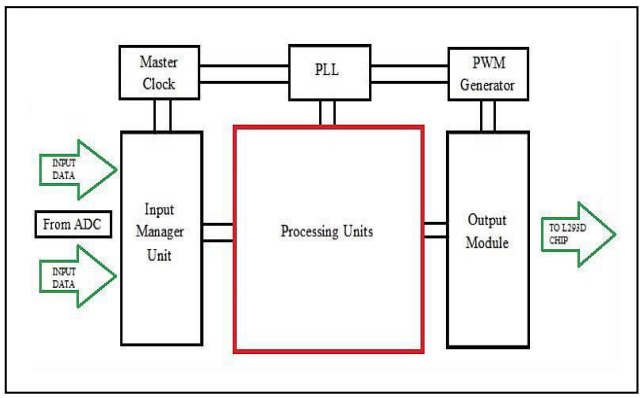


**Figure-6.** A top view of top level design.

**IR SENSOR**

The IR sensor estimates the reflected light intensity from the moving object for determining its distance from the IR source. However, some features of the IR sensor must be activated for it to work efficiently. Initially, the object should have the highly reflecting surface. Next, the ratio of the direction or the angle of the surface to the IR sensor must be considered. The sensor cannot work effectively in a poor lighting, angle relative to IR and low reflectivity from the surface of the object. The IR sensor has a detection distance of 100-550 cm and is basically used for tracking moving objects. These sensors were tested based on the features presented in the diagram and the results are shown in the data sheet. For overcoming the limitation of the IR sensor, wherein there was an interference in the data due to the coloured object's

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


reflectivity, many flat-surfaced coloured objects were used. The objects colours were blue, black and white.

Two IR long range sensors (GP2Y0A710K0F) for detecting and tracking the moving object. A robot could detect the motion of the object when it entered the area containing the IR light beam. The IR sensor was described in Figure-7.

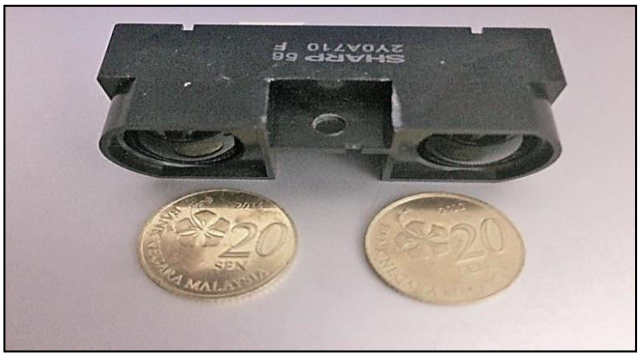


**Figure-7.** GP2Y0A710K0F IR sensor.

The signals obtained from the sensors were transferred using the on-board ADC to the digital signal which could be read by the DE0 board. The ADC type of NS ADC128S022 was used, which used a 12-bit A/D converter input for accessing and interpreting the analogue input value from 0 to 3.3V, which was then rejected by the DE0 Nano board. With regards to the safety problem, it only received and accepted 3.3V. For obtaining an accurate value, the clock frequency assigned to the ADC from 0.8 to 3.2 MHz. Despite these alterations, the ADC worked properly and showed a productivity rate of 50 to 200 ksps, which helped it receive 8 input signals [7].

For controlling the direction of the motor, we generated a VHDL block. Any disparity noted in the output values of the L293D chip allowed the robot to move in a completely new direction. The L293D consisted of 2-H bridge driver circuits for controlling the 2 DC motors and also simultaneously functioning. Out of the 16 L293D chip pins, the 2 and 7 pair, and the 10 and 15 pin pair were used for controlling the motor operation. An input of 00 or 11 stopped the movement of the respective motor, while an input value of 01 and 10 helped in rotating the motor either in a clockwise or an anticlockwise direction. The Pins 1 and 9 were enabled for activating the motor.

**Table-2.** Commands for controlling the motor operation.

| Direction | ENA | ENB | Command (RA, RB, LA, LB) |
|---|---|---|---|
| Forward | 1 | 1 | 1010 |
| Backwards | 1 | 1 | 0101 |
| Right | 1 | 0 | 1000/1001 |
| Left | 0 | 1 | 0010/0110 |

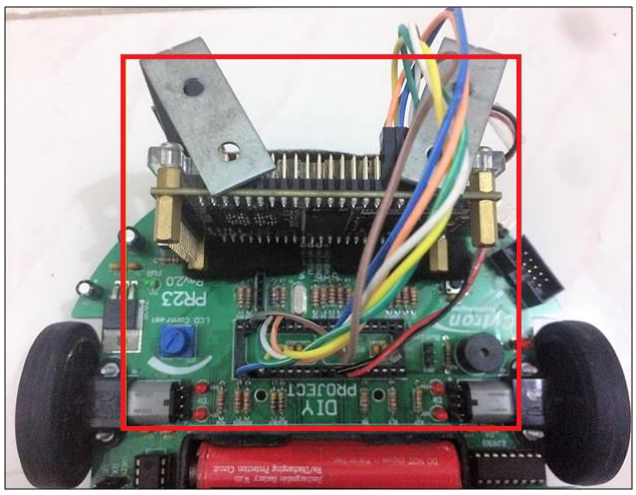

**Figure-8.** Robot controlled by using FPGA DE0-Nano.

A proper synchronization between the wheels of the 2-wheeled robot is essential for the robot stability. The VHDL block developed in the 2nd Phase on this 2-wheeled robotic platform was implemented. The robot was tested whether if it could move in a straight line in the forward direction, indicating that the robot was stable. If the robot was unstable, it veers towards the right or the left directions. We modified the VHDL coding till the robot could move straight forward.

## RESULTS

The IR sensor estimates the reflected light intensity from the moving object for determining its distance from the IR source. However, some features of the IR sensor must be activated for it to work efficiently. Initially, the object should have the highly reflecting surface. Next, the ratio of the direction or the angle of the surface to the IR sensor must be considered. The sensor cannot work effectively in a poor lighting, angle relative to IR and low reflectivity from the surface of the object. These sensors were tested based on the features presented in the diagram and the results are shown in the data sheet.

The testing procedure repeated by placing the object nearer to the sensor for obtaining the output reading for a different distance value, under different lighting conditions Table-3 shown the result for different object colour detection by using oscilloscope.

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


**Table-3.** Output voltage with different distance of reflective objects.

| **Distance** (cm) | **White object** (v) | **Blue object** (v) | **Black object** (V) |
|---|---|---|---|
| 50 | 2.71 | 2.63 | 2.45 |
| 100 | 2.16 | 2.00 | 1.80 |
| 150 | 1.80 | 1.63 | 1.52 |
| 200 | 1.62 | 1.57 | 1.48 |
| 250 | 1.53 | 1.46 | 1.35 |
| 300 | 1.45 | 1.37 | 1.20 |
| 350 | 1.36 | 1.20 | 1.13 |
| 400 | 1.25 | 1.22 | 1.1 |
| 450 | 1.1 | 1.00 | 0.98 |
| 500 | 0.99 | 0.96 | 0.95 |

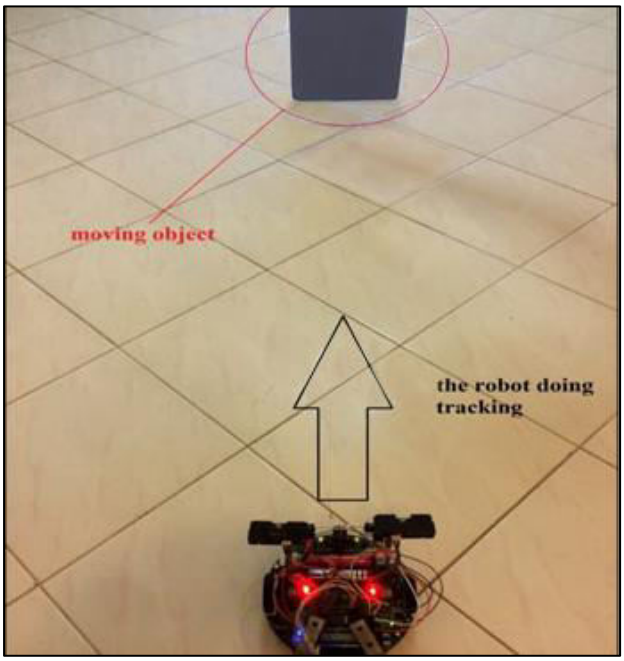


**Figure-9.** The robot the blue object.

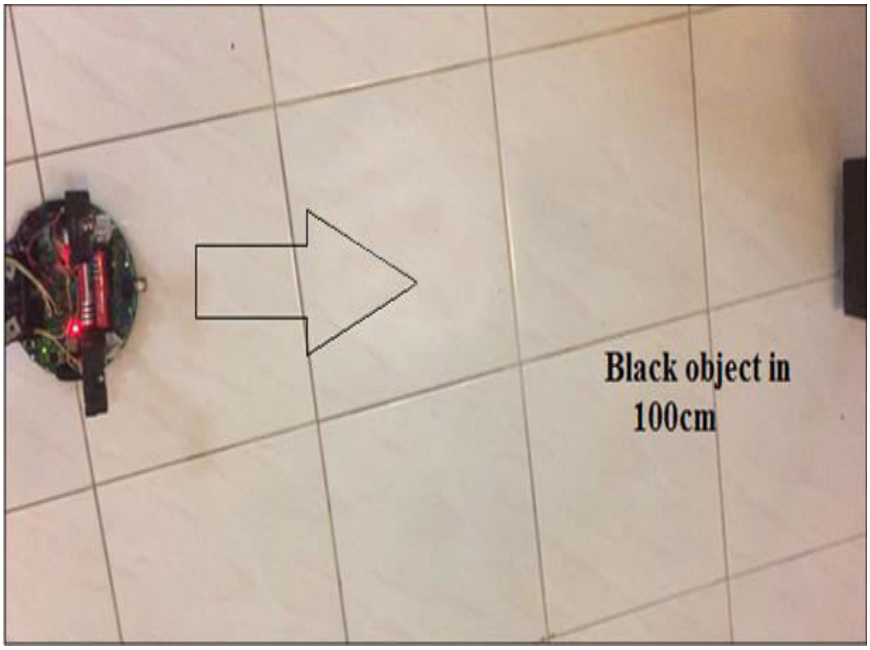


**Figure-10.** Tracking black object at a distance of 100 cm.

## IN-SYSTEM MEMORY READING

In-system memory very important function to check the sensors reading and get it output patterns, other ways used for testing, but in system memory more advanced to get the reading from the sensors and used it in coding design. In-System Memory Editor was used for observing and updating the memories using JTAG port connection. The In-System Memory Editor allows one to design a complicated FPGA platform. The JTAG interface was helped in accessing all the memories to read and write the commands when programming a device. After testing the changes in the FPGA memory all problems were solved in the design while running the device. As described in the figures, some of the sensor readings were carried out based on the In-system memory Figures 11and 13 shown the reading for the IR sensor, Figure-13 shown the robot.

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


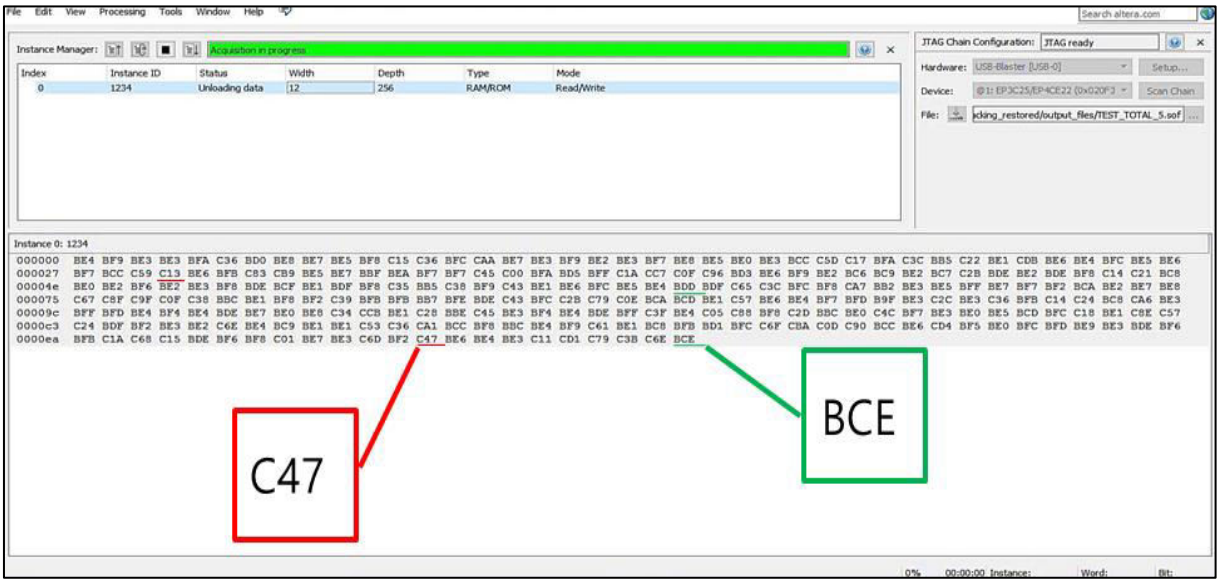


**Figure-11.** IR readings when detect the object.

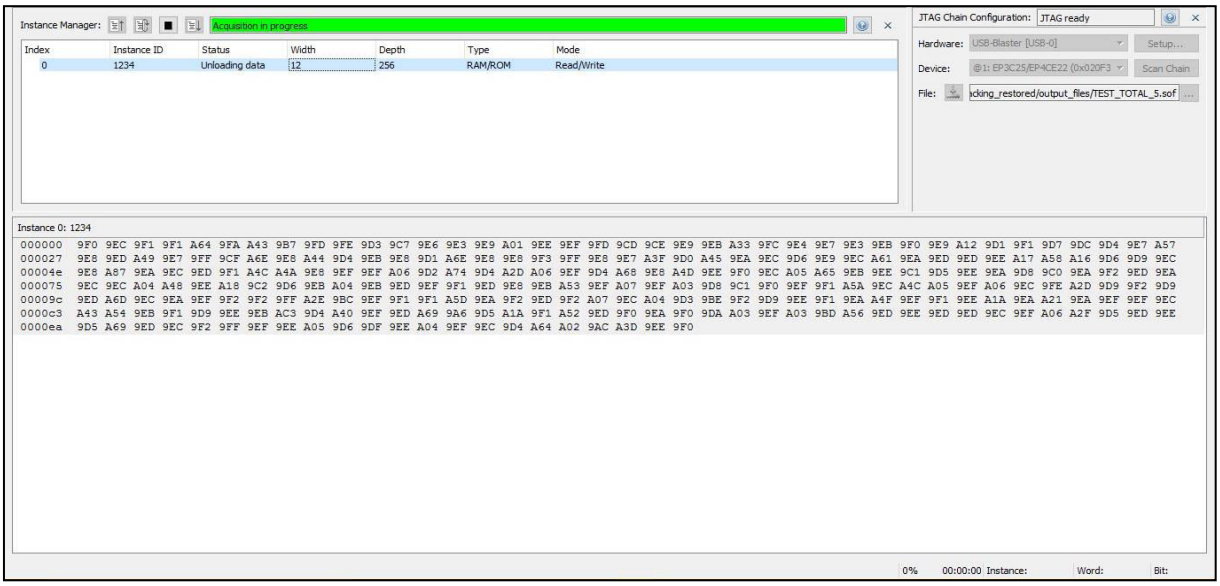

**Figure-12.** IR readings when the object was at a distance of 200 cm.

**Table-4.** Total Tapped Resources for the Projact.

| FPGA Recourses | Used by system | Percentage |
|---|---|---|
| Timing Models | Final | _ |
| Total logic elements | 4,022 / 22,320 | 19% |
| Total combinational functions | 4,023/ 22,320 | 18 % |
| Dedicated logic registers | 512 / 22,320 | 3 % |
| Total registers | 520 | _ |
| Total pins | 60 / 154 | 22 % |
| Total memory bits | 50,243 / 608,256 | 9 % |

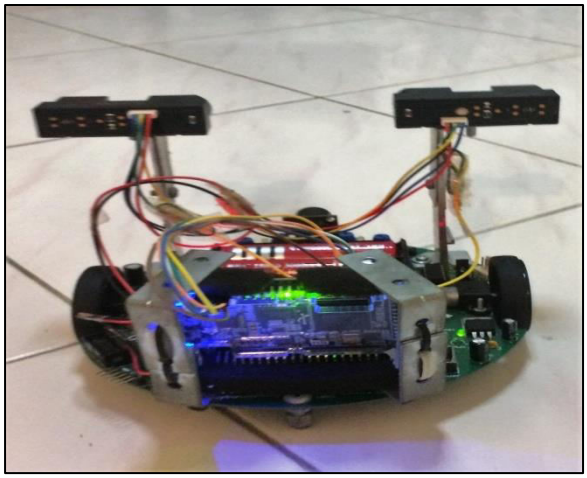

**Figure-13.** Robot with the full component.

©2006-2017 Asian Research Publishing Network (ARPN). All rights reserved.


## CONCLUSIONS

The project objectives are achieved successfully VHDL coding was used for design the robot tracking system using the Quartus II 13.0sp1 software, while the design was implemented on the DE0 Nano board, which was the brain of the system. The CAD tool Quartus II 13.0sp1 software acted as the designing tool for simulating the VHDL coding or the block diagram for validating the performance of this design.

Finally, observed that the robot tracking system was flexible enough to be used in any of the platforms, after some modifications. Besides, the ratio of the logic element proved that the DE0 Nano board could implement the complex tracking system, which is a very encouraging decision for better performance. Furthermore, the FPGA platform could be reconfigured many times, thus providing the designer with many opportunities to change the design without changing the hardware rewiring. Lastly, the frequency of the DE0 Nano Board gave a maximal value of 1.3 GHz, which indicated that the platform's frequency requirement would reach that value and the logic element that used in this project is 4, 022. Hence, using the FPGA technology improved the performance of the system.

## ACKNOWLEDGEMENT

The authors would like to thank the Ministry of Education Malaysia (MOE) for providing the FRGS research grant (Grant no. 9003-00474).

## REFERENCES

[1] D. Huang, J. Yu and G. Li. 2016. Software Radio System Design Based on FPGA. pp. 2655-2658.

[2] C. Ababei, S. Duerr, J. Ebel, R. Marineau and M. G. Moghaddam. 2016. Open Source Digital Camera on Field Programmable Gate Arrays. pp. 151-155.

[3] B. Jung and G. S. Sukhatme. 2010. Real-time Motion Tracking from a Mobile Robot.

[4] D. Kumar, R. Behera and K. Pandey. 2013. Concept of a supervector processor: a vector approach to superscalar processor, design and performance analysis. Int. J. Eng. Res. 29(3): 224-227.

[5] M. H. Salih, O. F. Yousif and M. A. M. Albreem. 2016. Design and implementation of laser missile jamming system using spatial parallelism on FPGA for better performance and throughput. ARPN J. Eng. Appl. Sci. 11(17): 10421-10429.

[6] Http://www.terasic.com. No TitleDE0 Nano User Manual. Available: http://www.terasic.com.

[7] Www.national.com. 2015. ADC128S022 8-Channel, 50 kSPS to 200 kSPS, 12-Bit A / D Converter.