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GAIN DOUBLING TECHNIQUE FOR MULTI-RECYCLED FOLDED CASCODE OPAMP IN DEEP SUBMICRON CMOS TECHNOLOGY

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ABSTRACT

Many analog design techniques and methodology have been devised for better performance of amplifier. Now a day operational amplifier is the backbone of the analog and mixed signal device. It is fundamental block of the many design circuit that utilize high gain, high bandwidth, fast settling time. Op amp is one of the basic building block of analog circuit which has wide range of application such as biomedical application, ADC converter, switched capacitor filter. This paper presents the novel structure of folded cascode amplifier for enhancing the gain. In this quadruple-recycling folded cascode (QRFC) operational transconductance (OTA) amplifier is used to improve the performance over the conventional folded cascode (FC), double recycle, and improved recycle folded structures. The proposed structure uses positive feedback, cross coupled transistors which significantly improve its unity gain bandwidth, DC gain and slew rate as compared to others OTA structures. Circuit level simulations and analysis results done with 180nm CMOS technology validate the improved gain of 95dB for single stage fully differential mode and enhance bandwidth of 185.2 MHz.

Keywords: operational transconductance amplifier, recycling current, folded cascode, DRFC.

1. INTRODUCTION

Generally, the operational transconductance amplifiers (OTAs) are extensively used in analog device (medical application like biosensors, industrial automation sensors) and mixed signal device for their better performance and its high gain. Telescopic and Folded Cascode are two major building blocks for CMOS device in analog circuit but instead of Telescopic the Folded cascode is preferred due to its better gain and signal swing at output [1]. Although multistage amplifiers used for the better gain but in consideration of bandwidth single stage OTAs is better than multistage. It is one of the most important block in analog circuit design which play major role.

Recently one of the most common architecture which is widely used in analog and mixed signal circuit, which is single stage in multistage known as Folded cascode amplifier which is used for its better gain and swing in future CMOS technology process. The folded-cascode amplifier (FC) basically used for low voltage application and operated at very low input signal to achieves high gain and bandwidth [2]. The performance of OTAs is limited due to various factor such as gain, bandwidth, slew rate, voltage swing, etc for this different work used different techniques to increase the gain as well as bandwidth with low power consumption [3]. As we go for improvement of the performance of FC OTA power budget is a major Calibriant (power increased with FC opamp performance improvement techniques). This has to be done without compromising the gain or UGBW with reduction in transconductance (g_m) [4]. On other hand if we use

Multistage amplifier for higher gain which introduce its own problem like, additional pole–zero, noise which degrade the performance of the micro sensor circuit [5]. In addition in the driver transistor PMOS input pair is used in case of NMOS because of its less flicker noise, high dominant pole.

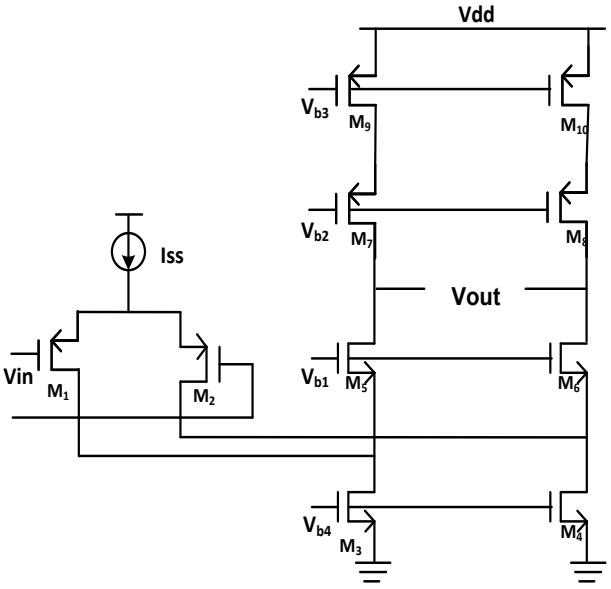

Figure-1. Basic cascode OTA

The simple conventional folded cascode amplifier which is shown in Figure-1.

In which the transistor M_1 and M_2 acts as driving transistor which equally fold the current through input and output [6]. As a result the transistor M_3 and M_4 draws most current through it and acts as a current source without any signal amplification. However there role is limited to provide folding node for the small current which is generated by that two driver transistor. Numerous techniques have proposed in various paper to enhance the significant performance of folded cascode such as recycle the input stage means recycle the current through multipath (double recycle, multi recycle tech.) [7] Also used positive feedback stages, cross coupled transistor to increase the overall performance of the conventional folded cascode stage.

2. CONVENTIONAL FC AND RFC STRUCTURE

The conventional FC and RFC is shown in Figures 1 and 2. To improve the efficiency of conventional FC design the modified FC called Recycle Folded. The input drivers in FC M_1 and M_2 are split in half to produce transistor $M_{1a(b)}$ and $M_{2a(b)}$. As mention before M_1 is twice of that M_{1a} and conduct twice amount of current (g_{m1} = $2g_{m1a}$) for same power consumption. Which conduct fix and equal current I_b /2 (Figure-2). Also, the bottom most transistor M_3 and M_4 also split as $M_{3a(b)}$ and $M_{4a(b)}$ with the ratio of K : 1 which draw more current through it. The cross connection of the current mirror to insure that small current added in the source of M_5 and M_6 (Figure-2). Due to this the small current is amplified by the ratio factor K. Transistor M_{11} and M_{12} are used to maintain the constant drain potential of $M_{3a(b)}$, $M_{4a(b)}$. The transconductance of FC is Gm but due to splitting of transistor the effective transconductance improve [8].

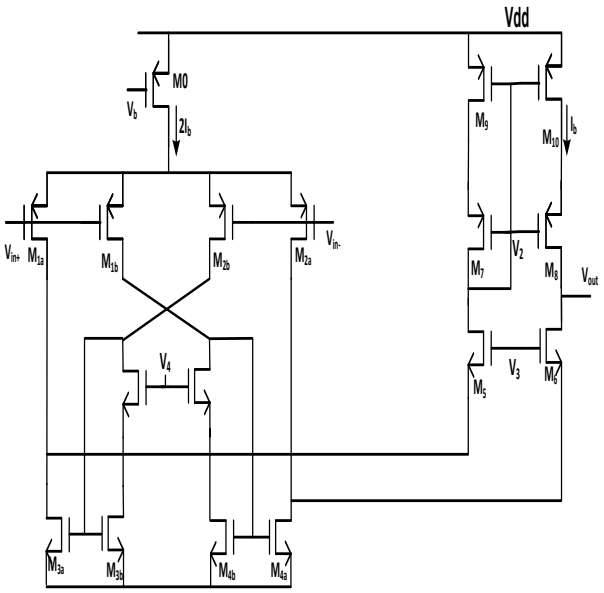

Figure-2. Recycle folded cascode OTA.

In order to achieve enhancement in the transconductance its needful to operate all transistor in saturation region, and follows square law for drain current which is given by,

$$I_d = \frac{1}{2}\,\mu\,Cox\,\frac{w}{L}\,(Vgs - Vth)^2$$

Here, to maintain same power budget for both FC and RFC shown in Fig 1 and 2. Current through M5- M10 is function of K which maintain same budget.

So, the enhance transconductance which help to boost the gain of amplifier also the bandwidth. Design and choose the ratio factor such that it fit into all required parameter but it is limited by ratio factor we can't increase more because the degradation in phase margin. K must be chosen <3 for proper performance. Hence, the transconductance of the RFC is double than FC so that gain, voltage swing, GBW is higher than FC. The small signal analysis of both FC and RFC is as follows,

$$Gm_{RFC} = g_{m1a}\,(1 + K) \quad (1)$$

$$Gm_{FC} = g_{m1} \quad (2)$$

3. PROPOSED QRFC OTA STRUCTURE

Figure-3 shows the Quadruple recycling folded structure (QRFC). The differential pair of input is now replaced with four times as compare with the conventional FC (M1a-M2a, M1b-M2b, M3a-M3b, M4a-M4b) and the current source (M3c-M4c) are divided in ($M3c_1$-$M3d_1$, $M4_{c1}$-M4d1, $M3c_2$-M3d2, M4c2-M4d2). The purpose of this splitting of transistor to reuse the shunt current source more times to increase the performance without more power loss.

Recently, Zushu Yan purposed an double recycling method which is used for folded cascode amplifier in which (M3c-M4c, M3d-M4d) is added in the input structure and the transistor M13, M14, M15, M16 are used for matching the bias current. Since, the bias current in diode connected M3b and M4b are reduced while M1b, M1c, M2b, M2c remains unaltered so, in this paper recycling those current source again which result in higher performance of amplifier. The main aim of this paper is improve the overall output resistance across the output. We propose the robust gain boosting technique for single stage amplifier using the shunt current source reusing and achieve gain 30dB more than the conventional amplifier without compromising stability.

3.1 Circuit description

The Figure-3 shows the structure of modified QRFC proposed OTA. The differential driver transistor pair is split in four times to recycle the source current more times. Since RFC, DRFC and proposed QRFC are modified from main conventional folded cascode OTA as shown in Figure-1 by properly adjustment of current mirror ratio which exact comparison between these four types of OTA in terms of transconductance, slew rate, bandwidth.

As mentioned before, the transconductance of FC is Gm and Transconductance of RFC is (K+1) gm1 which is cannot exceed more than three times because of it's symmetric slew rate. The proposed structure given by Zushu Yan is DRFC shown in whose transconductance is written as,

$$Gm_{DRFC} = \left[1 + \frac{2[K(2M+1)-(M+N+1)]}{K+M+N+1}\right] Gm \quad (3)$$

In this DRFC the current source provides much freedom for recycle the current through it by adjusting the sizing value K, M, N of the bottom transistor which help to increase the effective transconductance of DRFC. Also, in QRFC these current sources again reuse to enhance performance by adjusting K, M, N, P value of transistor which result the transconductance improved in QRFC is more than FC/RFC/DRFC. The gain and GBW (gain

bandwidth) product also highest as compare to other. Similarly for QRFC these current source reuse four times so it's called quadruple recycle OTA.

Adjusting value of K, M, N, P design the QRFC which help to enhance the overall performance of OTA compare with others. The following equations shows the mathematical analysis of all OTAs. The transistor M11 and M12 in RFC which shown in Figure-2 which split into M11, M12, M13, M14, M15, M16, M17, M18, M19 and M20 in which M19, M3d2, M20, M4d2 provide high impedance to the path. The small current flow through current mirror node which is larger than the previous method. The small signal current strengthened by the ratio of K, M, N, P. In this most of the transistor are working in sub threshold region which help to ignore the variation in the small signal input.

3.2 Equations and mathematical analysis

For output resistance of OTA is given by,

$$R_{OFC} = g_{m6}\, r_{d6}(r_{ds2}||r_{ds4})\, g_{m8} r_{ds8} r_{ds10} \quad (4)$$

$$R_{ORFC} = g_{m6}\, r_{d6}\left(\frac{K+1}{K-1}\, r_{ds2}||r_{ds4}\frac{K+1}{K}\right)||\, g_{m8} r_{ds8} r_{ds10} \quad (5)$$

$$R_{OIRFC} = g_{m6}\, r_{d6}\left(\frac{K+M+1}{K-M-1}\, r_{ds2}||r_{ds4}\frac{K+M+1}{K}\right)||\, g_{m8} r_{ds8} r_{ds10} \quad (6)$$

$$R_{ODRFC} = g_{m6}\, r_{d6}\left(\frac{K+M+N+1}{K-M-N-1}\, r_{ds2}||r_{ds4}\frac{K+M+N+1}{K}\right)||\, g_{m8} r_{ds8} r_{ds10} \quad (7)$$

$$R_{OQRFC} = g_{m6} r_{d6}\left(\frac{K+M+N+P+1}{K-M-N-P-1}\, r_{ds2}||r_{ds4}\frac{K+M+N+P+1}{K}\right)||\, g_{m8} r_{ds8} r_{ds10} \quad (8)$$

The equation 8 shows the mathematical value or theoretical analysis of QRFC compare with others the output resistance increase which effect in increases the overall gain of the circuit.

We know that,

$$Av = Gm * Rout \quad (9)$$

The equation 6 and 7 shows the proposed work done in literature survey. According to this they got this equation and the enhancement in gain, but in QRFC we modified the gain stage and try to enhance the gain more than other. For the value of K, M, N, P listed above we take some assumption for this gm6 rd6 = gm8 rd8, rds10= rds2 || rds4. Due to this the output resistance higher than other. Which effect on reduced the bias current from the driver transistor and bottom most transistor which help to enhance the performance of the QRFC circuit. Due to change in the current shunt circuit which effect on the overall circuit performance.

We reuse the current source more times which effect on the overall Gm (Transconductance) of the circuit, which also modified because of the reusing and splitting the driver transistors. The effective transconductance is given by,

$$G_{mQRFC} = \left[1 + \frac{2[K(M(2N+1)-(M+N+P+1))]}{K+M+N+P+1}\right] Gm \quad (10)$$

The above equation shows value of Gm is changes according with the current source reusing. Which will increase the overall gain of the system. While using the current shunt sources more times the output resistance increase in large extent which will help to increase the overall GBW product. Due to large GBW product which effect on the settling time, but QRFC settling time is still good compare with other structure.

The proposed method QRFC has very high gain and gain bandwidth frequency but it also shows the better linearity in closed loop and better input referred noise and Figure of merit (FOM) with highly stable pole zero location, because of high gain and GBW we have to compromise with the phase margin. Due to this, phase margin reduction is more as compare to FC, RFC and others but the achievable phase margin is still sufficient for well performance of transient response with lower settling time. Certainly phase margin of conventional FC is very high due this we get slow step response, but we more focus on gain and GBW. The proposed structure of QRFC is shown below:

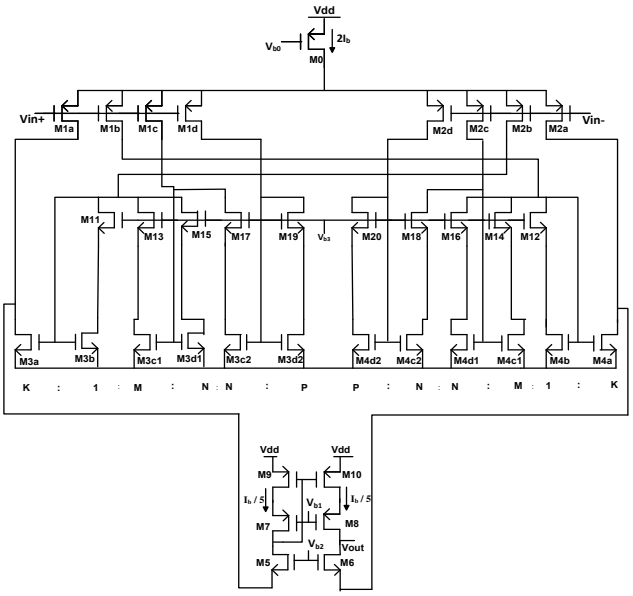

Figure-3. Proposed QRFC OTA.

The above figure shows the actual schematic of QRFC on virtuoso. The output stage is similar to all other OTA's.

For slew rate of OTA is denoted as SR_{QRFC} and given by following relation,

$$SR_{QRFC} = I_{BIAS}(I_{10}) / C_L \quad (11)$$

The Figure-3 shows the proposed structure of QRFC. As compare with the FC and RFC the current

source recycle many times to enhance the performance as the FC and RFC the current equally pass through the input and output stage but here the splitting the transistor four times which draws different current, according to bottom most transistor. The bias current reduces from the input branch and the bottom transistor work in triode region to limit the current which help to improve the overall output resistance. The transistor M8 draws current less than Itail /2 which effect on slew rate.

Some of the transistor is working in sub threshold region which has negligible effect of small signal variation. The current variation from the driver transistor is depending upon their ratio which differently draws current. Transistor M3a and M4a draw more current which add small signal as well as current coming from source side call I_{bias} which add in Node A and Node B. Due to this transistor M3a and M4a draws more current. Which result the overall output resistance increases.

4. SIMULATION AND RESULTS

For fair comparison between all the OTA's like (FC, RFC, DRFC, QRFC) they are design by using the value of K, M, N, P with take care of power and area budgets. We perform all the test on QRFC on virtuoso using 0.18nm technology. According to test performance it shows the following result. By performing all tests it shows the QRFC structure which enhances the gain and GBW with greater stability.

Figure-4 shows the closed loop test for all OTA's which shows the system performance. All the three amplifier used as unity gain amplifier and perform test. Figure-5 where $C_1 = 1pf$, $C_2 = 5\text{-}8pf$, $R_1 = 600K\Omega$.

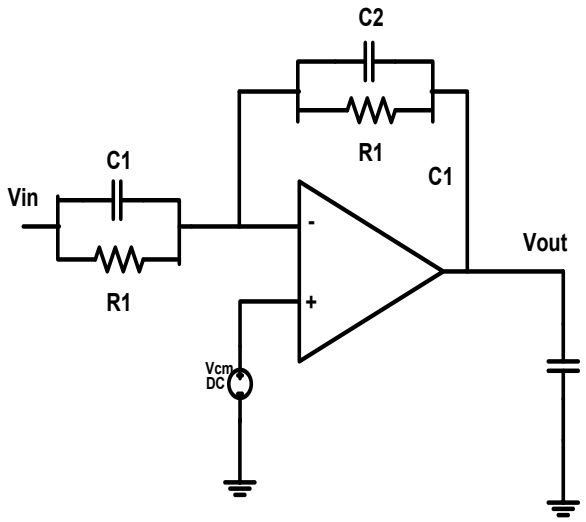

Figure-4. Unity gain amplifier.

Figure-5 shows the gain plot obtain in dB which shows the exact gain of the QRFC. A DC gain enhancement will be obtain.

By using this Quadruple recycle folded cascode OTA. Also the output resistance enhance because of increase in the output impedance of M3a and M1a which help to increase this this overall transconductance of QRFC stage. Due to this there is increase in gain of amplifier with larger extent.

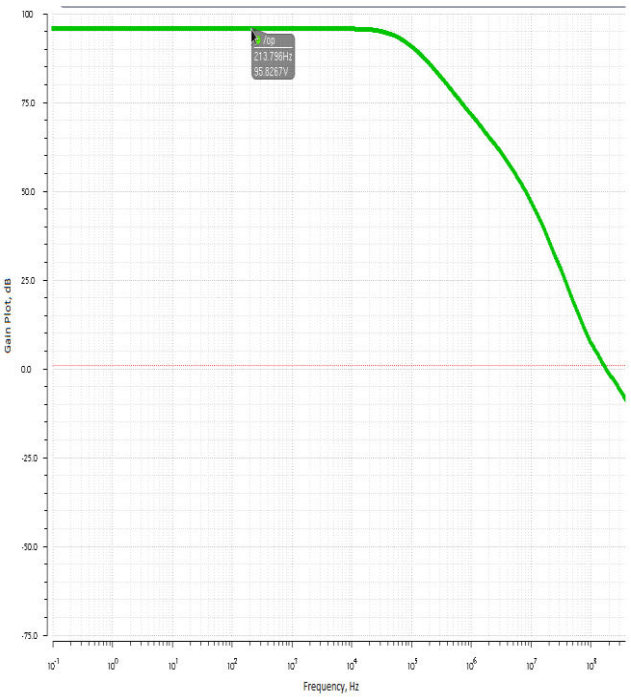

Figure-5. Gain plot in dB of QRFC.

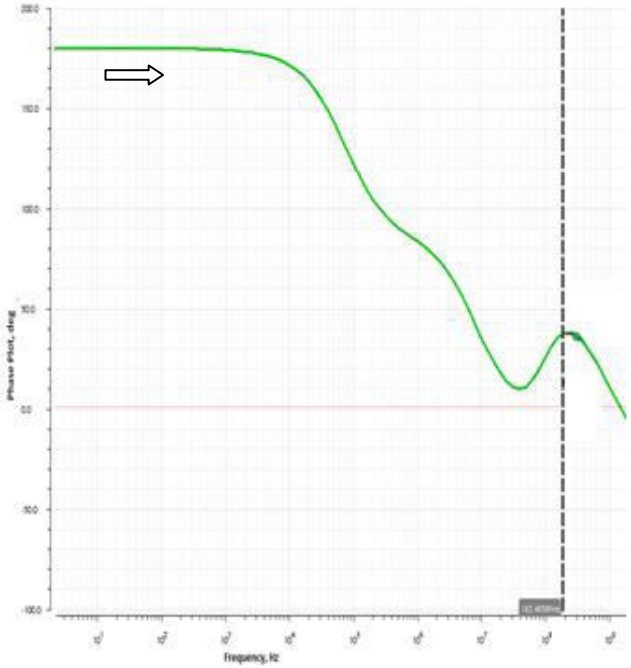

Figure-6. Phase plot of QRFC.

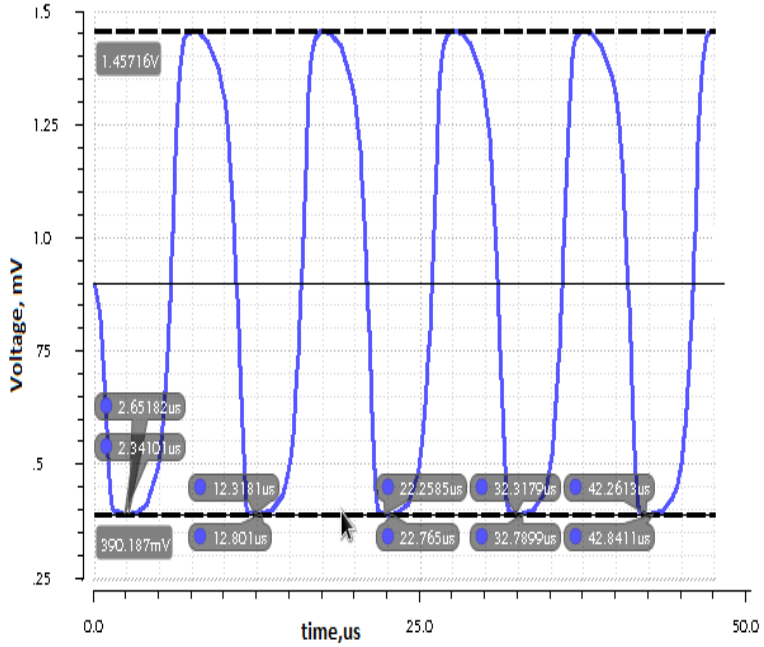

Figure-7. Transient response of QRFC.

Figure-6 shows the phase plot which nearly equal to 40 deg. It decrease due to high gain. Which shown in figure 5 the maximum gain obtain due to this proposed method is 95dB which better as we compare with other OTA's, but as we go for increasing the gain of an amplifier as high as much possible we have to compromise with phase margin. For operation amplifier this much phase margin is sufficient for working.

Table-1. Performance summary of FC, RFC, DRFC, QRFC.

Parameter	Conventional Folded Cascode (Xiao Zhao method)	Recycle Folded Cascode (Xiao Zhao method)	Double Recycle Folded Cascode (Zushu Yan) Method	Proposed method Quadruple Recycle Folded Cascode
Supply Voltage (V)	1.2	1.2	1	1.8
Bias Current (µA)	110	110	800	200
Capacitive Load (pF)	8	8	10	0.5
DC Gain (dB)	71.2	79.5	54.5	95.82
GBW (MHz)	12.5	25.4	203.2	182.81
Phase Margin (deg)	79.3	76.5	66.2	40.08
Average Slew rate (V/ µs)	5.8	13.4	84.1	78.4

Figure-7 shows the transient response of the QRFC from this we know the voltage swing obtain at the output is very high nearly equal to 1V which good for high swing application. Most of the application like bio-medical used in medical field application, industrial instrumentation application which require large gain with high gain bandwidth frequency for this application QRFC play major role. From the above table we compare with other OTA's QRFC is high gain OTA with good GBW frequency and voltage swing. This enhancement is obtain due to recycle the current shunt source more time.

5. CONCLUSIONS

A QRFC operational transconductance amplifier shows greater significant performance over the all existing OTA's FC, RFC, DRFC, etc. It enhance the overall gain up to 95dB which is quite large as compare to others. By recycling the current source of the input stages of DRFC more times we enhance the effective gain and GBW of OTA with less power budget. Due to this there is reduction in phase margin but is still enough for operating.

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