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ENERGY BALANCE CASCADED MULTILEVEL INVERTER FOR PHOTOVOLTAIC APPLICATION

A. Santhi Mary Antony, D. Ramya and D. Godwin Immanuel
Department of Electrical and Electronics, Sathyabama University, Chennai, India
E-Mail: msanthimary@gmail.com

ABSTRACT

Energy balance cascaded multilevel inverter for photovoltaic application. It is used for less no of power switches, losses, installation area, voltage stress and converter cost. It is also used for solar energy that is connected to the micro grid system. It reduces the transformerless operation and improves the power quality. Ability to operate in both symmetrical and asymmetrical mode is analyzed. The results are done with cascaded H bridge (CHB) and flying capacitor (FC) multilevel inverters. The simulation is done with Matlab Simulink.

Keywords: multilevel inverter, cascaded H Bridge, least power point tracking, buck boost converter.

1. INTRODUCTION

In the current scenario, due to the environmental issues and limited fossil resources, the demand for renewable energy is increasing. To meet this growing demand, Photovoltaic (PV), Fuel Cell and Wind Turbine (WT) systems have become the important integral part of grid connected renewable energy systems (RES). Harnessing of electrical energy from the PV systems contributes to power generation. This contribution made it wide spread in the current global climatic conditions. Long lasting, high efficiency and pollution free power generation are the advantages of PV systems. The low output voltage PV arrays are connected in series to accomplish high voltage DC, and DC to AC inverter is used to interface with the grid. This approach needs high voltage rated devices for the inverter. To overcome this issue, the step-up transformer is necessary. This system enables to use the low voltage rated devices for inverter and then boosting the voltage by transformer. This may lead to increase in losses and cost of the system. Using transformerless concepts are beneficial in reducing cost, size, weight and complexity of inverter besides enhancing the efficiency. A multilevel converter is the one which uses properly connected power semiconductor devices to several lower DC voltage sources to synthesize a near sinusoidal staircase voltage waveform. The small output voltage step results in high quality output voltage, reduction of voltage stresses on power switching devices, lower switching losses and higher efficiency. The era of multilevel inverters (MLIs) started with diode clamped multilevel inverter, also known as neutral point clamped (NPC), in 1981 [1], then capacitor-clamped multilevel inverter or flying capacitor in 1992 [2] and the cascade H-bridge (CHB) multilevel inverter in 1995. The different topology presented in the literature as multilevel converters [3-4] possesses the number of characteristics, giving their clear advantages over bi-level converters. These advantages promote the MLIs as the suitable choice for grid connected renewable energy systems in both the adoption of MLIs results in reduction of cost and size of filtering requirements in transformer less PV system depicted in Figure-1 [5-7]. Various MLI topologies for renewable energy applications are listed in [8-10]. The complexity and requirement of high number of power switches are the main disadvantages associated with the multilevel configurations. The reduction of semiconductor switches in the MLI topologies has lead to enormous significance in academia and the industry. The reduction in switches further reduces the number of components including gate drives. Eventually the reduction in switch count improves the efficiency and minimizes the control complexity.

2. CIRCUIT DIAGRAM AND SYSTEM MODULE DESCRIPTION

To discuss the impact of removing a PV panel for the purpose of maintenance or failure due to faults [4-9] on the behavior of overall inverter, the PV RES connected to proposed 9-level HCM MLI for single phase. In each phase of proposed inverter connected RES three PV panels viz., 1, 2 and 3 are employed. The sensors are provided at the buck boost converter end to detect the voltage and given to inverter control block. The switching logic is updated in the inverter control block to maintain the three phase balanced output voltages under faulty conditions. Three possible failures or removal are considered in this section and simulation results are presented.

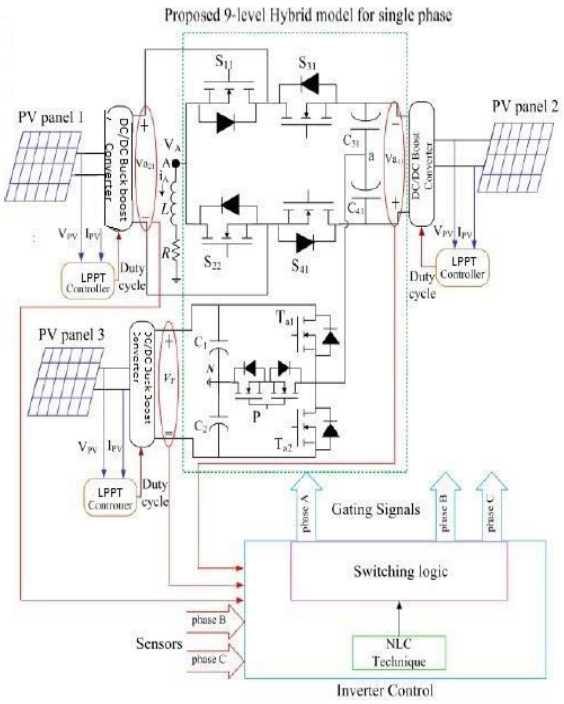

Figure-1.

When PV panel 1 is failed to pump the voltage V_{a11} due to the fault the phase _*A*' voltage gets distorted and level gets reduced resulting in unbalance in the three phase system. These dynamics are analyzed with the help of simulation studies presented in the Figure-2 (a)-(c). As shown in Figure-2 (a) the system enters into steady state after *t*=0.35 sec and producing balanced three phase voltages. When a fault is introduced by setting the PV panel 1 irradiance to zero at t=0.5 sec, the corresponding panel 1 voltage V_{a11} gradually reduced to zero at *t*=1.2 sec as seen from the Figure-2 (b). The phase _*A*' voltage gets distorted resulting in a reduced fundamental voltage of 35.51V unlike the fundamental at normal operation of 83.87V and increased %THD from 8.40% to 41.74%.

To balance the system, the switching logic in Table-3 is updated according to the Table XI at *t*=1.4 sec. The system is well balanced and producing 5-levels in all three phases with the improvement of %THD to 17.5% and fundamental is increased to 46.93V. During these changes, the balancing of capacitors is unfazed as shown.

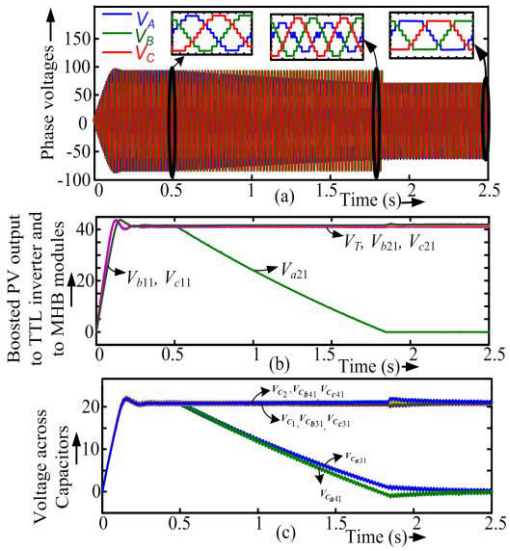

Fig. 1.1 Dynamics of PV panel 1 failure for symmetrical 9-level HCM MLI operation

Figure-2(a).

3. BLOCK DIAGRAM

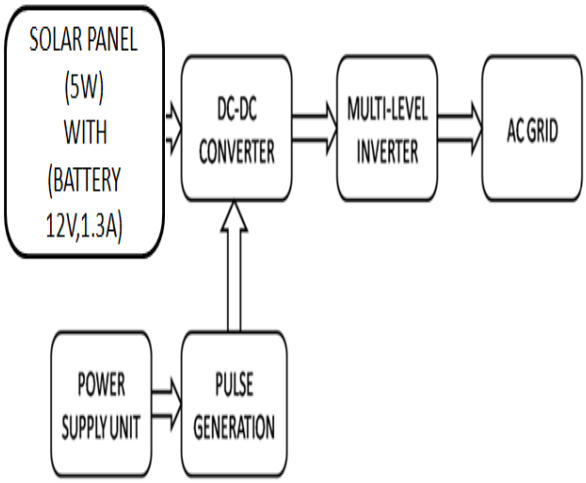

Figure-2(b).

4. MODES OF OPERATION

To discuss the impact of removing a PV panel for the purpose of maintenance or failure due to faults [4-9] on the behavior of overall inverter, the PV RES connected to proposed 9-level HCM MLI for single phase is shown in Figure-3. In each phase of proposed inverter connected RES three PV panels viz., 1, 2 and 3 are employed. The sensors are provided at the boost converter end to detect the voltage and given to inverter control block. The switching logic is updated in the inverter control block to maintain the three phase balanced output voltages under faulty conditions. Three possible failures or removal are considered in this section and simulation results are presented.

When PV panel 1 is failed to pump the voltage V_{a11} due to the fault the phase _*A*' voltage gets distorted

and level gets reduced resulting in unbalance in the three phase system. These dynamics are analyzed with the help of simulation studies presented in the Figure-3 (a)-(c). As shown in Figure-3 (a) the system enters into steady state after *t*=0.35 sec and producing balanced three phase voltages. When a fault is introduced by setting the PV panel 1 irradiance to zero at t=0.5 sec, the corresponding panel 1 voltage V_{a11} gradually reduced to zero at *t*=1.2 sec as seen from the Figure-3(b). The phase _*A*' voltage gets distorted resulting in a reduced fundamental voltage of 35.51V unlike the fundamental at normal operation of 83.87V and increased %THD from 8.40% to 41.74%. To balance the system, the switching logic in Table-1 is updated according to the Table-2 at *t*=1.4 sec. The system is well balanced and producing 5-levels in all three phases with the improvement of %THD to 17.5% and fundamental is increased to 46.93V. During these changes, the balancing of capacitors is unfazed.

Table-1.

BALANCED SYSTEM

SYMMETRICAL 9-LEVEL MLI.

L.NO.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	T_{a1}	T_{a2}	P	V_A
1	1	0	0	1	1	0	0	+2V
2	1	0	0	1	0	0	1	+3V/2
3	1	0	0	1	0	1	0	+V
4	0	1	0	1	0	0	1	+V/2
5	1	0	1	0	1	0	0	0
6	1	0	1	0	0	0	1	-V/2
7	0	1	1	0	1	0	0	-V
8	0	1	1	0	0	0	1	-3V/2
9	0	1	1	0	0	1	0	-2V

5. LPPT (least power point tracking)

It is used for faster than the MPPT in power tra dynamics for the failure of PV panel 2 at *t*=0.5 sec are shown in Figure-2 (a)-(b). Since the capacitors are connected across the PV panel 2, V_{a21} takes more time to settle down to zero at *t*=1.78 sec as depicted in Figure-2(b) and correspondingly the capacitor voltages settle down to zero, while the other capacitor voltages are balanced as shown in Figure-2 (b). The unbalance occurs in system due to Phase _*A*'and it is rectified by updating the switching states as per the Table-1. The balance is achieved by synthesizing 7- level in other phases _*B*'and _*C*'with updating entries of Table-2. The Phase _*A*' is recovered from distortion as shown in Figure-2(a) and improves the fundamental voltage from 58.04V to 71.43V and %THD from 24.71% to 14.14%.

Table-2. Unbalanced system.

S.NO.	S_{a11}	S_{a21}	S_{a31}	S_{a41}	T_{a1}	T_{a2}	P	V_A
1	0	1	0	1	1	0	0	+V
2	0	1	0	1	1	0	0	+V
3	0	1	0	1	0	0	1	+V/2
4	0	1	0	1	0	0	1	+V/2
5	1	0	1	0	1	0	0	0
6	1	0	1	0	0	0	1	-V/2
7	1	0	1	0	0	0	1	-V/2
8	1	0	1	0	0	1	0	-V
9	1	0	1	0	0	1	0	-V

5. LPPT (least power point tracking)

It is used for faster than the MPPT in power tracking. The optimal sting current for LPPT changes based on the PV modules operating points which will vary during MPPT. In contrast, each PV modules MPPT is not affected by sting current variation. The LPPT algorithm aims to dynamically track the unique LPPT according to the instantaneous PV voltage and current in the system.

The dynamic response of LPPT should be designed such that one of the algorithms is significantly slower relative to the other algorithm. We can use LPPT in low power appliances for examples kitchen appliances Speakers, LED light etc.

6. BUCK-BOOST CONVERTER

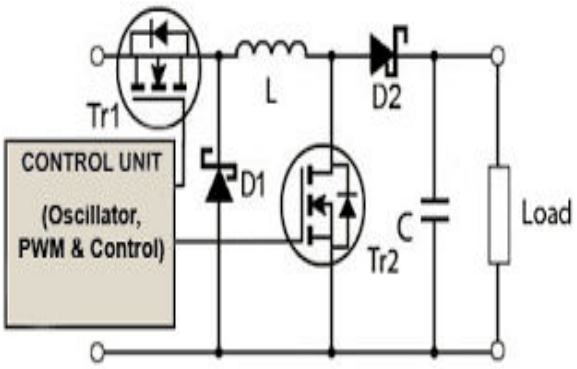

Figure-3(a).

The buck–boost converter is a type of DC-to-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. It is equivalent to a flyback converter using a single inductor instead of a transformer. A 2-switch buck-

boost converter can be built with two diodes, but upgrading the diodes to FET transistor switches doesn't cost much extra while due to lower voltage drop the efficiency improves. The operation of the buck-boost is best understood in terms of the inductor's "reluctance" to allow rapid change in current. From the initial state in which nothing is charged and the switch is open, the current through the inductor is zero. When the switch is first closed, the blocking diode prevents current from flowing into the right hand side of the circuit, so it must all flow through the inductor. However, since the inductor doesn't like rapid current change, it will initially keep the current low by dropping most of the voltage provided by the source. Over time, the inductor will allow the current to slowly increase by decreasing its voltage drop. Also during this time, the inductor will store energy in the form of a magnetic field.

7. SOFTWARE REQUIREMENTS

- MATLAB 7.14
- MPLAB

8. HARDWARE REQUIREMENTS

- Power MOSFET: IRF840
- Driver IC : IR2112
- Capacitor : 470uF (25V); 1000uF
- Controller :PIC16F877A
- Regulators :LM7805; LM7812
- Diodes : 1N4000; 1N5408
- Inductors : 100uH; 200uH; 1mH

9. EXPERIMENTAL RESULTS

The experimental circuit of the proposed converter is developed. The experimental result of input voltage, input current and output voltage is shown in Figure.

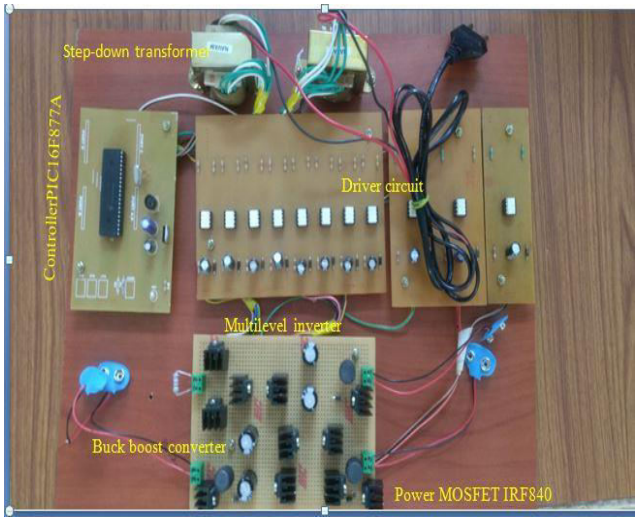

Figure-3(b)

CONCLUSIONS

The experimental results show the ability of a proposed inverter to generate all the levels in both symmetrical and asymmetrical modes while maintaining the natural balancing of all the capacitors voltages in each module. Due to its modular structure, it can be easily interfaced with PV connected micro grid.

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