VOL. 13, NO. 3, FEBRUARY 2018 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

PERFORMANCE EVALUATION OF REVERSIBLE VEDIC MULTIPLIER

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ABSTRACT

Multipliers are one of the building blocks of several computational units. The speed of the computational units is determined by the speed of the multipliers. To increase the speed of computational units, faster multipliers should be utilized. The Vedic multiplier is one such solution, which is capable of performing the quicker multiplications. In Vedic mathematics Urdhva Tiryakbhayam sutra discards the non essential steps in multiplication process which in turn increases the speed of a multiplier. In this work, the performance of the Urdhva Tiryakbhayam Vedic multiplier is improved by reducing the Number of gates, Garbage outputs, Quantum cost and TRLIC.

Keywords: multipliers, Urdhva Tiryakbhayam.

1. INTRODUCTION

Vedic mathematics is rediscovered by the Swami Sri Bharati Krsna Tirthaji in between 1911 and 1918. He implemented sixteen sutras (formulae) in his research. Each individual formula has its own importance and is capable of solving a mathematical problem in different branches of mathematics such as algebra, calculus, geometry, trigonometry etc [1].

In Vedic mathematics, the Urdhva Tiryakbhayam sutra is the one of the multiplication algorithm. The Sanskrit words Urdhva and Tiryakbhayam means vertically and crosswise respectively. The Urdhva Tiryakbhayam algorithm is suitable for all kinds of multiplication such as Binary, Decimal and Hexadecimal etc. The concept behind this sutra is that partial product generation can be done and then the concurrent (parallel addition) summation of these partial products is performed which leads to the reduction in the computational time.

Multiplication is a one of the main arithmetic operation that is frequently used in several applications like ALU, MAC and DSP etc. In DSP units, to perform important operations such as Filtering, FFT, convolution, correlation and wavelet compression etc the multipliers are essential [2].

In the past few decades, reversible logic has become one of the prominent research area and having its applications in the emerging technologies such as Optical computing, DNA computing, Quantum computing etc [3].

The organization of the paper begins with back ground of reversible logic in section 2, section 3: previous work of reversible Urdhva Tiryakbhayam Multiplier. Section 4: proposed work which explains the implementation of Reversible Vedic multiplier based on Urdhva Tiryakbhayam sutra. Comparison of the implemented design with the existing Reversible Urdhva Tiryakbhayam multiplier in section 5 followed by conclusion in section 6.

2. BACKGROUND OF REVERSIBLE LOGIC

Landauer has demonstrated that for every bit of information lost during conventional logic computation produces KTln2 joules of heat energy Where K = Boltzmann's constant, T = Absolute Temperature [4]. Bennett proved that energy loss can be avoided only if the circuits are implemented with reversible logic gates [5].

A Reversible logic gate is an m-input m-output (denoted by m x m) digital logic circuit that generate a unique output vector from each input vector and vice versa. The few design parameters used to evaluate the performance of the reversible circuit are Gate count, Constant inputs, Garbage outputs and Quantum cost etc. Gate count is defined as the numbers of reversible logic gates essential to build the reversible circuit are known as Gate count. Constant inputs are the inputs of a reversible logic gate that is maintained with a constant value ('0' or '1'). The outputs of the reversible gate that is not needed for additional computations is called Garbage outputs. The Quantum cost is computed by knowing the number of 1x1 and 2x2 (primitive) gates [6]. TRLIC is defined as the summation of the number of reversible gates, quantum cost, constant inputs and garbage outputs [7]. It is given as

TRLIC = $\sum$ (NG, QC, CI, GO).

2.1 Reversible logic gates

The following are the reversible logic gates which are used in this work.

CNOT Gate: It is a 2 inputs (A, B) and 2 outputs (W, X) gate which is shown in Figure-1. Its quantum cost is one [8].

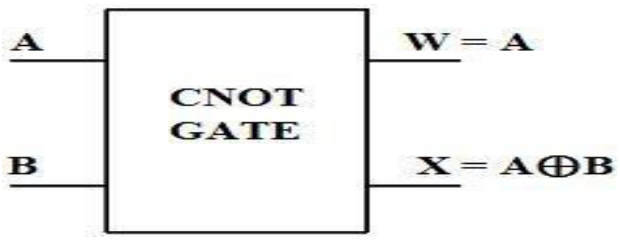

Figure-1. CNOT GATE.

BVF Gate: It is a 4 inputs (A, B, C, D) and 4 outputs (W, X, Y, Z) gate which is shown in Figure-2. Its quantum cost is two [9].

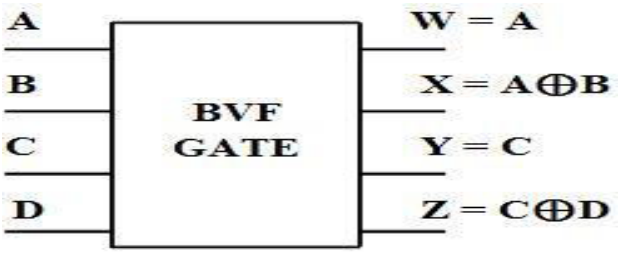

Figure-2. BVF GATE.

PERES Gate: It is a 3 inputs (A, B, C) and 3 outputs (W, X, Y) gate which is shown in Figure-3. Its quantum cost is four [10].

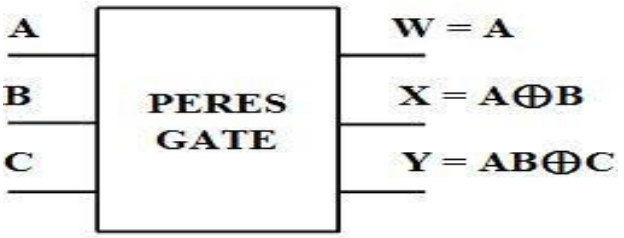

Figure-3. PERES GATE

RMUX 1 Gate: It is a 3 inputs (A, B, C) and 3 outputs (W, X, Y) gate which is shown in Figure-4. Its quantum cost of four [11].

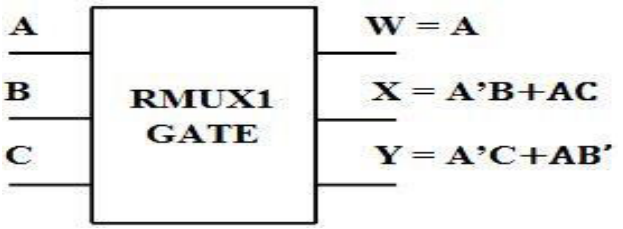

Figure-4. RMUX1 GATE.

BME Gate: It is a 4 inputs (A, B, C, D) and 4 outputs (W, X, Y, Z) which is shown in Figure-5. Its quantum cost is five [12, 13].

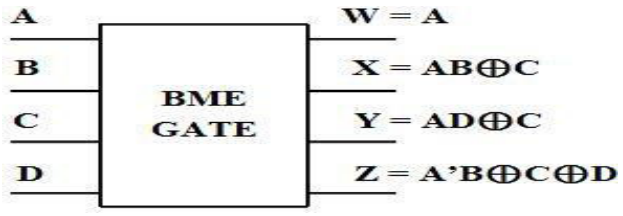

Figure-5. BME GATE.

HNG: It is a 4 inputs (A, B, C, D) and 4 outputs (W, X, Y, Z) gate which is shown in Figure-6. Its quantum cost is six [14].

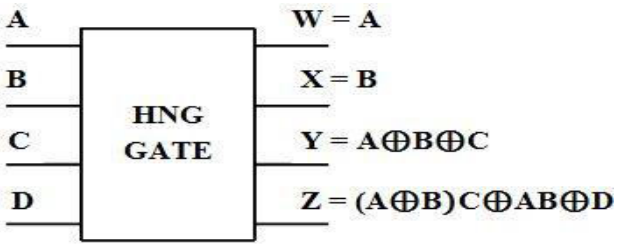

Figure-6. HNG GATE.

3. RELATED WORK

In existing design [7] the reversible 2x2 and 4x4 Urdhva Tiryakbhayam Multiplier (UT Multiplier) was proposed. The existing reversible 2x2 UT Multiplier is implemented with one CNOT Gate and five Peres Gates. In this design a total number of reversible gates are six, the quantum cost of the design is twenty one, it generates nine garbage outputs and constant inputs are four. The drawback of this design is it does not take the Fanout into consideration.

The existing reversible 4x4 UT Multiplier is implemented with four reversible 2x2 UT Multiplier, two four bit and one five bit reversible ripple carry adders. The drawback of this design is it suffers from an improper arrangement of adders.

4. PROPOSED WORK

4.1 Reversible 2x2 Urdhav Tiryakbhayam multiplier

The proposed design shown in the Figure-7 makes use of totally five reversible logic gates. This design requires five constant inputs and produces five garbage outputs. The quantum cost of the design is seventeen [16]. The Reversible 2x2 multiplier using Urdhva Tiryakbhayam algorithm is implemented based on following four equations [7].

$q_0 = a_0.b_0$
$q_1 = (a_1.b_0) \oplus (a_0.b_1)$
$q_2 = (a_0.a_1.b_0.b_1) \oplus (a_1.b_1)$
$q_3 = (a_0.a_1.b_0.b_1)$

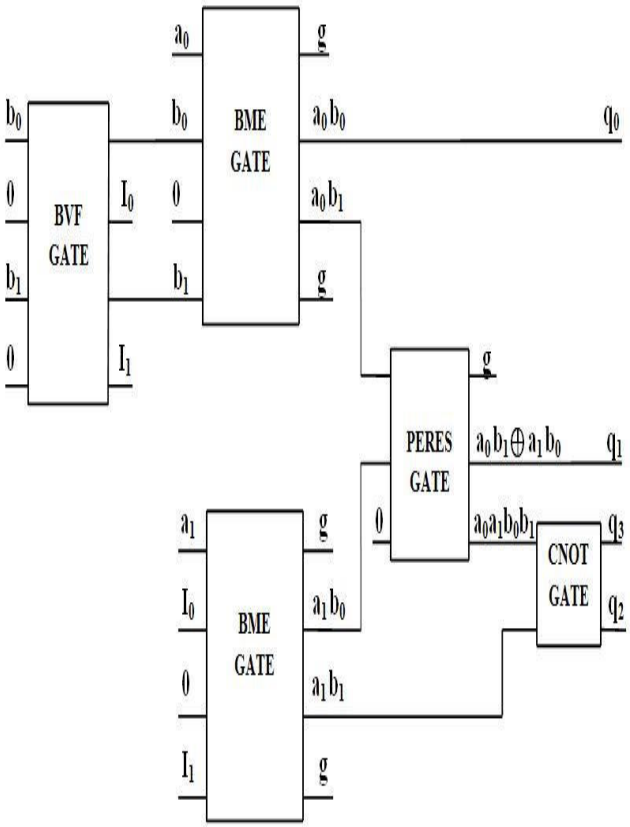

Figure-7. Proposed reversible 2x2 Urdhav Tiryakbhayam multiplier.

4.2 Reversible 4x4 Urdhav Tiryakbhayam multiplier

In [15] the architecture of the conventional (irreversible logic) Urdhav Tiryakbhayam multiplier was modified by replacing the irreversible circuits with the reversible circuits.

Figure-8 shows the block diagram of Reversible 4X4 Urdhva Tiryakbhayam (UT) multiplier which emanates from the reversible 2x2 UT multiplier. In this, the outputs of first 2x2 reversible UT multiplier whose inputs are b[1:0], a[1:0] forms the LSB's of the final result (y[1:0]). The results of second and third 2x2 reversible UT multipliers are added using the upper 4-bit reversible ripple carry adder. The sum outputs (qa[3:0]) except carry (C1) of upper 4-bit reversible ripple carry adder, the remaining bits of first 2x2 reversible UT multiplier and LSB bits of fourth 2x2 reversible UT multiplier are applied as inputs to the lower 4-bit reversible ripple carry adder. The sum outputs of lower adder serve as the second, third, fourth and fifth bits of the final result (y[5:2]). The carry bits C1 and C2 of the 4-bit reversible ripple carry adders are applied to the reversible OR gate. The remaining bits of the final result (y[7:6]) is obtained by using two reversible half adders.

In the implementation of reversible ripple carry adders HNG gate is used as a reversible full adder. For 4-bit reversible ripple carry adder requires 4 HNG gates as shown in Figure-9 and Peres gate is used as a reversible half adder when the third input of the gate is zero as shown in Figure-10 and RMUX1 gate can be used as reversible OR gate when the second input of the gate is zero as shown in Figure-11.

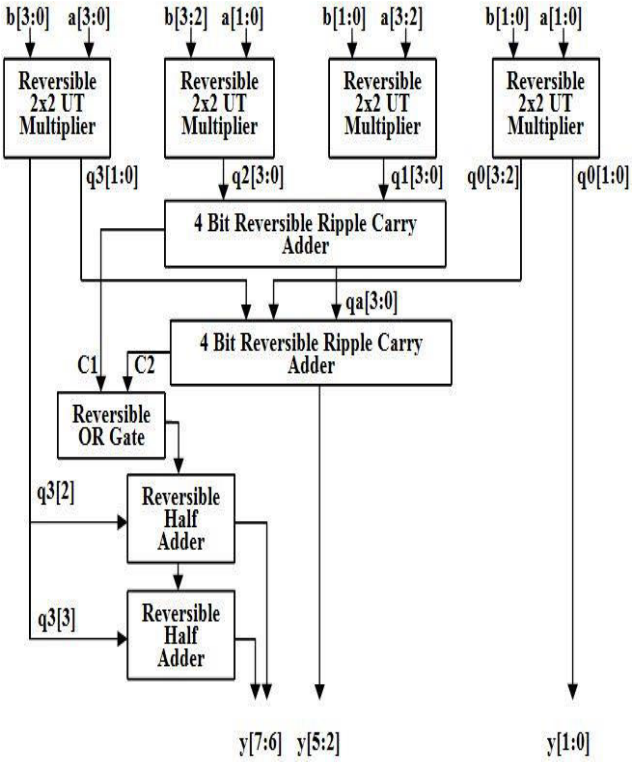

Figure-8. Block diagram of reversible 4x4 UT multiplier.

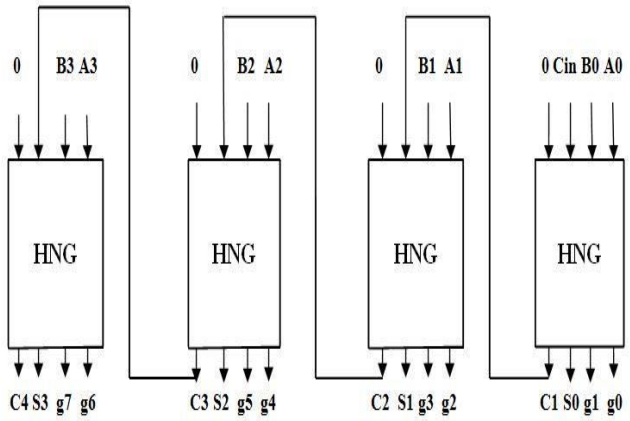

Figure-9. 4-Bit Reversible Ripple Carry Adder.

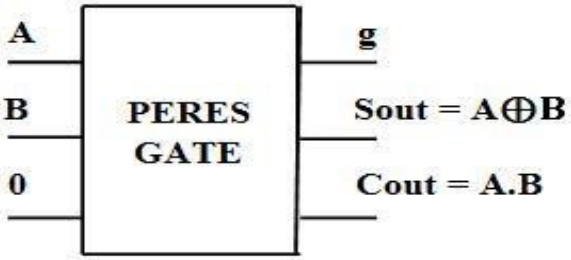

Figure-10. Reversible half adder.

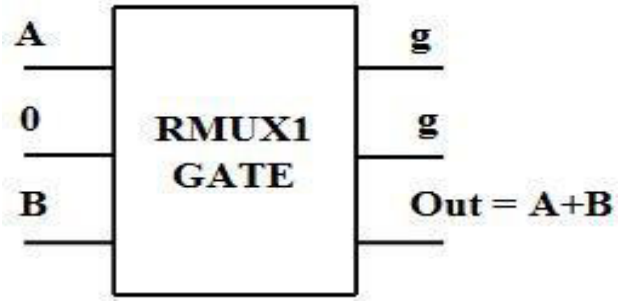

Figure-11. Reversible OR Gate.

4.3 Reversible 8X8 Urdhva Tiryakbhayam multiplier

For the implementation of the Reversible 8X8 Urdhav Tiryakbhayam multiplier which is shown in Figure-12 needs four Reversible 4x4 UT multipliers. The result of first 4x4 reversible UT multiplier whose inputs are b[3:0], a[3:0] forms the LSB's of the final result (y[3:0]). The results of second and third 4x4 reversible UT multipliers q1[7:0] and q2[7:0] are added using the upper 8-bit reversible ripple carry adder. The sum outputs (qa[7:0]) except carry (C1) of upper 8-bit reversible ripple carry adder, the remaining bits of first 4x4 reversible UT multiplier (q0[7:4]) and LSB bits of fourth 4x4 reversible UT multiplier (q3[3:0]) are applied as a inputs to the lower 8-bit reversible ripple carry adder. The sum outputs of this adder serve as fourth to eleventh bits of the final result (y[11:4]). The carry bits C1 and C2 of the reversible ripple carry adders are applied to the RMUX1 which act as a reversible OR gate. The remaining bits of the final result (y[15:12]) is produced by using four Peres gates as reversible half adders. In the construction of 8-bit reversible ripple carry adders requires 8 HNG gates as shown in Figure-13.

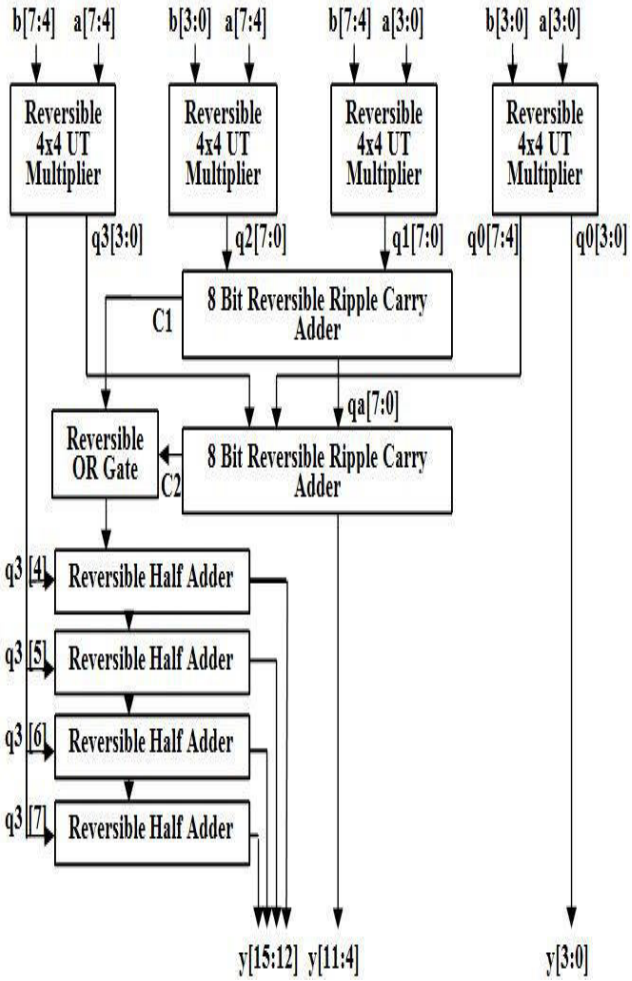

Figure-12. Block diagram of 8x8 UT multiplier.

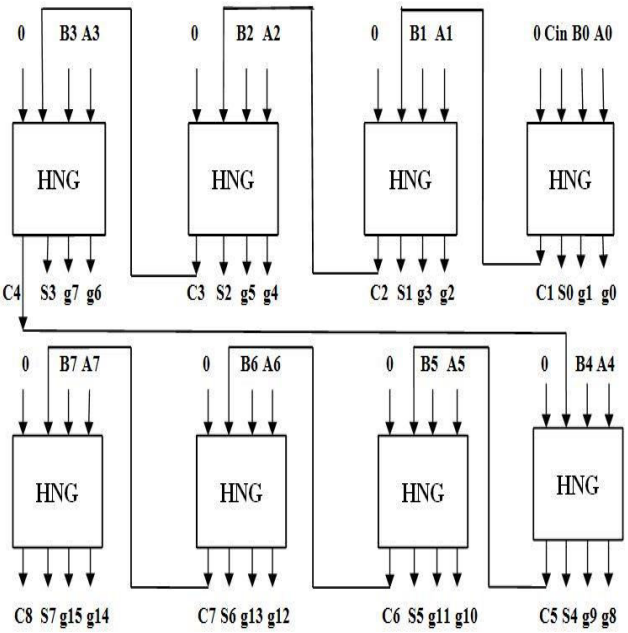

Figure-13. 8-Bit reversible ripple carry adder.

4.4 Reversible 16x16urdhva Tiryakbhayam multiplier

The reversible 16X16 Urdhva Tiryakbhayam multiplier requires four reversible 8x8 UT multipliers which is shown in Figure-14. The result of first 8x8 reversible UT multiplier whose inputs are b[7:0], a[7:0] forms the LSB's of the final result (y[7:0]). The results of second and third 8x8 reversible UT multipliers q1[15:0] and q2[15:0] are added using the upper 16 bit reversible ripple carry adder. The sum outputs (qa[15:0]) except carry (C1) of upper 16-bit reversible ripple carry adder, the remaining bits of first 8x8 reversible UT multiplier (q0[15:8]) and LSB bits of fourth 8x8 reversible UT multiplier (q3[7:0]) are applied as a inputs to the lower 16-bit reversible ripple carry adder. The sum outputs of this adder serve as eighth to twenty third bits of the final result (y[23:8]). The carry bits C1 and C2 of the reversible ripple carry adders are applied to the reversible OR gate. The remaining bits of the final result (y[31:24]) is generated by using eight reversible half adders. The 16-bit Reversible ripple carry adder is designed using 16 HNG gates as shown in Figure-15.

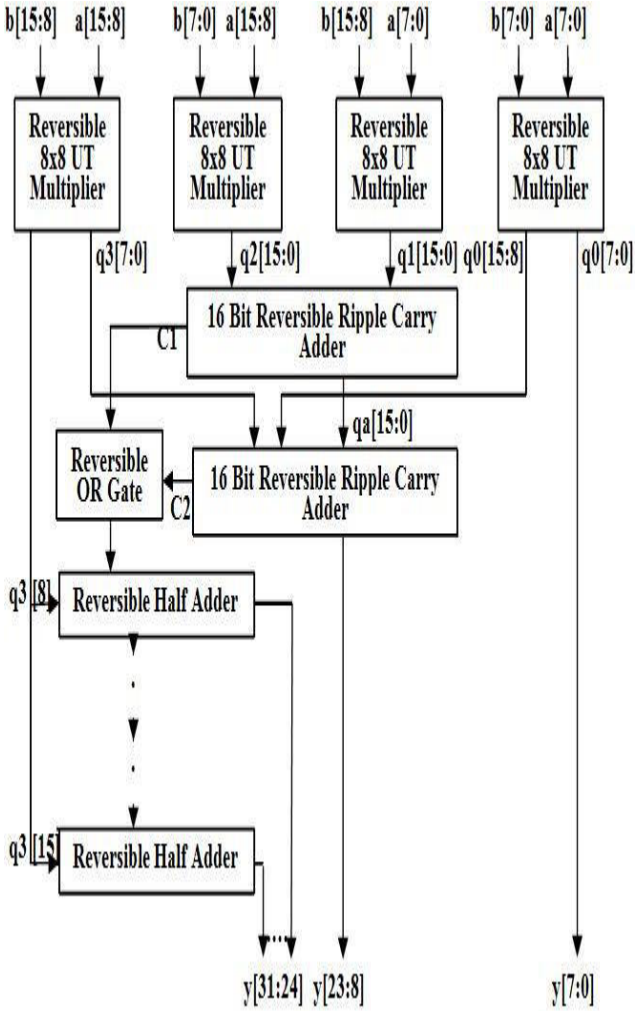

Figure-14. Block diagram of 16x16 UT multiplier.

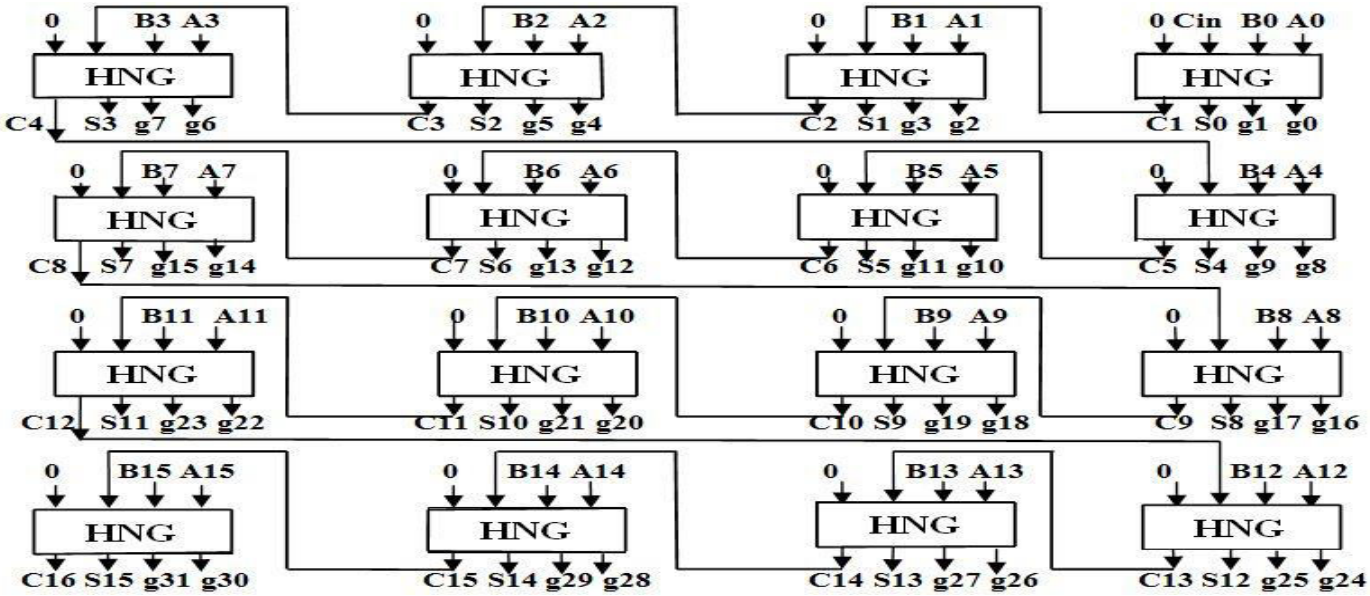

Figure-15. 16- Bit reversible ripple carry adder.

5. RESULTS AND COMPARISONS

The proposed reversible UT multiplier designs are functionally verified through a logic simulation process. To perform simulation, test benches are created for the reversible UT multiplier designs. The Verilog HDL is used to code the designs. The simulation is carried out using Xilinx 14.3 ISE. The Figure-16, Figure-17 and Figure-18 shows the simulation waveforms for reversible 4x4, 8x8 and 16x16 Urdhva Tiryakbhayam multipliers.

Figure-16. Simulation results for reversible 4x4 Urdhva Tiryakbhayam multiplier.

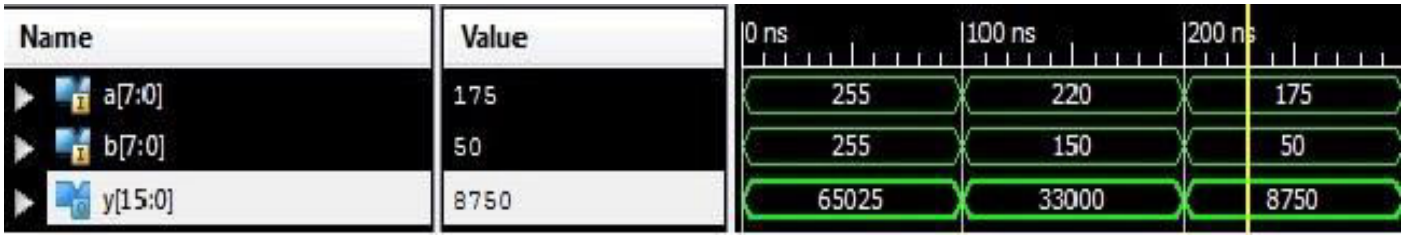

Figure-17. Simulation results for reversible 8x8 Urdhva Tiryakbhayam multiplier.

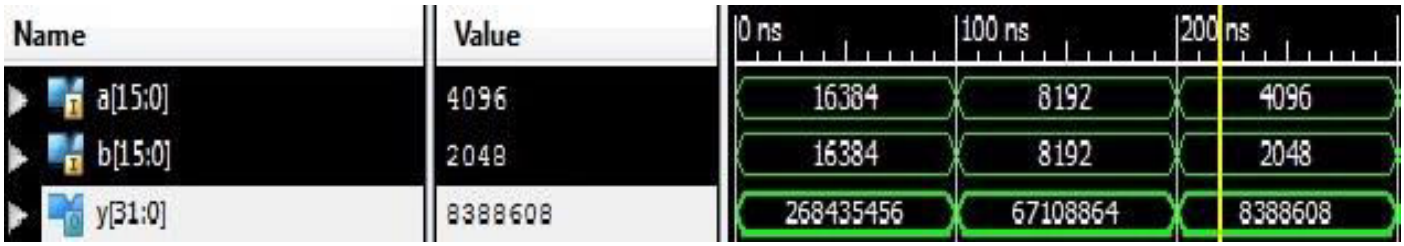

Figure-18. Simulation results for reversible 16x16 Urdhva Tiryakbhayam multiplier.

The comparison between proposed and existing reversible 4x4 Urdhva Triyakbhayam multiplier design parameters are given in Table-1.

Table-1. Comparison of Reversible 4x4 UT Multipliers.

Parameters	4x4 UT Multiplier	
	Proposed Design	Existing Design [7]
No. of gates	31	37
Constant inputs	31	29
Garbage outputs	40	62
Quantum cost	128	162
TRLIC	230	290

The number of reversible gates, constant inputs, garbage outputs and quantum cost for the higher bit (such as 8x8 and 16x16) reversible Urdhva Triyakbhayam multiplier is given in Table-2.

Table-2. Higher bit reversible multiplier parameters.

Parameters	Multipliers	
	Proposed 8x8 UT multiplier	Proposed 16x16 UT multiplier
No. of gates	145	621
Constant inputs	145	621
Garbage outputs	198	866
Quantum cost	628	2740
TRLIC	1116	4848

6. CONCLUSIONS

In this work, multiplier based on Urdhva Triyakbhayam formula of Vedic mathematics is implemented by using reversible logic gates. The obtained result from implemented reversible 4x4 UT multiplier design is compared to the existing reversible UT multiplier which shows the reduction in the number of gates, garbage outputs, quantum cost, TRLIC and also implemented, calculated the design parameters for higher bit reversible UT multipliers.

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