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DESIGN OF FULL SWING LOCAL BITLINE SRAM ARCHITECTURE BASED ON FinFET USING SVL TECHNIQUE

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ABSTRACT

FinFET design was introduced as an alternative for CMOS due to its mitigate short channel effects at lower technology nodes and also scaling of the single bulk MOSFETs faces problems in nanometre technology due to its short scaling effect that causes leakage current to increase. Dual gate FinFET has better short channel effect because of its alignment of the gates. The previous average 8T SRAM has more area and it requires write back scheme. The full scheme local bitline (BL) swing connected to read buffer gate can be obtained with boosted word line (WL) voltage. But we cannot use this voltage because it reduces the SRAM stability and threshold voltage is high. In this paper the SRAM architecture based on FinFET using SVL circuit technique is designed. In the proposed architecture scheme of full swing is determined by cross coupled PMOSs and the gate of the read buffer is driven by full Vdd without the use of boosted wordline voltage. The SRAM based on FinFET is designed on tanner tool. By applying SVL circuit technique the leakage power and the area consumption of SRAM based on FinFET is 83.74µw and 47% which is lower than the normal FinFET based SRAM architecture.

Keywords: architecture, FinFET, SVL technique.

1. INTRODUCTION

A self controllable voltage level (SVL) circuit can supply maximum dc voltage to load circuit in active mode or can decrease the dc voltage to stand-by load circuit. This Self controllable Voltage Level circuit can be applied to the memory circuits and registers to decrease the power in the stand-by mode and also such circuits with SVL techniques can retain data in the stand-by condition [1]. Low power circuit design is not needed only for logic circuit but also for storage circuits.

In this paper SVL technique is used with SRAM (static random access memory) based on FinFET to reduce its leakage power. FinFET is very attractive among dual gate devices and is also known as quasi planar because of its geometry in the vertical direction [2]. The basic diagram of FinFET structure is shown in the Figure-1.

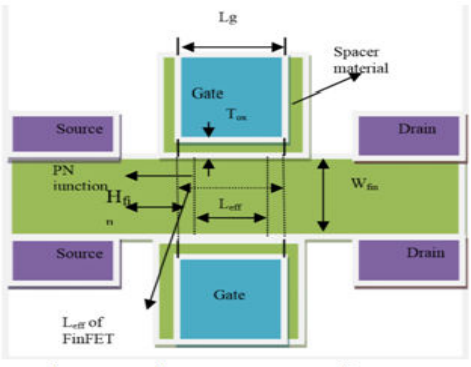

Figure.1 Basic FInFET structure diagram

The proposed 8T SRAM architecture based on the advanced nanometer technique can resolve the half select issue mentioned in the section 2 without the need for write back scheme and it also have more area, full swing local bitline that has smaller read delay [3].

2. LITERATURE SURVEY

There are two well known techniques for reducing power in the stand-by mode (Ps) one is MTCMOS (multi threshold voltage CMOS) [4] and [2]. This reduces power in the stand-by condition (Ps) by disconnecting the power supply through P-MOS switches with higher voltage but its drawback is it requires more fabrication process for higher Vth (threshold voltage) and it cannot retain data in the stand-by mode. Second is VTCMOS (variable threshold voltage CMOS) [5] this also reduces leakage current by raising the substrate bias voltage (Vsub). This technique also has the disadvantage such as very low substrate bias operation, competitive area penalty, competitive power penalty. The power can also reduced by lowering the operating voltage but at operating voltage effect variation in the threshold voltage becomes more significant [6]. SRAM cell is highly susceptible to threshold voltage variations (Vth) so it is designed with small transistors for high density integration. In case of 6T SRAM cell trade off occurs between read stability and write ability. So proposed SRAM cell is added with a decoupled read port that avoids this trade off to which bit-interleaving is not applied [3]. Some SRAM cell is also susceptible to errors induced by α-particles, to address these error SRAM cell has to exhibit bit-interleaving. The selected, half-selected, and unselected cells in a bit-interleaved of the SRAM array [7] is shown in the figure 2. Its operation is explained in the reference paper [3] and [7].

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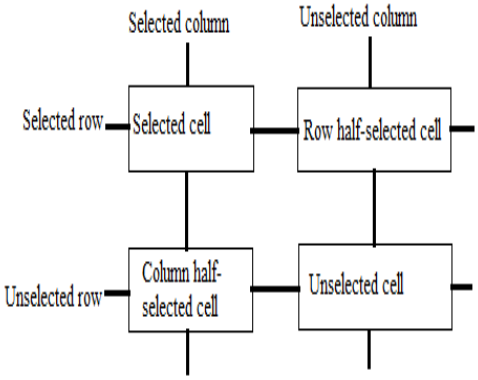

Figure.2 Selected, half-selected, and unselected cells in a bit-interleaved SRAM array

In bit-interleaving half-select issue occurs (half-select issue refers to stability consideration of half selected row cells). To address this issue without using write back scheme 10T SRAM cell of cross point structure was proposed [8]. This method eliminates half-select issue but itb has the drawback that it requires competitive area to balance additional transistors in its architecture. To address these drawback an average 8T SRAM architecture based on 130nm technology was proposed [9]. This also address half-select issue without using write back scheme and have large area. This also has an disadvantage that its read delay raises when it is fabricated using advanced technology such as 22nm technology, that shows variation in the threshold voltage (Vth). All these drawbacks are overcome in this paper by designing SRAM architecture based on 22nm FinFET technology [3] and further its leakage power is reduced in the proposed SRAM cell by using SVL circuit in this paper.

3. PROPOSED SYSTEM

There are three types of self controllable voltage level (SVL) circuits were developed and shown in the Figure-3 [1] and [2]. Type 1 (figure 3(a)) upper SVL circuit which has single p-MOSFET switch (P-SW) and 'q' number of n-MOSFET switches (n-SWs) connected in series. The "on" p-SW (p-MOS switch) is connected to Vdd and load circuit in the active mode and "on" n-SWs, load circuit are connected in stand-by mode. The type 1 upper SVL circuit is shown in the figure 3(a). In the upper SVL circuit at logic '0' p-MOS gets "on" and n-MOS gets "off". When the control signal (CLB) turns "on" n-SW1 (n-switch 1) and turns "off" p-SW (p-switch) Vdd is supplied to the load circuit i.e., inverter through 'q' n-SWs. Thus drain to source voltage is given as,

Vdsn=Vdd-qv

Where v is the voltage drop across single n-SW and 'q' is the number of n-MOS. Vdsn can be increased or decreased by varying qv or either q or v. By increasing qv, Vdsn will get decreased which further increases the barrier height of "off" n-MOS, i.e., it will eliminate DIBL effect (drain induced barrier lowering) and increases threshold voltage. As a result sub threshold current decreases and leakage current through inverter also decreases.

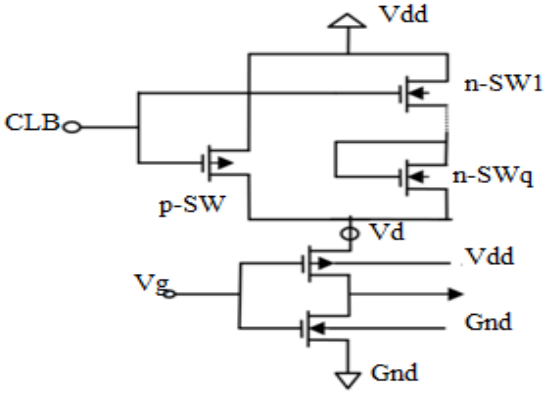

Figure.3(a) Upper SVL circuit

Type 2 is lower SVL circuit (Figure-3(b)) which has single n-MOSFET switch (n-SW) and 'q' number of p-MOSFET switches (p-SWs) connected in series. The lower circuit not only supplies Vss through "on" n-SW to active load circuit but also supplies Vss through "on" p-SWs to the load circuit in stand-by condition. The type 2 lower SVL circuit is shown in the Figure-3(b). In the lower SVL circuit where negative control signal turns "on" p-switch1 (p-SW1) and turns "off" n-switch (n-SW) Vss is applied to the load circuit i.e., inverter in the stand-by mode with zero gate voltage through 'q' p-SWs. Thus drain to source voltage decreases the sub threshold leakage current which further increases the source voltage by qv so that substrate bias voltage is increased and is given as,

Vsub= -qv

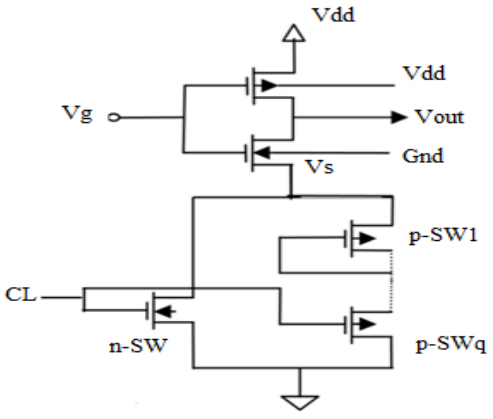

Figure.3(b) Lower SVL circuit

Type 3 (Figure-(c)) is a combination of upper SVL circuit and lower SVL circuit. The circuit of type 3 SVL is shown in the Figure-3(c). The working of type 3 SVL circuit is the combination of type1 and type 2 SVL circuit which further reduces the leakage current and its drain to source voltage is expressed as,

Vdsn= Vdd-2qv

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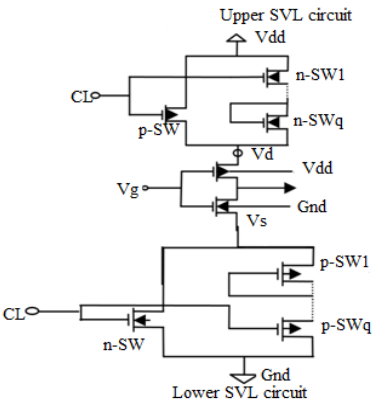

Figure.3(c) Type 3 SVL ciruit (upper and lower SVL circuit)

The basic average 8T SRAM architecture and its operational waveform is shown in the Figure-4(a) and Figure-4(b) [3]. Each block stores 4 bits and 4 pairs of cross coupled inverters, pass gate transistor (PGL 1¬4 and PGR 1¬4), block mask transistor (MASK 1 and MASK 2), write access transistors (WR 1 and WR 2) and read buffers (RD 1¬4).

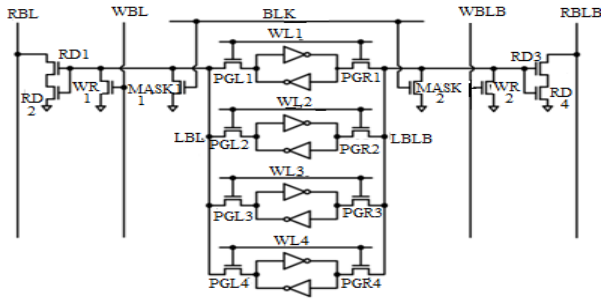

Figure.4(a) Average 8T SRAM architecture

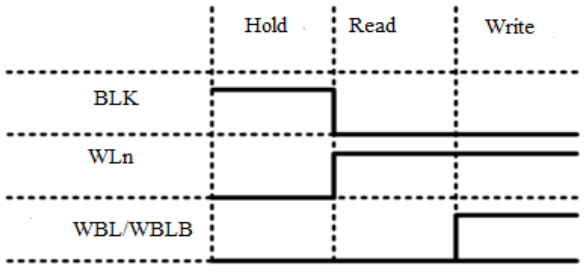

Figure.4(b) Average 8T SRAM operational waverform

A n-MOS is used as read buffer to decrease read BL leakage. It is necessary to have block select signal (BLK) and WLs are row based signals and RBLs and WBLs are column based signals. Its operation is explained is explained un the reference paper [9]. The proposed differential SRAM architecture using SVL circuit and its operation will be explained in section 4.

4. SRAM ARCHITECTURE USING SVL CIRCUIT

The proposed SRAM stores multiple bits in single block, its architecture is shown in the figure 5 that stores 'm' bits in single block [3]. The operating voltage and area depends on number of bits in each block. The architecture that stores 4 bits in single block is selected as basic architecture of proposed SRAM.

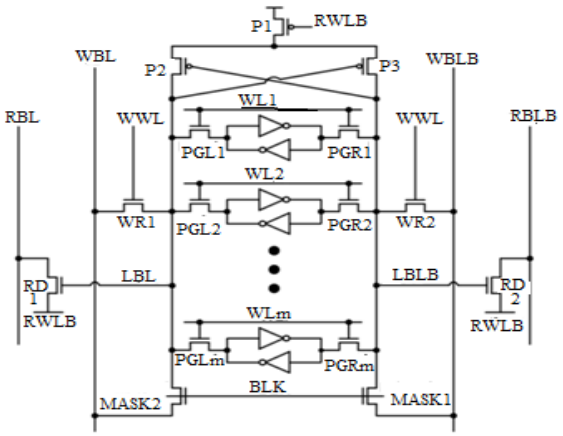

Figure.5 SRAM architecture that store 'm' bits

The configuration of SRAM includes pair of 4 cross coupled inverter, pair of four pass gate transistor (PGL 1¬4 and PGR 1¬4), block mask transistor (MASK 1 and MASK 2), write access transistor (WR1 and WR2) and read buffers (RD1 and RD2), switch (P1) and cross coupled p-MOSs (P2 and P3). The switch and cross coupled pMOSs of the proposed SRAM are the difference from average 8T SRAM architecture. The row based signals are WLs, BLK (block select signal) and RWLB where column based signals are WL, write BLs and read BLs. During hold state WLs, WWL, WBLs are at zero volt. BLK is at Vdd to connect WBLs and LBLs and they are discharged at zero volt and read buffers are turned "off" and RWLB is also at Vdd to turn "off" the switch (P1) to avoid the RBL leakage current. The stand by circuit of the differential SRAM architecture is shown in the Figure-6 [3].

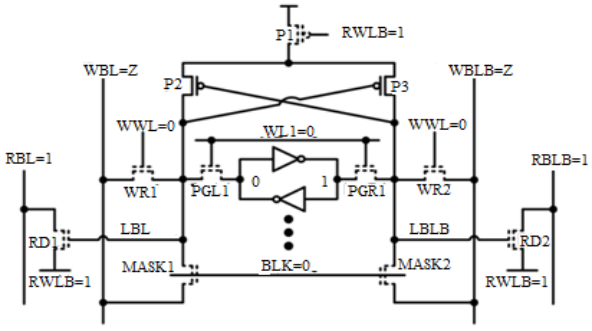

Figure.6 SRAM architecture in stand-by mode

A. Read operation

Read operation of proposed SRAM architecture is shown in the Figure-7(a) and Figure-7(b) [3]. It is operated in two phase. During first phase selected BLK is at zero volt, and selected WL is enabled. Read operation is

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same as that of average 8T SRAM in first phase except that RBL is not discharged because RWLB is high in this phase. With the assertion of WL the read disturbance is small this makes SRAM to operate in low voltage. The next phase starts with falling of RWLB, and enabling the assertion of RWLB it discharges the RBL and also the feedback of cross coupled pMOSs. LBL is increased due to full Vdd value by positive feedback of cross coupled pMOSs by which LBL can achieve entire swing and read buffered gate is operated by complete Vdd without boosted WL voltage. In this case, WL voltage can be used to enable the read stability, and entire swing of LBL reduces the read delay. The advantage of this architecture is that it completely avoids the trade off between read stability and delay.

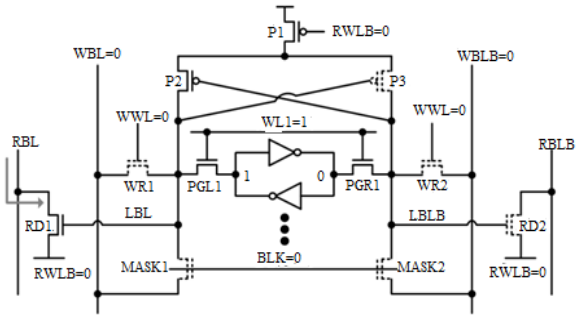

Figure.7(a) SRAM architecture in read opertion

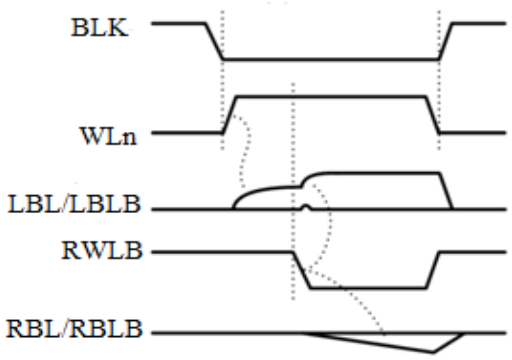

Figure.7(b)Read operation waveform of SRAM

B. Write operation

The write operation of the proposed differential SRAM architecture and its operation is shown in Figure-8 [3]. As shown the selected BLK is at zero voltage and selected WL is enabled, where WWL remains at Vdd so that transistors of write access are turned "on", and voltage level of WBLs are based upon write data. Through pass gate and write access transistor both the storage nodes are connected to WBLs. Thus write operation is differential and the write ability of differential SRAM is better when compared to average 8T SRAM which has single ended write operation.

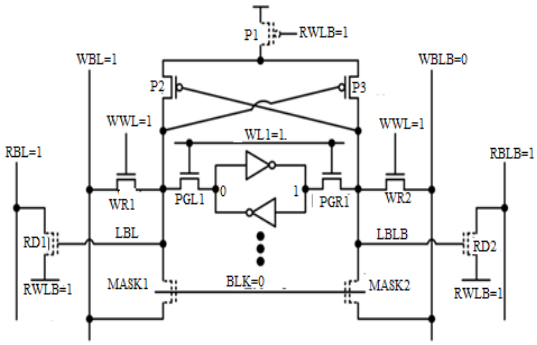

Figure.8 SRAM architecture in write operation

C. SVL circuit operation in SRAM

Differential SRAM architecture based on type 3 SVL circuit is shown in the Figure-9. The SVL circuit supplies lower Vdd and high Vss to the SRAM cell in the stand-by mode. When the negative control signal (CL) becomes high, Vdd increases and Vss reduces to zero voltage. So that SRAM becomes active and operate quickly. Thus by applying SVL circuit operation the power of the SRAM cell in stand-by mode will be reduced drastically.

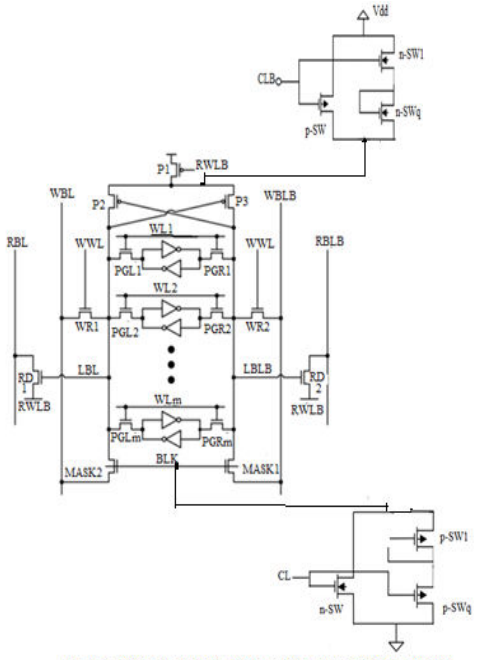

Figure.9 Sram architecture using type 3 SVL circuit

5. SIMULATION RESULT

In this section the simulation of SRAM architecture based on FinFET technology and SVL modified SRAM based FinFET is shown in the Figure-10 and Figure-11. The simulation and design of the circuit is done in the tanner tool using S-edit and the power consumption and area consumption analysis is done using T-spice simulator. The graph of the power consumption of the SRAM and SVL modified SRAM architecture is shown in the Figure-12. The power consumption and area

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of SRAM architecture is 623.38µw & 54% and the power consumption and area of SVL modified SRAM architecture is 83.74µw & 47% where 97% of the power and 7% of the area is reduced.

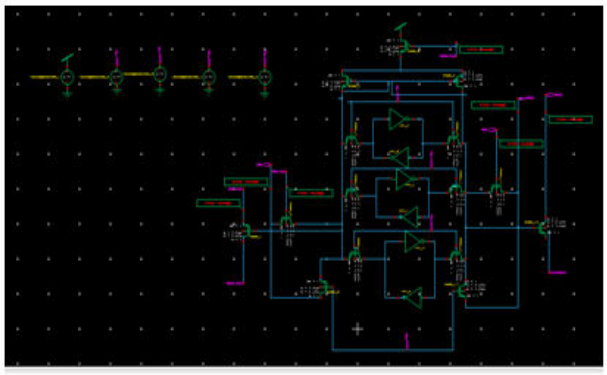

Figure.10 Differential SRAM architecture

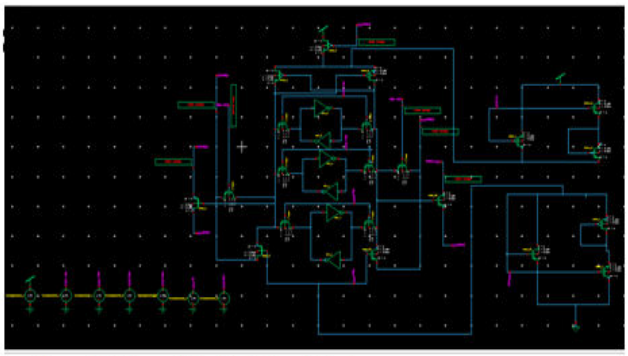

Figure.11 SVL modified SRAM architecture

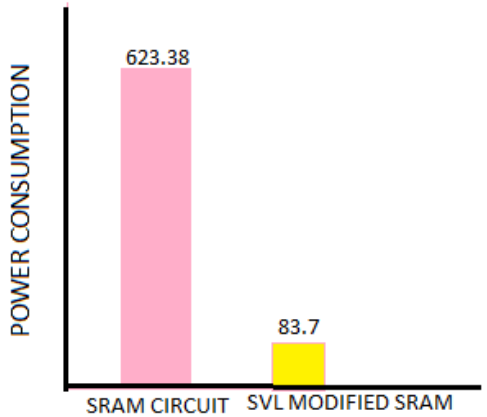

Figure.12 Power consumption comparison

The result shows that SVL modified SRAM circuit consumes less power compared to differential SRAM circuit. And the operating voltage of SRAM architecture based on different configuration is shown in the Figure-13 [3].

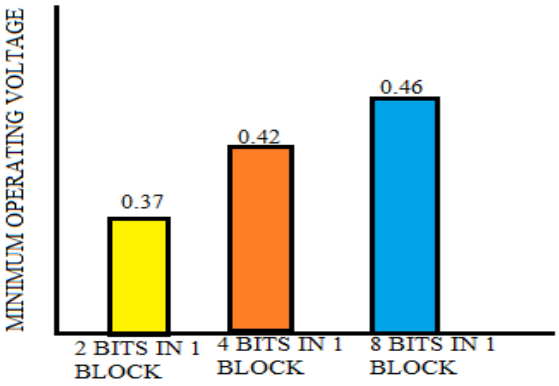

Figure.13 Minimum operating voltage graph

Energy consumed in read and write operations of average 8T SRAM and differential SRAM architecture is shown in the Figure-14 [3].

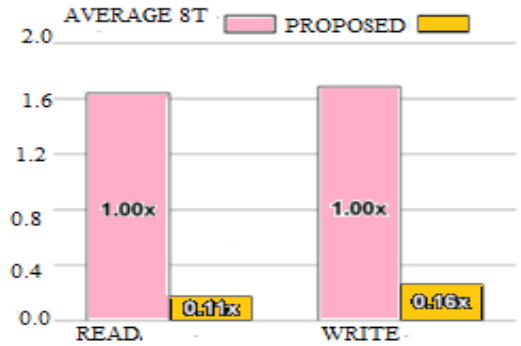

Figure.14 Energy consumption comparison graph

6. CONCLUSIONS

The advantage of average 8T SRAM is that it does not require write back scheme for bit interleaving and it has competitive area. But average 8T SRAM on advanced technology, the complete swing LBL and trade off between read stability and read delay cannot be achieved. Thus the differential SRAM architecture overcomes the drawbacks in average 8T SRAM architecture by eliminating trade off between read stability and read delay. The full swing LBL is obtained using cross coupled pMOSs and gate of read buffer is driven by full Vdd and also WL is used to enable read stability. Further by applying type 3 SVL circuit technique in the SRAM architecture it reduces the power and area consumption.

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