VOL. 13, NO. 6, MARCH 2018 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

A MONOLITHICALLY INTEGRATED PHOTORECEIVER WITH AVALANCHE PHOTODIODE IN CMOS TECHNOLOGY

Zul Atfyi Fauzan Mohammed Napiah[1,2] and Koichi Iiyama[2]
[1]Centre for Telecommunication Research and Innovation, Faculty of Electronics and Computer Engineering, Universiti Teknikal Malaysia Melaka, Malaysia
[2]School of Electrical and Computer Engineering, Kanazawa University, Japan
E-Mail: zulatfyi@utem.edu.my

ABSTRACT

An avalanche photodiodes were fabricated by standard 0.18 µm CMOS process (CMOS-APD) with the maximum bandwidth of 8.4 GHz at the avalanche gain of about 10 and the gain-bandwidth product of 280 GHz. To achieve high-speed photo receivers, two types of TIA which are common-source and regulated-cascode TIAs were simulated by utilizing the output of the CMOS-APDs. The figure of merits of gain-bandwidth product was applied to find better results of the transimpedance gain and bandwidth performance due to trade-offs between them. The common-source TIA produced the transimpedance gain of 22.17 dBΩ, the bandwidth of 21.21 GHz and the gain-bandwidth product of 470.23 THz × dBΩ. Besides that, the simulated results of the regulated-cascode TIA configuration demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth, and 845.35 THz × dBΩ gain-bandwidth product.

Keywords: avalanche photodiode, photoreceiver, transimpedance amplifier, regulated-cascode, common-source.

INTRODUCTION

Optical transmission method has been studied in board-to-board and chip-to-chip data transmission to enhance the data transmission speed in electronic system (Woodward and Krishnamoorthy 1999; Yang *et al*. 2003; Radovanović, Annema, and Nauta 2005). Due to this, a monolithically integration of silicon photodiodes fabricated by complementary metal-oxide-semiconductor (CMOS) with transimpedance amplifiers and others electronic circuits are expected (Tavernier and Steyaert 2009; Youn *et al.* 2009; Huang *et al*. 2011). We have already designed and prototyped avalanche photodiodes fabricated by standard 0.18 µm CMOS process with the maximum bandwidth of 8.4 GHz at the avalanche gain of about 10 and the gain-bandwidth product of 280 GHz (Napiah *et al*. 2016; Napiah, Hishiki, and Iiyama 2017).

Photodiodes by themselves are generally not sufficient to produce signals directly for optical information processing systems. In most cases, the photocurrent produced by the photodiode is quite weak and require electronic amplification before it can be used for further processing. Therefore, it is essential to have an amplification circuit along with photodiode because the CMOS-APDs have no internal gain. The amplification used in this research is TIA.

Recently, a lot of pre-amplifier especially TIA have been widely studied. Several TIA are designed to improve the performance of bandwidth, gain and sensitivity. For instance, the common-gate (CG), common-source (CS), common-drain (CD), and regulated cascade (RGC). To realize the photoreceiver which offer state-of-the-art performance, optimization of each device is necessary. Therefore, we focus on available high-speed TIA which can be integrated with our photodiodes to realize a photoreceiver.

TIA has several advantages such as ease of biasing, high bandwidth, low noise, and low input resistance. Besides that, TIA has to be design wisely because it has some tradeoffs between the sensitivity (due to noise), speed (bandwidth) and transimpedance gain. Transimpedance gain is usually equal to the feedback resistor for large open-circuit amplifications (Razavi 2001). If the output voltage signal is small, post-amplifier is needed to further amplify the signal. The gain is increase with increasing the feedback resistance, but at the same time, the bandwidth of the preamplifier will reduce by increasing the input resistance (Razavi 2001).

In this paper, there are two TIA design which are common-source and regulated-cascode. It is necessary for the TIA circuit satisfy the following conditions; (i) the output signal with sufficient voltage amplitude to make sure the electronic circuit connected to the subsequent stage can be operate, and (ii) have fast response in GHz order. To achieve these conditions, the TIA circuit should have a high-speed response compare to the CMOS-APD and low power consumption.

TRANSIMPEDANCE AMPLIFIER

TIA is one of important building blocks in the whole photo receiver. Since the output current signals from the photodiode are small, the TIA become the most critical part in this design. The overall performance of the photoreceiver is limits by TIA, thus, the tradeoffs between transimpedance gain, bandwidth must be observed. In this paper, there are two TIA design which are common-source and regulated-cascode.

Common-source TIA

Figure-1 shows the voltage-current or shunt-shunt feedback topology so-called common-source TIA. This type of feedback was preferred because it can degrade both input resistance and then increase the bandwidth by increasing the input pole magnitude and output impedance, thus it can produce better drive capability. It is also selected because of the ability to achieve high sensitivity and wide bandwidth simultaneously. By

referring the common source configuration of TIAs as depicted in Figure-1, typically shunt feedback resistance, RF role is to provide low input impedance. Resistive load, RL, on the other hand, is usually used to get wider bandwidth response. However, it suffers from direct trade-off between gain and voltage headroom. The achievable transimpedance gain of each stage is reduced by load resistance which is required the headroom at low voltage supplies. Higher scaled of 65 nm or 45 nm CMOS technologies offer NMOS and PMOS devices with high unity gain cut-off frequencies. Consequently, high-speed data communication can get this advantage by using high scale CMOS technologies. However, as the device size of these technologies is scales down, the breakdown voltage of the transistors is also decreases. Thus, low supply voltage is needed for successful operation. Therefore, the trade-off between gain and voltage headroom for common source TIA is become more critical in nano-scale circuit design.

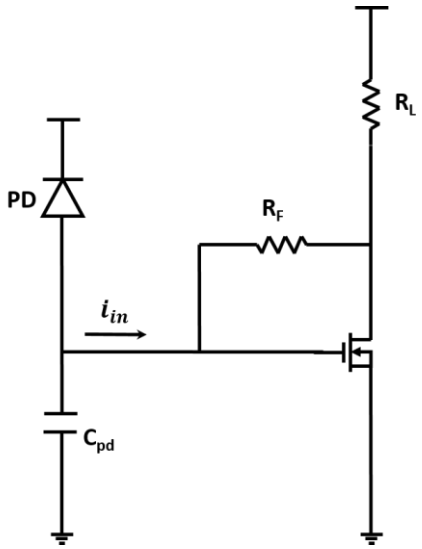

Figure-1. Common-source TIA with shunt feedback.

The transimpedance gain and input resistance of a common-source TIA with shunt feedback are (1) and (2), respectively,

$$Z_{TIA} = \frac{g_m R_F - 1}{g_m R_L + 1} R_L = -R_F \quad (1)$$

$$R_{in} = \frac{R_F + R_L}{g_m R_L + 1} \quad (2)$$

From (1) and (2), a trade-off between transimpedance gain and input resistance of common-source TIA occurs. To make the transimpedance gain higher, R_F needs to be increased, but increasing R_F increases the input impedance which yields the reduction of input pole frequency.

Regulated cascode (RGC) TIA

Figure-2 shows the regulated-cascode (RGC) amplifier that is widely used for TIA design in high-speed optical communication. RGC is well known to deliver the high output impedance and wide output voltage range (Sackinger and Guggenbuhl 1990). RGC is actually a modified common gate amplifier which is the common gate architecture with a local feedback. The common gate amplifier consists of transistor M1 and resistor R1. The local feedback is produced by transistor M2 that has connected between the gate and source of M1.

Resistor R2 and transistor M2 forms a common source configuration that gets a small portion of input signal and then produces a voltage at the gate of M1. At the output of M1, this signal is amplified and then common gate configuration increases the amplified output of M1. The effective transconductance of whole architecture is increased by M2 which benefits to reduce the input resistance to separate the input pole connected with large parasitic capacitance, Cpd from the bandwidth determination. The dominant pole of RGC is usually located within the amplifier rather than at the input node as offer by common gate or common source TIAs. The input resistance and transimpedance of RGC are shown in (3) and (4), respectively (Razavi 2001).

$$R_{in} = \frac{1}{g_{m1}(1 + g_{m2} R_2)} \quad (3)$$

$$Z_{TIA} = \frac{v_{out}}{i_{in}} = \frac{R_1}{s^2 C_{PD} C_0 R_{in} R_{out} + s(C_{PD} R_{in} + C_0 R_{out}) + 1} \quad (4)$$

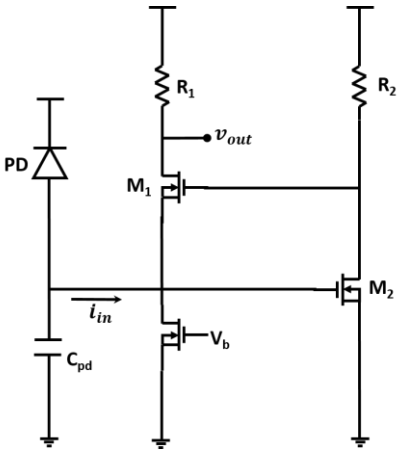

Figure-2. Regulated-cascode (RGC).

The RGC TIA has a good potential for optical receiver applications with high gain, low noise, and lower power consumption characteristics.

CIRCUIT CONFIGURATION

Figure-3 shows the schematic diagram of a common-source TIA. In this circuit, the gain can be increased or decreased by changing the resistances R1 and R2 or the gate width W of the MOSFET. Although the gain can be increased by increasing the value of each parameter, but, it is different for each parameter. Therefore, it is necessary to select the parameter properly according to the feature. In addition, it is desirable that the

gain is large, but as the gain is increased, the range for linear amplification is possibly narrows and maybe the waveform collapses, so it is important to balance with the input signal current.

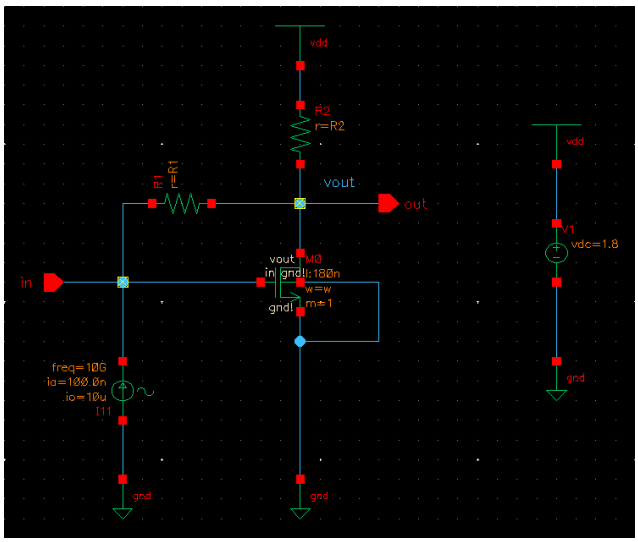

Figure-3. Schematic diagram of a common-source TIA.

Figure-4 shows the schematic diagram of a RGC TIA. In this circuit, the photocurrent is amplified to be a voltage at the drain of M1. The M2 and R3 stage functions as a local feedback to reduce the input impedance by its voltage gain. The input signal used for this circuit is same with previous common-source circuit. The output signal is located between the source of transistor M1 and resistor R2. The input voltage is 1.8 V. The gate length L of all the transistors is 0.18 µm, which is the minimum value in this technology aims for high-speed response.

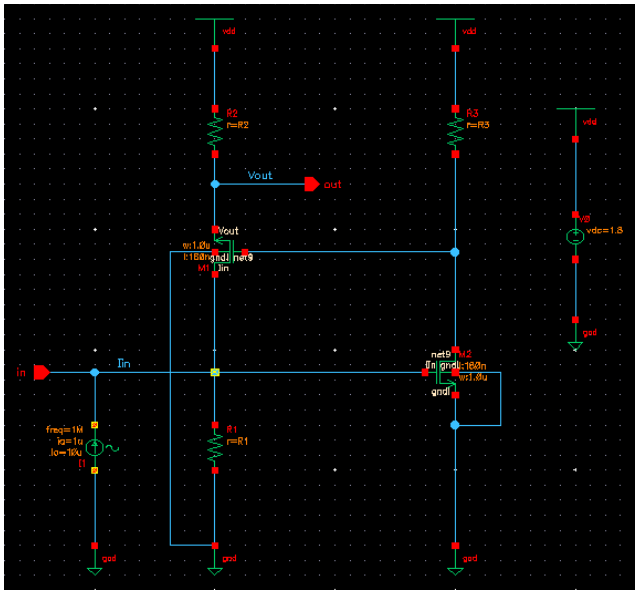

Figure-4. Schematic diagram of a regulated-cascode TIA.

RESULT AND DISCUSSIONS

At first, DC analysis of the CS is done by varied the parameters of resistances R1 and R2 and the gate width W. The gate length L of the nMOS is 0.18 µm, which is the minimum value in this technology aims for high-speed response. By using 3 types of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and 5 types of W: 0.5 µm, 1 µm, 2 µm, 5 µm, 36 simulations were performed in total. As a results,

a) The wider the gate width, the steeper the slope of the IV characteristic, therefore, the gain is increased.
b) Gain is also increased if R1 or R2 value increased.
c) It is more effective to increase the gain if R2 larger than R1.
d) but, if the gain is too high, the linear amplification range becomes narrow, so it is not suitable for the TIA.

In order to investigate whether the simulation is correctly performed, the transient analysis is simulated. Randomly, the simulation was carried out with the resistance value R1 = 10 kΩ, R2 = 10 kΩ, and varied the gate width W to 0.5, 1, 2, 5 µm. Three types of input currents are examined: 0, 25, and 50 µA. As a result, the output current for 0, 25, and 50 µA input current is same with previous DC analysis. Thus, this simulation is in good agreement and can proceeds for frequency response analysis.

To simulate the frequency response, input of the simulation is AC current and the output voltage is in the logarithmic region, then, a -3 dB bandwidth is obtained. To consider which combination that each parameter gives a wider -3 dB bandwidth, the conditions are similar to DC analysis. The resistors R1 and R2 and the gate width W are variables, and the gate length L of the nMOS is fixed to 0.18 µm, which is the minimum value in the process in order to achieve high-speed response. The input signal current was selected as the offset value of 10 µA which is a region where linear amplification is possible in all parameters. The amplitude was set at 0.1 µA, which was sufficiently small with respect to the offset.

A total of 36 simulations were performed by three values of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and four values of W: 0.5 µm, 1 µm, 2 µm, 5 µm. As a results, the resistors that yields the optimum results are R1: 20 kΩ and R2: 50 kΩ. The frequency response for these resistors is shown in Figure 5. Typically, the gain-bandwidth product is a figure of merits that can define the optimum design of the particular circuit because gain and bandwidth is trade-off. Therefore, for this common-source TIA, the optimum parameters are R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 µm, that provide the results of transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ. units.

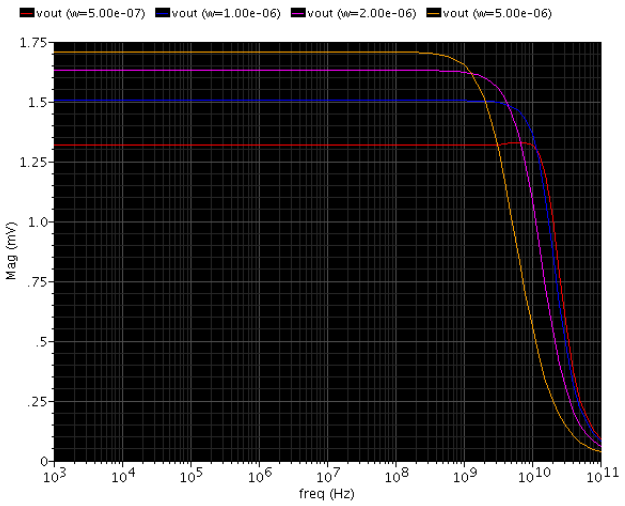

Figure-5. Frequency response of the common-source TIA.

The method used to find the optimum parameters of RGC circuit is quite same with previous common-source circuit analysis. The parameters for this RGC circuit analysis is three types of resistors: R1, R2, and R3. The values are varied for 10 kΩ, 20 kΩ, and 50 kΩ, therefore, a total of 26 simulations were performed. The gate length and width for both transistors are 0.18 µm and 1 µm, respectively. The target bandwidth and transimpedance gain for this RGC TIA are > 9GHz and > 54 dBΩ, respectively. Form all 26 simulations, only four combinations meet both requirements. Based on highest gain-bandwidth product, the optimum combination parameter values of resistors R1, R2, and R3 are 20 kΩ, 10 kΩ, and 10 kΩ, respectively. The bandwidth achieve for this RGC TIA is 10.64 GHz and transimpedance gain of 79.45 dBΩ with the gain-bandwidth product of 845.35 THz × dBΩ. The frequency response is shown in Figure 6.

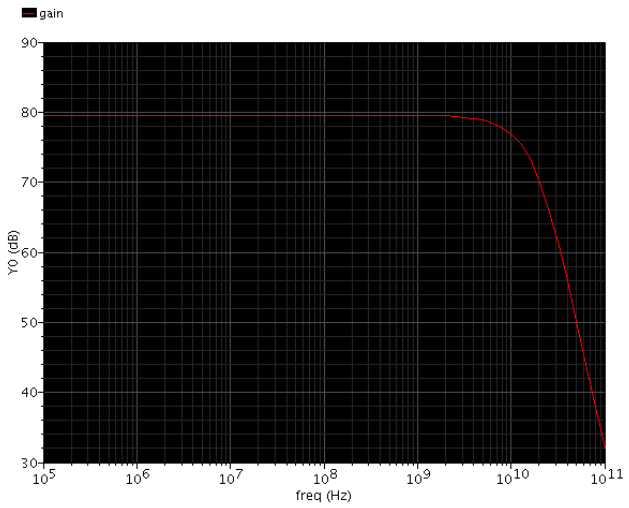

Figure-6. Frequency response of a regulated-cascode TIA.

CONCLUSIONS

The main purpose of this paper is to find the optimum parameters for both type of TIA circuits in term of resistances and channel width of the transistor to achieve high transimpedance gain and high bandwidth performance. But, trade-offs between gain and bandwidth are hindrances to attain optimum performance of the TIA. Therefore, the figure of merits of gain-bandwidth product is used to find the ideal results. The common-source TIA provide the good results of transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ via the optimum parameters of R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 µm. On the other hands, the RGC configuration which is a modified common gate amplifier enhances the effective input transconductance and therefore isolates efficiently the large input parasitic capacitance from the bandwidth determination. It also relaxes the effect of the large input capacitance on the high-frequency noise characteristics. The simulated results of the RGC TIA demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth and 845.35 THz × dBΩ gain-bandwidth product for 20 µA input current. Both of the results of common-source and RGC TIA meet the target of this research to realize a high-speed photo receivers for our successful CMOS-APDs.

ACKNOWLEDGEMENT

The author would like to thank optical and electronic sensing Laboratory, Kanazawa University and supported by VLSI design and educational center (VDEC), the University of Tokyo in collaboration with Cadence Corporation that makes this work possible. The avalanche photodiode has been fabricated in the chip fabrication program of VDEC, University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

REFERENCES

[1] Huang Shih-Hao, Wei-Zen Chen Yu-Wei Chang and Yang-Tung Huang. 2011. A 10-Gb/s OEIC with Meshed Spatially-Modulated Photo Detector in 0.18-CMOS Technology. IEEE Journal of Solid-State Circuits. 46(5): 1158-69.

[2] Napiah Z. A. F. M., Ryoichi Gyobu, Takuya Hishiki, and Koichi Iiyama. 2016. Characterizing Silicon Avalanche Photodiode Fabricated by Standard 0.18 Mm CMOS Process for High-Speed Operation. IEICE Trans. Electron. E99-C (12): 1304-11.

[3] Napiah Z. A. F. M., Takuya Hishiki and Koichi Iiyama. 2017. Wavelength Dependence of Silicon Avalanche Photodiode Fabricated by CMOS Process. Optics and Laser Technology 92 (January). Elsevier: 193-97.

[4] Radovanović Saša, Anne Johan Annema and Bram Nauta. 2005. A 3-Gb/s Optical Detector in Standard

CMOS for 850-Nm Optical Communication. IEEE Journal of Solid-State Circuits. 40(8): 1706-17.

[5] Razavi B. 2001. Design of Analog CMOS Integrated Circuit. McGraw-Hill Higher Education.

[6] Sackinger Eduard and Walter Guggenbuhl. 1990. A High-Swing, High-Impedance MOS Cascode Circuit. IEEE Journal of Solid-State Circuits. 25(1): 289-98.

[7] Tavernier Filip and Michel S. J. Steyaert. 2009. High-Speed Optical Receivers with Integrated Photodiode in 130 Nm CMOS. IEEE Journal of Solid-State Circuits. 44(10): 2856-67.

[8] Woodward T. K. and Ashok V. Krishnamoorthy. 1999. 1-Gb/s Integrated Optical Detectors and Receivers in Commercial CMOS Technologies. IEEE Journal on Selected Topics in Quantum Electronics. 5(2): 146-56.

[9] Yang B., J.D. Schaub S.M. Csutak, D.L. Rogers and J.C. Campbell. 2003. 10-Gb/s All-Silicon Optical Receiver. IEEE Photonics Technology Letters 15 (5): 745-47.

[10] Youn Jin Sung, Hyo Soon Kang Myung J. Lee, Kang Yeob Park and Woo Young Choi. 2009. High-Speed CMOS Integrated Optical Receiver with an Avalanche Photodetector. IEEE Photonics Technology Letters. 21(20): 1553-55.