



# A LOW POWER AND FAST LOCKING ADPLL TO ENHANCE HEALTHCARE MONITORING SYSTEMS FOR ELDERLY PEOPLE

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## ABSTRACT

Wireless Body Sensor Networks are frequently used in remote health care systems, particularly for elderly health care monitoring systems. The most important concerns of these systems are considered to be the accuracy of the data and the latency in transmission. Transceivers used in medical applications have important constraints like low power consumption, size limitation, speed and precise transmission. In this paper, we present a method of increasing the efficiency of the transmission by using an enhanced transceiver with ADPLL by considering short locking time, good locking range and good frequency resolution as focus factors. ADPLL based RF transceiver is used for modulating and transferring the information to the monitoring station or to the hospital. For this, two ADPLLs are compared based on locking time, locking range, power consumption, frequency resolution etc and ADPLL most suited for this application is given.

**Keywords:** all digital phase locked loop, loop control, modified frequency divider, lock monitor, digital controlled oscillator, wireless body sensor network.

## 1. INTRODUCTION

Due to the development of wireless communications, many advance techniques have been applied in medical field. Wireless data transfer gives precise data transfer and reduces clutter in the medical environment which can be useful in monitoring patients without the patients having to go through the pain of getting the appointment and waiting for the turn. Emergency cases also can be given extra care by alerting the medical attendants, doctors, specialists and machine operators thus saving a lot of precious lives. Vital signs such as ECG, EEG etc can be monitored on a regular basis and the tracking of progress is made easier by installing a complete wireless monitoring system with alerts.

Nowadays, the number of aging population is growing. The old aged peoples are dependent on others and every day the dependency ratio is also increasing [12]. The aged population living independently have health problems, safety problems etc. Hence monitoring the health as well as safety of the elders has become mandatory thus making the presence of wireless alert system a must.

To ensure elders to live independently and safely in their homes several techniques have been used. The tele-home care system that continuously monitors the elderly people and also their health care is described by Heng Shuan Chen *et al* [15]. Many robots are designed for aged people's health care and their security applications [14]. The above mentioned approaches are costly and complex and are also difficult for wide promotion.

Wireless Body Sensor Network is widely used in medical field especially for health care system. It consists of wireless sensor nodes placed in various parts of the body to collect information about the patient [11]. The important data usually collected by these sensors are

temperature, heart rate, Electro cardiogram, pressure level and glucose level etc.

The bio medical information collected from various sensor nodes attached to the human body are stored and transmitted by RF transmitter. Conventional RF transmitter is not flexible for this application with respect to power consumption and size of transceiver. For this type of application, the transceiver should be selected in such a way that it enables fast transmission without loss of signals and with low power consumption. Victor Kathan Sarker *et al* describes the important of bio signal transmission using a low power, portable wearable device and presents an Internet of things based system with the above factors [16].

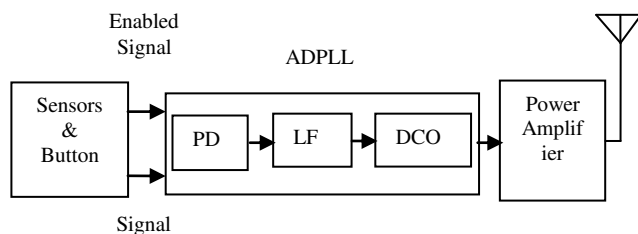
In this paper, the design for transmitter with enhancement is based on All Digital Phase Locked Loop (ADPLL). The sensor detector consists of a button and sensors. During emergency situations like robbery aged people can press the button and it generates an enabled signal. The enabled signal enables the ADPLL transmitter. The ADPLL will transmit the information to the monitoring station or to the hospital. For comparison two ADPLL techniques- Feed forward compensation and Bang bang detector algorithm are taken and the comparison is performed for structure as well as electrical factors.

Frequency search algorithm based ADPLL is hard to implement and the frequency range of oscillator is hard to enlarge [5]. The binary search algorithm used in ADPLL gives fast locking. The important drawbacks of binary search algorithm are trade-off exists between locking time, DCO gain and frequency range [3] [6]. Feed forward compensation technique detects the code based on several ADPLL parameters. The important advantages of feed forward compensation techniques are, it reduces frequency error between the reference clock and divider



clock [7], reduces locking time and it is easy to implement. The bang bang phase detector is used because it consumes low power and also robustness [8] - [10]. The bang bang detector gives slow frequency tracking and high locking time. Modified bang bang phase detector reduces locked time with a high frequency locking range.

The system has three modes- low power mode, active wake up mode and passive wake up mode. During emergency situation when the emergency button is pressed, it will move to active wake up mode. For transferring information, it will move to passive wake up mode, otherwise it will be in low power mode.



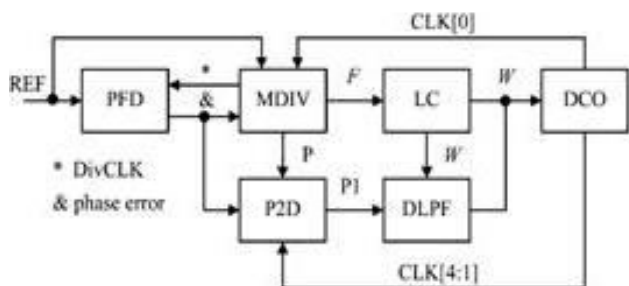
**Figure-1.** ADPLL for monitoring elder people.

The ADPLL based topology gives precise quality in the communication as DCO is always locked by ADPLL.

## 2. ADPLL USING FEED FORWARD COMPENSATION

Feed forwarding techniques directly feed the reference signal as input to the voltage controlled oscillator without passing into the loop filter and other components. Feed forward compensation is difficult to implement in analog systems because conversion of input frequency to output voltage is complex. But in ADPLL as both reference signal input and DCO output are digital conversions it is very simple to implement with little calculations.

ADPLL consists of Phase/ frequency detector, Loop control(LC), Modified frequency divider, (MDIV), Digital loop filter (DLPF), Ring type digital controlled oscillator and Phase to digital converter(P2D)[2].



**Figure-2.** Structure of the proposed ADPLL.

Loop control produces a code and the code is used to tune DCO. DCO output a clock based on code and the clock frequency is 'f.' Modified frequency divider

gives divider value F based on clock frequency and reference value frequency  $f_{ref}$  and it is given by

$$F = f / 2 f_{ref} \quad (1)$$

Consider two codes  $W_1$  and  $W_2$  are assigned to tune DCOs and based on the code two clock frequencies  $f_1$  and  $f_2$  are generated by DCO.  $F_1$  and  $F_2$  are the corresponding frequency divider output for the clock frequencies  $f_1$  and  $f_2$  [2].

The frequency error between  $f_1$  and  $f_2$  can be given by

$$F_1 - F_2 = (f_1 - f_2) / 2 f_{ref} \quad (2)$$

$$f_1 = f_{min} + k_0 \cdot W_1 \quad (3)$$

$$f_2 = f_{min} + k_0 \cdot W_2 \quad (4)$$

$k_0$  is the DCO gain measured in mega hertz and  $f_{min}$  is the minimum frequency

$$K_f = 2 f_{ref} / k_0 \quad (5)$$

$$W_1 = W_2 + K_f (F_1 - F_2) \quad (6)$$

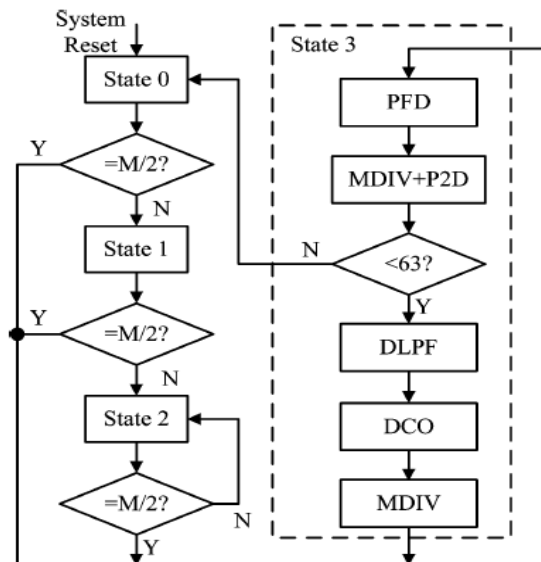
Substitute  $F_1 = M/2$  and  $W_1 = W_{locked}$

$$W_{locked} = W_2 + K_f (M/2 - F_2) \quad (7)$$

Proposed ADPLL consists of two modes-phase acquisition mode and frequency acquisition mode.

### Frequency acquisition mode

Feed forward compensation structure is implemented in this mode. The MDIV is also used as a frequency detector. The output F from MDIV passed to the Loop Control. Loop Control generates code based on the value of F and sends to DCO and DLPF. The mode consists of three states- states 0, 1, 2. Frequency locking will happen when the condition  $F = M/2$ .



**Figure-3.** Flow chart of frequency acquisition mode.

**State 0:** LC produces code  $W_1$  and the corresponding output of MDIV is  $F_1$ . When  $F_1$  equals  $M/2$ , Phase locked loop moves to state 3 else state 1[2].

**State 1:** When  $F_1$  value is greater than  $M/2$ , DCO frequency is higher than desired frequency and this frequency should be decreased. So decrease  $W_2$  value compare to  $W_1$ . When  $F_1$  value less than  $M/2$ ,  $W_2$  value increased. If  $F_2$  is the corresponding output of MDIV and value equals  $M/2$ , then PLL enters state 3, otherwise PLL enters state 2.

**State 2:** Loop Control found the parameter  $K_f$  based on equation 5 and the parameter  $W_3$  based on equation 7. If  $F_3$  not equal to  $M/2$ , it remains in state 2,  $W_4$  will be computed based on  $F_3$ . In this state  $K_f$  value will be reduced to half of previous value based on the relation between  $F$  and  $M/2$  changes (large to small). The process continues until frequency locking condition will happen. After achieving frequency locking, ADPLL enters to phase acquisition mode (state 3).

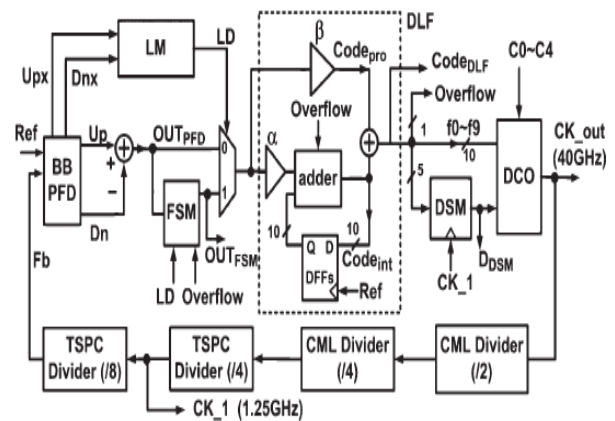
### Phase acquisition mode

Phase locking condition will be achieved when DCO code oscillates between neighbouring codes.

The phase error between divided clock and reference clock will be calculated and it will be converted in to digital values with the help of MDIV and P2D. When the digital value is lesser than 63 then digital values will be send to DLPF. Otherwise, state will turn to state 0. The output of Digital loop filter tunes the DCO and the DCO clock is divided by MDIV and the output of MDIV is sent to phase frequency detector.

### 3. ADPLL USING MODIFIED BANG BANG ALGORITHM

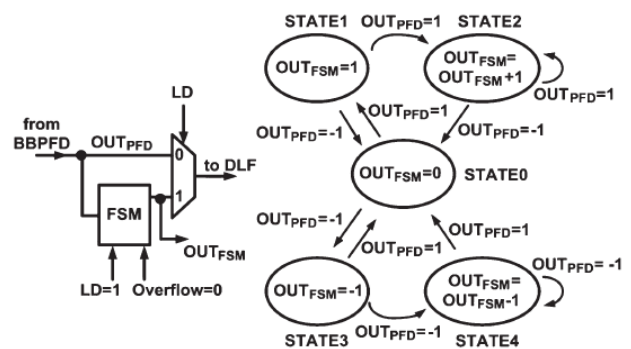
Bang-bang phase detector tracking frequency takes longer time with low power consumption. So bang bang detector is modified in such a way that it reduces the locking time and also to increase the tuning range of DCO.



**Figure-4.** Block diagram of ADPLL.

ADPLL consist of Bang Bang Phase Frequency Detector (BBPFD), Finite State Machine (FSM), Lock Monitor (LM), Digital Loop Filter (DLF), DCO with delta sigma modulator [1].

When the phase error between reference clock and feedback clock is less or equal to reference clock then conventional bang bang operation is enabled. Otherwise modified bang bang operation is enabled; Modified bang bang algorithm can be explained by finite state machine.



**Figure-5.** FSM of modified bang bang algorithm.

Two bits LD and overflow controls the FSM. Lock monitor gives output as LD. Another control bit overflow = 1. When DLF code reaches maximum, then overflow = 1; otherwise overflow = 0. When phase error is equal to reference clock then output of FSM=0 (conventional bang bang operation), otherwise Modified bang bang operation. The above flowchart is based on the condition when LD =1 and overflow = 0 [1].

FSM has five states, when output of FSM =1, then FSM stays in state 1-conventional bang bang operation. If the next OUTPFD =1, then state changes from 1 to 2 and there is an update in the output of FSM. When the OUTPFD is still high the above steps are repeated. If OUTPFD= -1 then FSM output is cleared to zero and state changes to 0.

### Digital control oscillator (DCO)

It consists of inductance, capacitance, oscillator and two varactor arrays. Due to this array, parasitic



capacitances limit the tuning range of DCO to 40 GHz. The frequency tuning range obtained based on simulation is 17.5 MHz and the inductor extended the frequency

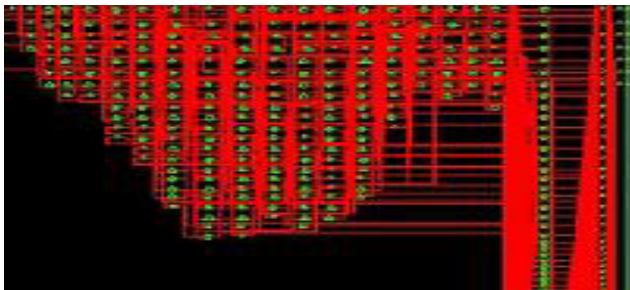
range to 200 MHz. DCO frequency range is between 39.1 to 41.22 GHz.

**Table-1.** Comparisons of two Adpll structures.

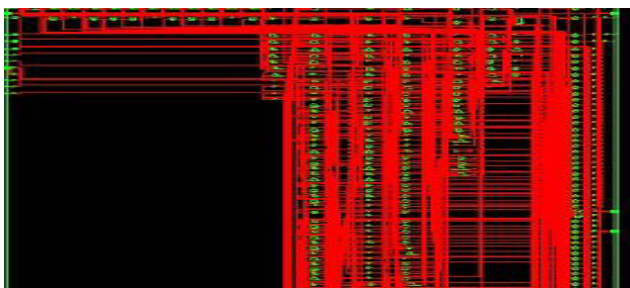
S. No.	Performance parameters	ADPLL based on feed forward compensation	ADPLL based on modified bang bang deteacor
1	Area	0.2mm <sup>2</sup>	0.3mm <sup>2</sup>
2	power	11.394 mW@ 376 MHz	46 mW
3	Locking time	<3 cycles (frequency locking) <19 cycles (phase locking)	15μs (50 MHz)
4	Maximum frequency	416 MHz	40 GHz
	Minimum frequency	4 MHz	-
5	Applications	Frequency synthesis, clock generation, Precision agriculture, Green house management	Distributed clock generation, Efficient transmitter for medical applications

#### 4. RESULTS AND DISCUSSIONS

##### RTL schematic

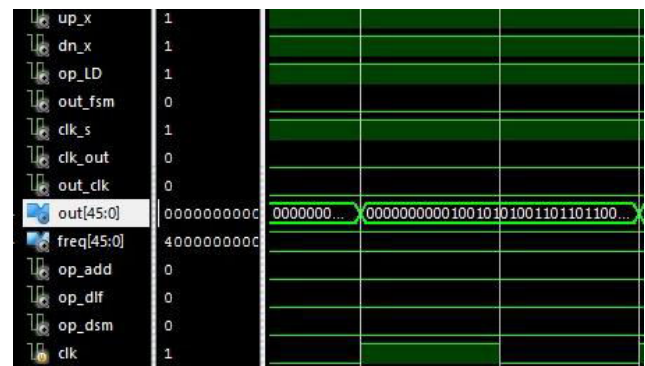


**Figure-6.** ADPLL designed using bang-bang algorithm.



**Figure-7.** ADPLL designed using feed forward compensation.

##### Simulation outputs



**Figure-8.** ADPLL designed using bang-bang algorithm.



**Figure-9.** ADPLL designed using feed forward compensation.





## Power calculations

**Table-2.** ADPLL designed using bang-bang.

S. No.	Clock frequency (KHz)	Power (watts)
1	100	1.403
2	200	1.405
3	300	1.407
4	400	1.408
5	500	1.410

**Table-3.** ADPLL designed using feed forward compensation.

S. No.	Clock frequency (KHz)	Power (watts)
1	100	1.417
2	200	1.418
3	300	1.420
4	400	1.422
5	500	1.424

**Table-4.** ADPLL based on bang bang algorithm-hardware.

Family: Virtex 4 -xc4vlx2900

Logic utilization	used	Available	Utilization
Number of sliced flip flops	109	178,176	1%
Number of 4 input LUTs	101	178,176	1%
Number of bonded IOBs	120	960	12%
Number of Bufg	1	32	3%

**Table-5.** ADPLL based on feed forward compensation-hardware.

Family: Virtex 4 -xc4vlx2900

Logic utilization	used	Available	Utilization
Number of sliced flip flops	117	178,176	1%
Number of 4 input LUTs	105	178,176	1%
Number of bonded IOBs	94	960	9%
Number of Bufg	5	32	15%

## ADPLL based on feed forward compensation: Inference

### Locking time

ADPLL achieves a fast frequency locking by using feed forward compensation and also by reusing frequency divider. Mostly frequency locking times lies in the range 0.25  $\mu$ s to 0.75  $\mu$ s. Phase locking times are much larger than frequency locking times. Phase locking times lie in the range of 2 to 4.75  $\mu$ s. The phase locking times

are directly proportional to the frequency difference between reference clock and divided clock and inversely related to the loop bandwidth. Phase locking time can also be reduced by increasing the band width of digital loop filter.

### Locking range

Frequency locking time is time between initialization of ADPLL and the frequency locking and phase locking time is time between initialization of ADPLL and the phase locking. The Locking range of ADPLL using feed forward compensation is 4MHz to 416 MHz. Within two reference cycles full frequency locking is achieved, locking frequency 376 MHz. Phase locking takes maximum 19 reference cycles.

### Power consumption

Mostly Digital controlled oscillator utilizes more than fifty percentage of power consumption. The important advantage of ring type DCO used in this ADPLL is low power consumption. The delay cell in the Ring based DCO moves to low level state hereby saves power. But still power consumption is 11.394mW because phase locking needs larger reference cycles.

## ADPLL based on Bang Bang operation: Inference

### Locking time

The modified bang bang detector will reduce the locked time. The locked time for a conventional bang bang operation is 1.3 ms and locked time reduced to 1.5 $\mu$ s for a modified bang bang operation. When the reference phase value is increased, locked time will decrease.

### Locking Range

Locking range of ADPLL using modified bang bang operation is 39.13 GHz to 42.21 GHz.

### Power consumption

The delta sigma modulator (DSM) consists of three current mode logic divider and the power is saved by applying the low bias current to the third divider compared to the remaining dividers. Dividers in DSM are realized by single phase clocking logic which reduces active area and power consumption. Bang bang phase detector also consumes low power.

### Frequency resolution

Parasitic capacitances in DCO limit the tuning range of 40 GHz DCO. An inductor of 70 pH connected in parallel with fixed capacitor improves the tuning range and frequency range of DCO increases from 39.13 GHz to 42.21 GHz.

## CONCLUSIONS

In this paper we present a comparison of ADPLL techniques most suited for a health care monitoring system for monitoring the health condition of elder people. The system is designed in such a way that elders can ask for help by themselves using passive wake up mode. ADPLL



transceiver gives fast and precise communication as DCO is always locked by ADPLL. ADPLL based on feed forward compensation and ADPLL based on modified bang bang algorithm are simulated using Xilinx ISE tool and the important parameters like locking time, locking range, total power consumption and frequency resolution are compared.

In ADPLL based on feed forward compensation technique, feed forward compensation technique itself reduces locking time. The largest frequency locking time is 0.75 $\mu$ s and the largest phase locking time is 4.15 $\mu$ s. The phase locking time can also be reduced by bandwidth of digital low pass filter and in ADPLL based on modified bang bang algorithm; modified bang bang detector reduces locking time and also by increasing the reference phase (30ps), locked time reduces to 2 $\mu$ s.

In ADPLL based on feed forward compensation technique, locking range is 4 MHz to 416 MHz and achieves frequency locking in two reference cycles at 316 MHz and in ADPLL based on modified bang bang algorithm, parasitic capacitances present in the LC oscillator limits the tuning range and the output frequency is 40 GHz.

In ADPLL based on feed forward compensation technique, delay cell present in the ring based DCO reduces power and in ADPLL based on modified bang bang algorithm, bang bang detector reduces power consumption and also by reducing the bias current in delta sigma modulator power can be saved.

In ADPLL based on modified bang bang algorithm, an inductor added along with the LC based DCO improves the tuning range and output from 40 GHz increases to 42.21 GHz.

The RF transceiver should be a low power transceiver and the frequency range must be in GHz. As ADPLL based on bang bang detector consumes low power and has good locking range, less locking time, good frequency resolution, fast and precise communications and also the frequency range is in terms of GHz, it is most suited for these applications. The system cost is also less compared to the other techniques.

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