VOL. 13, NO. 7, APRIL 2018 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

SPICE MODEL OF MEMRISTOR WITH THRESHOLD SWITCHING CHARACTERISTICS

N. Khadar Basha and T. Ramashri
Department of Electronics and Communication Engineering, S V University, India
Email: basha.svuce@gmail.com

ABSTRACT

A novel technology Memristor is one of the most promising in the view of their low power consumption, good scalability, and state retention without need of power supply, simple cell structure, nonlinear functionality and compatibility with CMOS technology. From circuit model designer's point of view, any model is to be simple and at the same time, it is as complex as to produce the device properties and applications. The memristor modeling is challenging task because of the linear and nonlinear complexity of the mechanism. we design, reliable SPICE memristor models with threshold switching functionality by using physical parameters and mathematical equations that works based on quantum tunnelling phenomenon provides nonlinear dopant drift and exhibits threshold voltage switching effect with accurate memristor simulation characteristics over a wide range of input voltage and frequency.

Keywords: nonlinearity, SPICE, scalability, memristor, dopant, tunnelling, threshold.

INTRODUCTION

In 1971, Leon Chua formulated equations for electric circuit elements links with the basic physical quantities of charge, current, voltage, and flux. He postulated new equation between the charge and flux, it is considered as the fourth basic element called memristor [1].

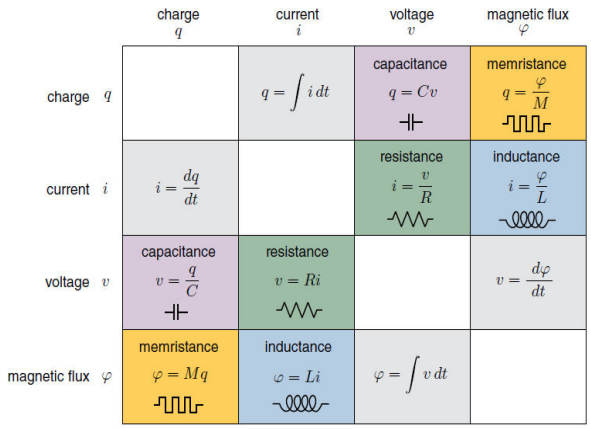


Figure-1. Physical quantities and their relation with fundamental electrical circuit elements.

In 1978, memristor concept was extended to devices and systems design by Leon and Kang [2]. In 2008, memristor was implemented by hardware by HP lab [3]. This gives good clue on working functionality of memristor to more scientists and researchers and they increased their efforts on modeling of memristor and architectures. Memristor fancier a new hope to bring a wave of revolution in electronics. Memristor technology will not totally replace with transistors, but supplement in logic circuits and memories, and also useful in applications of information processing. Implementation of the memristor is not only with TiO_2but also possible with other materials, each material has its own switching thresholds, hence different memristor modes are available [4]-[12]. Most models implemented without threshold voltage and some suffer from 'backing problems'. Threshold voltage switching is an important feature of memristor and responsible for logic operations and non-volatile storage. For switching operation, atomic migration is more responsible for resistance switching i.e change in resistance. Reliable and accurate SPICE model of the memristor is necessary for designing circuits and analysis of complex memristive circuits in biological process and systems. Models have many fitting parameters due to different memristive structures, typical operation and implementation of different materials. Our Model provides nonlinear dopant drift and exhibits threshold voltage effect with accurate memristor simulation characteristics over a wide range of input voltage and frequency. This model is developed to be incorporated in any electronic CAD works. This model is highly parameterized and have the flexibility to change the parameters according to the material properties.

Physical memristor model

Memristor consist of two layers with thin ion oxide is sandwiched between the two terminal electrodes as shown in Figure-2. The top layeris doped with oxygen vacancy and it acts as a semiconductor and bottom layer of ion is undoped layer able to liberate elections when current passed through it, acts as a resistor. The oxygen deficit has charge, they act as positive ions. The slow drift of dopants does not effect on change in resistance i.e contribution of current through the memristor but changing the boundary between the doped and undoped regions is considered as signs of change in resistance. The oxygen deficiency present in TiO_2 able to vary resistance. The total resistance of oxide layer is the sum of contributions of doped region resistance (Ohmic Resistance - R) and undoped region resistance (Tunnelling Resistance - Rt). On other words boundary position of the two layers. If the external power supply applied, then the dopants moved in bi-directionally [3]. For positive applied voltage the total resistance

decreased, i.e. the oxygen deficiency (dopants) moves from the top layer to bottom layer, due to this increases the doped region length. For negative applied voltage the resistance is increased and the doped region shrinks, mostly the oxide layer appears as undoped. The non-volatile behaviour of resistance is used as a state variable to implement the model. In this model, we deliberate on Rt because there is a significant difference between R and Rt. i.e. Rt >> R. It retains low resistance state or high resistance state by removing or generating oxygen deficiency in the oxide layer. The width of the doped and undoped layers must be in nanometers because this dopant tunnelling process is one million times more effective than the dopant process at the micrometer scale. Memristive dopant process observed not only in titanium dioxide [14] - [17] but also in other materials [18] - [21]. The physical memristor exhibits threshold voltage property in which the hysteresis is not seen if the applied voltage is less than threshold voltage [22]. The speed of movement of the boundary from doped region to undoped region varies gradually to zero. This phenomenon is called non-linear dopant drift. Non-volatile resistance is primarily associated with oxide channel. Understanding the oxide layer nature and switching dynamics is a crucial task. Valance Change Mechanism is triggered by channel assisted oxygen anions drifted and valence change of cation sublattice. Based on this mechanism SET and RESET threshold voltage operation performed.

Model equations of memristor

Memristor model works based on state and port equations. For voltage controlled memristor state and port equations are given below (2) and (3) respectively [2].

$$i = G_M(x, v, t)v \tag{2}$$
$$(v = iR_M \rightarrow i = \frac{v}{R_M} \rightarrow i = G_M v)$$

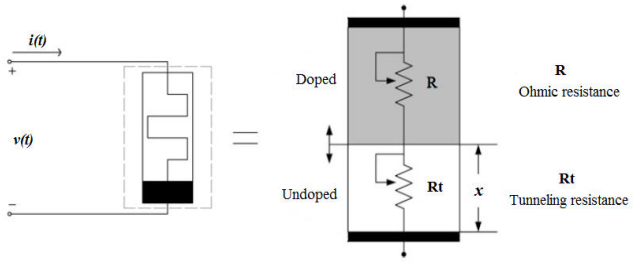


Figure-2. Memristor symbol and physica internal structure.

The current passing through the memristor is calculated as the product of voltage v_M between its terminals and the memductance under the applied voltage $v(t)$.

$$\hat{x} = f(x, v, t) \tag{3}$$

The quantities G_M and R_M denotes memductance (state dependent conductance) and memristance respectively. The corresponding physical units are Siemens and Ohms. The function $G_M(.)$ the function governs the non-linear behaviour and the function $f(.)$ governs how state variable x changes overs time t. v and i are the voltage and current passing through the memristor in the time (t) interval. x represents the single state variable (internal memristor state), which is the thickness of tunnel barrier of undoped oxide layer. The time derivative of state ($\hat{x}$) of voltage controlled memristive system is derived from voltage passing through the memristive port. It represent the movement of barrier between the two layers. The state variable is proportional to tunnelling resistance. If the state variable increases then tunnelling resistance is increases, hence it value is anticipated with boundary under applied polarity of voltage. The derivative of state is controlled by voltage, however such memristor is denoted as Flux Controlled ($G_M(\varphi) = \frac{dq}{d\varphi}$).

The input voltage should be masked in our model to work within the boundary limits at hard switching condition by a function H such that flux is always with in boundaries. The masking function of voltage controlled memristor is defined as

$$H(v) = \begin{cases} v, \ if\ R_M \in (R_{min}, R_{max}) \\ 0, \ else\ if\ v\ does\ not\ pass\ zero. \end{cases} \tag{4}$$

The above equation disregarded any excess applied voltage applied to the memristor. Once it reaches the value of boundary resistance, it hold that resistance regardless of input amplitude. It bring back to the resistive region [23].

The G_M and f are also the functions the various constants related to memristor model initial state and physical properties of memristor. This all depends on the physical realization of memristor and the sway how the device is used to design hardware synapses.

$$x(v, t) = x_0 \left[1 - \frac{p}{y(v,t)}\right] \tag{5}$$

The parameter x_0 represents the maximum value that x can attain in the oxide layer. Tunnelling barrier width (x) is within the restricted range only, hence fitting constant m and function $y(v, t)$ is used to determine the boundaries such that the function $x(v, t)$ gives expected response under applied voltage. The function $y(v, t)$ gives the dynamics and current position of barrier with in the specified boundaries of initial values of y_{min} and y_{max} such that $y < y_{min}$ or $y > y_{max}$. To avoid backing problem [4], [23], [24], in the equation (5) the parameters set as $y_{min} \neq 0$ and $(p/y_{min}) < 1$. The parameter y corresponds to x in the oxide region, hence the tunnelling resistance is set as maximum such that the memristor is in OFF state (R_{OFF}) or its value is set to minimum such that the memristor is in ON state (R_{ON}).

$$sigm(v) = \begin{cases} \alpha \frac{v+v_{thr}}{\gamma+|v+v_{thr}|}, & v \in [-v, -v_{thr}) \\ \alpha \frac{v+v_{ths}}{\gamma+|v+v_{ths}|}, & x \in (v_{ths}, v] \end{cases} \quad (6)$$

Sigmoid function performs switching operations at threshold voltages (v_{ths}, v_{thr}) and perform nonlinear operation ('s' shape curve). The derivative of sigmoid function makes use of quotient rule. This function add or subtracts from the numerator, hence it act as memory feed farward activation function. This divide the voltage - current plot characteristics region into linear and nonlinear, below and above the $|v_{th}|$ respectively.

$$\hat{y}(v,t) = \begin{cases} \beta v, & v \in [-v_{thr}, v_{ths}] \\ sigm(v), & others \end{cases} \quad (7)$$

The fitting constant parameter α, β and γ are used to change the rate of memristance by setting α>>β and γ between '0' and '1'. Based on the material properties this model parameters are changed for switching rates (rate of change of tunnel barrier width) and different thresholds. When β = 0, state change not occurs until the applied voltage reaches threshold.

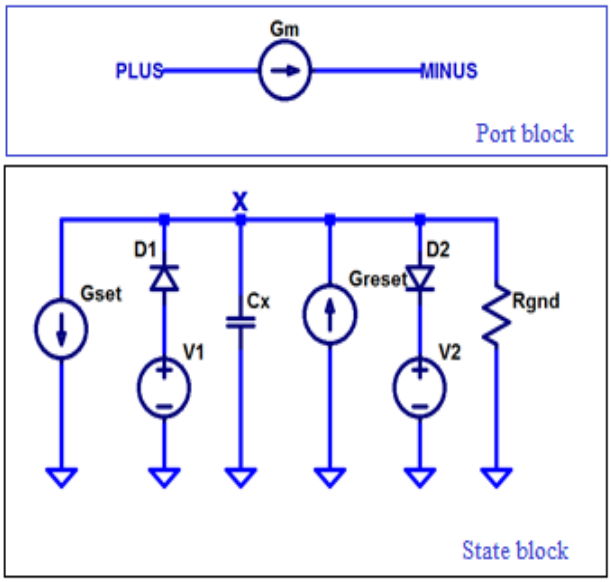


Figure-3. Schematic circuit of Memristor SPICE Model.

Spice model of memristor

Spice simulator model has been used mostly to simulate, analysis and testing complex circuits before actual experimental circuit implementation, thus a lot of time and fabrication cost reduced. The mathematical model equations as mentioned in the previous section is divided into port equations (port block) of memristor and the differential equations for state variable (state block).Spice model depends on the state and port equations as mention above. The port block interact with external environment via its two terminals voltage or current passing through it [5], [25].The port of memristor is modeled by current source G_m. The port current is equal to the ratio of terminal voltage to memristance. i.e. state equations controls the port current of memristor. The current source G_m generate memristor current according the voltage on the memristor Cx.

The state equations are modelled by using the integrator concept. The integrator is implemented parallel combination of G-type current source and capacitor with initial value, this initial value represent the initial state of memristor either in ON state or OFF state. The $G_m$denotes memductance it is the parameter of memristor and its value depends on the flux (temporal integral of voltage) and threshold. The flux in the model is represented as the voltage at node x. The node x voltage is obtained by integrating the terminal voltage with respect to the time. The nodal voltage of node x will represents the numerical value of state variable x. i.e. voltage at node x is equal to the memristance. The port voltage of the model is determined by variable resistance, which is modelled via voltage controlled source at node x. This voltage is used to simultaneously evaluate port voltage. In state block, if current source value is equal to the value which is integrated, then the voltage of the capacitor is equal to the calculated integral during the transient analysis.

In the state block, two voltage controlled current sources G_{set} and G_{reset} are connected in parallel to the capacitor Cx. The voltage across the capacitor is the node voltage at x, which is equal to the value of the function $x(v,t)$. The RESET operation of memristor is modeled by charge feeding into capacitor from $G_{reset}$and the SET operation is performed by letting reversed connected G_{set} by charge draining away from the capacitor Cx[26].

The function f(.) generate pulse when the memristor voltage exceeds threshold voltage. For positive pulse the memristor spice model integrated the value at node x until the value at node x reaches ROFF. At this instant the current source Gx is set to '0' and the memristance value becomes ROFF. The memristor remains in this state until the voltage across the memristor is negative threshold voltage and the function f(.) becomes negative and also the current source Gx becomes negative, then the integral decreases the value at node x and finally this value equal to the RON.

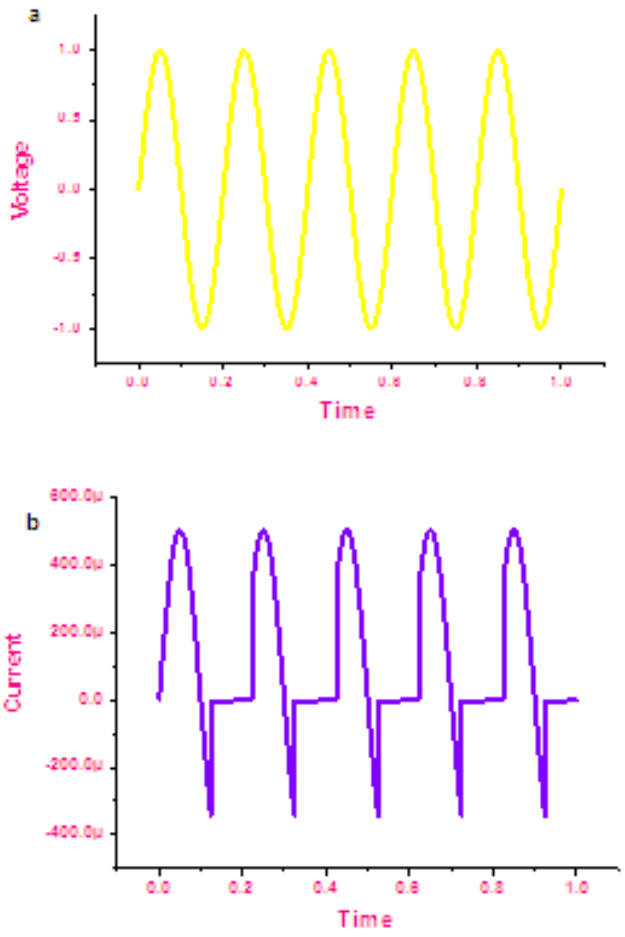
The capacitor is shunted with shunting resistor with large resistance in order to define DC path to ground such the simulator calculate initial dc operating point, it has no effect on simulation results due to its large resistance. The ideal diodes clips the function of memristor when the memristor voltage is greater the threshold voltage. The diode D1 and D2 provide voltage masking (4), either when capacitor voltage is lower than SET or capacitor voltage is greater than RESET voltage, so that the node voltage x is within the boundary conditions for hard switching operations.

RESULTS AND ANALYSIS

The objective of this work is to design and implementation of memristor model with fairly accurate characteristics of physical memristor by solving boundary problems and it is used as a basic circuit element in designing memristor circuits and architectures. To consider a model as memristor model that must satisfy the fallowing fingerprints of memristor. [3], [27], [28].

a) The V-I characteristics of the model must form lissajous (hysteresis) curve pinched at origin when bipolar voltage or current passed through the model.
b) Pinched hysteresis each side lobe area is reduced as the frequency increases.
c) The applied signal frequency tends to infinity, then hysteresis loop degenerates to a straight line through the origin.

This proposed spice model was tested using LTSpice simulation environment successfully and the simulation results of this model is depicted as shown in Figure-4.



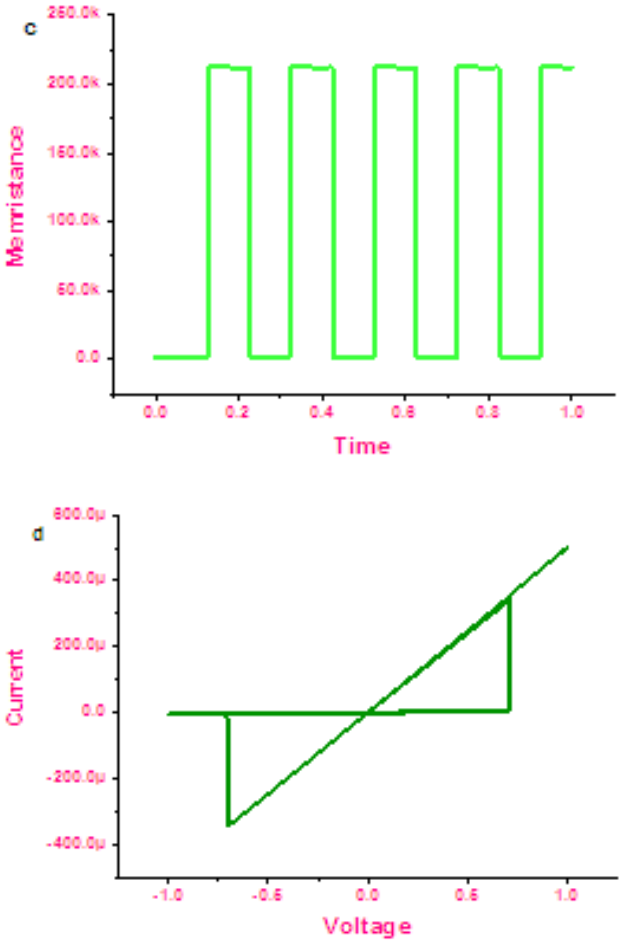


Figure-4. (a) Sinusoidal signal with amplitude 1V and frequency 5Hz applied to memristor. (b) Current passing through the memristor. (c) Memristance of memristor along with the time for applied voltage. (d) V-I characteristics of memristor.

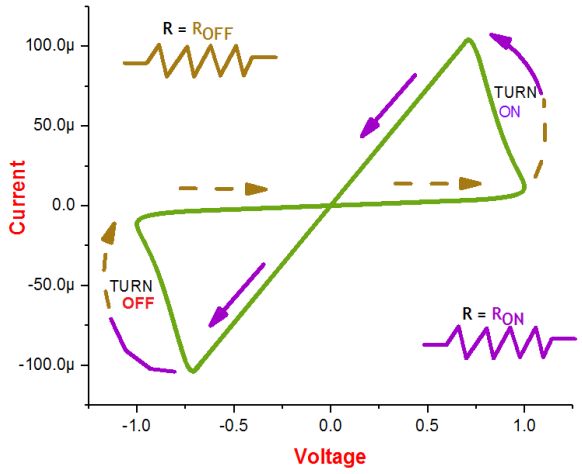


Figure-5. switching dynamics of memristor model at 500Hz.

Here we applied sinusoidal signal with amplitude of 1v at frequency 5hz to our model, the current passing through the memristor is shown in Figure-4(b), here we

observe that when the applied voltage is greater than the applied voltage then the current flows through the memristor and when it reaches the RESET voltage (-0.7V) then there is no current flow until applied voltage reaches SET voltage (0.7V). The change in memristance is observed as shown in Figure-4(c) according to the applied sinusoidal signal. The most important characteristic of memristor hysteresis curve is observed in Figure-4(d), from the hysteresis we observe the operating conditions of memristor, linear and nonlinear operations of memristor and switching behaviour of memristor (Figure-5). Hence our memristor model satisfied the first property of memristor fingerprints.

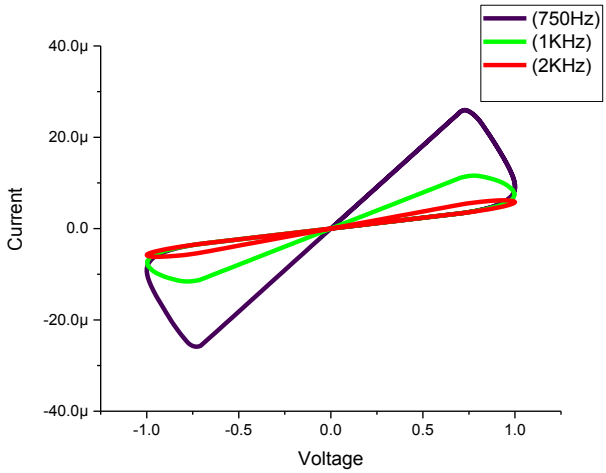


Figure-6. V-I characteristics of memristor model at 750 Hz, 1K Hz and 2K Hz's frequencies.

Next we test the effect of frequency on memristor when applying different frequencies stating from 5 Hz's to 10K Hz's of sinusoidal signals to the memristor, the results are shown in figure 6,the side lobes area in the V-I characteristics are decreasing as frequency is increases as shown in Figure-6. At 750 Hz, 1K Hz and 2K Hz's frequency of sinusoidal signal. When the frequency of signal is increases the V-I characteristics curve form straight line at high frequency as shown in 3D representation of frequency related V-I characteristics, hence our memristor model fallows three memristor fingerprints. In the spice model the convergence problems can be solved by using proper model design rules [5], [29]. Concrete analysis of parameter, proper program options and settings [30] can perform for resolve imperfections and nonconference issues.

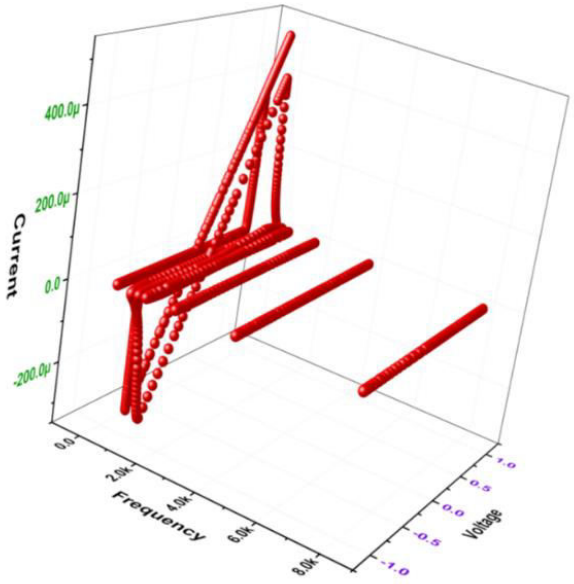


Figure-7. 3D view of VI characteristics of model at different frequencies.

CONCLUSIONS

The simulation results of this model match with the characteristics of the memristor and close to the results of different published memristormodels. Changing the fitting parameters, simulate the device for different physical structures. This model provides boundary assurance, does not require any special window function for setting the boundary and nonlinear drift effect because the model equations itself reflect all device characteristics along with nonlinear drift effect i.e. The nonlinear kinetics of movable dopants are within the boundaries of device. This model is flexible to design different circuits for different areas of applications.

REFERENCES

[1] L. O. Chua. 1971. Memristor - The Missing Circuit Element. IEEE Transactions on Circuit Theory. 18(5): 507-519.

[2] L. O. Chua and S. M. Kang. 1976. Memristive Devices and Systems. Proceedings of the IEEE. 64(2): 209-223.

[3] B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams. 2008. The Missing Memristor Found. Nature. 453: 80-83.

[4] Biolek Z., Biolek D., Biolkova V. 2009. Spice Model of Memristor with Nonlinear Dopant Drift. Radioengineering. 18(2): 210-214.

[5] Biolek Z., Biolek D., Biolkova V. 2009. Spice Modeling of Memristive, Memcapacitative and Meminductive Systems. Proc. of Ecctd '09, European

Conference on Circuit Theory and Design. Antalya (Turkey). pp. 249-252.

[6] Benderli S., Wey T. A. 2009. On Spice Macromodelling of Tio2 Memristors. Electronics Letters. 45(7): 377-378.

[7] Rak A., Cserey G. 2010. Macromodeling of the Memristor in Spice. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 29(4): 632-636.

[8] Biolek D., Biolek Z., Biolkova V. 2013. Spice Modelling of Memcapacitor. Electronics Letters, 2010, Vol. 46, P. 520 - 522. Radioengineering. 22(4): 967.

[9] Biolek D., Biolek Z., Biolkova V. 2011. Pspice Modeling of Meminductor. Analog Integrated Circuits and Signal Processing. 66(1): 129-137.

[10] Kolka Z., Biolek D., Biolkova V. 2011. Hybrid Modelling and Emulation of Mem-Systems. International Journal of Numerical Modelling. 25(3): 216-225.

[11] Pershin Y. V., Di Ventra M. 2013. Spice Model of Memristive Devices with Threshold. Radio engineering. 22(2): 485-489.

[12] Kvatinsky, S., Friedman, E. G., Kolodny, A., Weiser, U. C. Team: Threshold Adaptive Memristor Model. IEEE Transactions on Circuits and Systems I, 2013, Vol. 60, No. 1, P. 211 - 221.

[13] [13] R. S. Williams. 2008. How we found the Missing Memristor. IEEE Spectr Mag. 45(12): 28-35.

[14] S.-G. Park, B. Magyari-Kope, and Y. Nishi. 2008. First-Principles Study of Resistance Switching in Rutile Tio2 with Oxygen Vacancy. In Proc. 9th Non-Volatile Memory Technol. Symp., Pacific Grove, Ca, Nov. pp. 1-5.

[15] M. Fujimoto, H. Koyama, M. Konagai, Y. Hosoi, K. Ishihara, S. Ohnishi and N. Awaya. 2006. Tio2 Anatase Nanolayer on Tin Thin Film Exhibiting Highspeed Bipolar Resistive Switching. Appl. Phys. Lett. 89(22): 223509-1-223509-3.

[16] D. R. Stewart, D. A. A. Ohlberg, P. A. Beck, Y. Chen, R. S. Williams, J. O. Jeppesen, K. A Nielsen, And J. F. Stoddart. 2004. Molecule-Independent Electrical Switching in Pt/Organic Monolayer/Ti Devices. Nano Lett. 4(1): 133-136.

[17] K. Kinoshita, T. Tamura, H. Aso, H. Noshiro, C. Yoshida, M. Aoki, Y. Sugiyama, and H. Tanaka. 2006. New Model Proposed for Switching Mechanism of Reram. In Proc. 21st Ieee Non-Volatile Semicond. Memory Workshop, Monterey, Ca, Feb. pp. 84-85.

[18] Courtade, C. Turquat, C. Muller, J. G. Lisoni, L. Goux and D. J. Wouters. 2007. Improvement of Resistance Switching Characteristics in Nio Films Obtained from Controlled Ni Oxidation. In Proc. 8th Non- Volatile Memory Technology Symposium, Albuquerque, Nm, Nov. pp. 1-4.

[19] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, And Y. Sugiyama. 2007. Low Power and High Speed Switching of Ti-Doped Nio Reram Under the Unipolar Voltage Source of Less Than 3 V. In Proc. IEEE Int. Electron Devices Meet., Washington, Dc, Dec. pp. 767-770.

[20] W. Guan, S. Long, Q. Liu, M. Liu and W. Wang. 2008. Nonpolar Non-Volatile Resistive Switching in Cu Doped Zro2. IEEE Electron Device Lett. 29(5): 434-437.

[21] Y. Dong, G. Yu, M. C. Mcalpine, W. Lu and C. M. Lieber. 2008. Si/A-Si Core/Shell Nanowires as Nonvolatile Crossbar Switches. Nano Lett. 8(2): 386-391.

[22] Y.V. Pershin, M. Di Ventra. 2011. Memory Effects in Complex Materials and Nanoscale Systems. Adv. Phys. 60(2): 145-227.

[23] Shin Et Al. 2010. Compact Models for Memristors Based On Charge-Flux Constitutive Relationships. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 29(4).

[24] A. R Ak and G. Cserey. 2010. Macromodeling of the Memristor in Spice, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions On. 29(4): 632-636.

[25] Pickett M. D., Strukov D. B., Borghetti J. L., Yang J. J., Snider G. S., Stewart D. R., and Williams R. S. 2009. Switching Dynamics in Titanium Dioxide Memristive Devices, J. Appl. Physics. (106), Article No. (074508), pp. 1-6, Doi: 10.1063/1.3236506.

[26] Xudong Fang, Xuejun Yang. 2013. A Compact Spice Model of Unipolar Memristive Devices. IEEE Transactions on Nanotechnology. 12(5).

[27] Leon Chua. 2012. The Fourth Element. Proc. IEEE. 100(6): 1920-1927.

[28] S.P. Adhikari, M.P. Sah, H. Kim, L.O. Chua. 2013. Three Fingerprints of Memristor. IEEE Trans. Circuits Syst. I Reg. Papers. 60(11): 3008-3021.

[29] Kundert K. S. 1995. Foreword By-Gray, P. The Designer's Guide to Spice and Spectre. Kluwer Academic Publishers.

[30] Kielkowski R. M. 1998. Inside Spice. New York (Usa): Mcgraw-Hill.