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CATASTROPHIC FAULT ANALYSIS ON BUTTERWORTH LOW PASS FILTER

Shailaja Mantha[1] and Asha Rani. M[2]
[1]Department of Electronics and Computer Engineering, Sreenidhi Institute of Science and Technology, Hyderabad, India
[2]Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University, Hyderabad, India
E-Mail: shailaja.mantha@gmail.com

ABSTRACT

Testing of analog circuit is a challenging domain compared to digital circuits. This is mainly due to the difficulty to access the internal nodes. To prevail this difficulty an approach is presented for testing of Analog circuits. In this paper a hierarchical method for detection, location and identification of a single catastrophic fault is proposed. The circuit under test (CUT) is analyzed with different values of components which can be faulty. The response of the circuit is analyzed considering few parameters for analysis. A Fault dictionary consisting of these parameters is developed. This method uses top down Hierarchal testing of the system. Using this proposed method, single catastrophic faults in an analog circuit can be identified.

Keywords: testing of analog circuits, hierarchal testing and catastrophic faults, fault dictionary.

1. INTRODUCTION

Analog circuits are continuous in nature. The complexity of the circuit, the relation between excitation and response and the nonlinearities of the elements of the circuits are the main cause which make the analog testing a tough task. Analog faults can be categorized as catastrophic faults (hard faults) and parametric faults (soft faults). Hard faults occur when there are sudden huge variations in the circuit components leading to an unacceptable deviation in the response of the system. Soft faults occur if the value of the parameter varies with time leading to a variation in circuit functionality. Analog fault diagnosis methods are generally classified into simulation after test (SAT) and simulation-before-test (SBT) [2, 3].

1.1 Simulation-after-test methods

The standard methods in SAT are namely parameter identification and fault verification. The first step of parameter identification technique is to formulate sufficient number of independent equations from the measurements to determine all component values. A component value that lies outside the design tolerance range specification is identified as a faulty component.

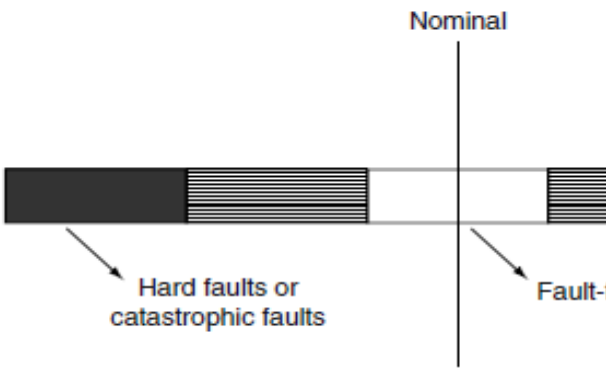

Figure-1. Taxonomy of faults [1].

The fault verification methods use almost the same equations as are used in the parameter identification approaches, except that in the fault verification approaches, circuit components are partitioned into two classes, a fault-free class (class1) and a faulty class (class2). It is assumed that all components in class1 are fault-free and all faults are localized in class2. Using the measurement data and the nominal characteristics of all circuit components, test equations are formulated and expressed as functions of deviations of class2 components. Test equations are over determined and can be satisfied only if all faults are indeed confined in class2. This technique of making assumptions on faults and checking their validity is called fault verification.

1.2 Simulation-before-test methods

In this method a fault dictionary is developed which contains the nominal response of the system in DC, time domain and frequency domain .The parameters that decide the effectiveness of this method are appropriate selection of input signals, test nodes, etc. The response parameters obtained at different test nodes are compared with nominal values and thus the deviation is calculated.

2. ANALOG FAULT DIAGNOSIS METHODS

2.1 In circuit testing and functional testing

In-circuit testing and functional testing are Initial methods of analog testing. In in-circuit method, the component which is to be tested is electrically isolated from other components connected to it. The functionality is performed independently. As the complexity of the circuit increases, the number of test pins required to access the component connections become difficult. In Functional testing, various input signals are applied to the circuit and the functionality of the circuit is verified. The main disadvantage of the functional testing method is to detect a faulty component [4].

2.2 System level testing using correlation functions

In this proposed method, the analog circuit to be tested is excited with a sequence of pulses and the response is compared with signature of known fault free response. The test sequence is a pseudorandom binary sequence which is compatible with digital BIST circuitry. These sequences have well defined properties and can be used to estimate the impulse response of the analog circuit under test (CUT). This method compares the signatures of the autocorrelation and cross-correlation functions of the fault free circuit with those of the CUT. A tolerance window is placed around the functions of the fault free circuit. If either of the functions of the CUT generates a signature that falls outside the tolerance window, then the fault is said to have occurred and can be detectable [5].

2.3 Testing of Analog circuits using spectral analysis

In this method, the power spectral density (PSD) of the fault free circuit is calculated. The basic idea is shown in Figure-2. In the training phase, a random noise with known statistical characteristics is applied to the input of the fault-free circuit, and the PSD of the output is estimated. This is kept as the signature of the fault-free circuit. In the testing phase, the PSD of the circuit under test (CUT) is estimated and compared to the signature of the fault-free circuit.

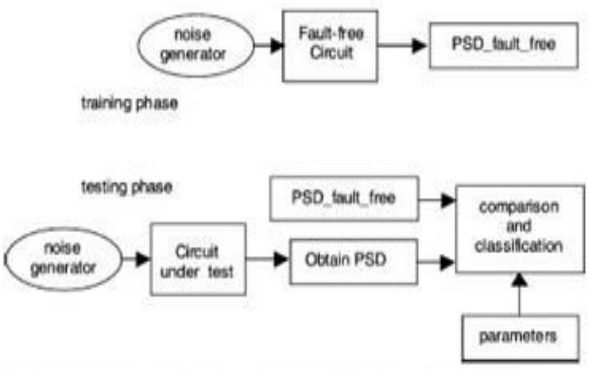

Figure-2. Testing using power spectral density estimation [6].

The major disadvantage of this method is that it masks the soft faults as it has low frequency resolution.

2.4 Testing of Analog circuits using transient output voltage

In this method, the transient output voltage of analog circuits was used for fault detection. The circuit is excited with an input signal and its response is analyzed.

The features from the response are extracted and analyzed. The selected features of transient response are: the magnitude component values of the first four harmonics in frequency domain, the peak to peak value, the maximum value, the standard deviation, and the mean value in time domain. The fault free circuit is also excited with an input signal and its response features are analyzed. If the CUT is faulty, the relations of features will be disturbed. They will be different with those in fault-free circuits [7].

2.5 Testing of Analog circuits using sensitivity analysis

Sensitivity gives a scale of the circuit's performance change in response to a change in the circuit elements values. Sensitivity is defined as the effect of a change in the element **x** to the resulting change in the circuit performance parameters T. Differential sensitivity is defined as the change of the output parameters T due to an infinitesimal change of the element x ($\Delta x \rightarrow 0$) . The following equation defines the differential sensitivity of parameter Tj with respect to component X_i [8].

$$S_{X_i}^{T_j} \stackrel{\text{def}}{=} \frac{X_i}{T_j}\frac{\partial T_j}{\partial X_i} = \frac{\frac{\Delta T_j}{T_j}}{\frac{\Delta X_i}{X_i}} \Big|_{\Delta X_i \rightarrow 0} \quad (1)$$

3. ACTIVE ANALOG FILTER

An active filter is a network of passive R, C elements, and one or more active elements. The active element is usually one or more op-amps. Active filters offer accuracy, stable tuning, and high immunity to electromagnetic interference. The high input and low output impedance found in active filters allow combinations of two or more stages without the interaction found in passive cascades. Active filters function similar to simple, frequency-selective control systems; as such, any desired filter characteristic can be generated from the interconnection of integrators, inverter, summing amplifier, and integrators.

3.1 Design of active filters

For the design of filters, the conditions that are required are:

- The selection of set of frequencies (the pass band) along with the type of the frequency response. This indicates the selection of filter and the centre or corner frequencies.
- Input and output impedance requirements.
- Dynamic range of the active elements - The amplifier should not saturate at the expected input signals, nor should it be operated at such small amplitudes where noise dominates.
- The range to which superfluous signals should be attenuated.
- The acceptable "ripple" (variation from a smooth response, in decibels) within the pass band of low pass and high-pass filters, along with the shape of the frequency response curve close to the corner frequency [9, 10]

3.2 6th Order butterworth low pass filter

The Butterworth filter has a smooth frequency response in the pass band. It is also known as the maximally flat magnitude filter. It has a flat frequency response with no ripples in the pass band and rolls off towards zero in the stop band. The gain $G(\omega)$ of an n-

order Butterworth low pass filter is given in terms of the transfer function H(s) as:

$$G^2(\omega) = |H(j\omega)|^2 = \frac{G_0^2}{1 + (\frac{j\omega}{j\omega_c})^{2n}} \quad (2)$$

Where n is the filter order, ω_c = cutoff frequency and G_0 is the DC gain of the filter.

A LPF has a constant gain, 0 Hz to cut off frequency f_c. At f_c the gain will be 0.707 times the constant gain, after f_c, it decreases at a constant rate with an increase in frequency. The gain is decreased by 20dB whenever the frequency is increased by 10 times. Hence the rate at which the gain rolls off after f_c is 20dB per decade or 6dB per octave [11].

The circuit shown in Figure-3 can be considered as three stages. The input section is considered as stage1, the middle section is considered as stage2 and the last section is considered as stage3. Each stage has its individual gain and the overall performance of the circuit depends on all the three stages. The parameters considered in this circuit for catastrophic fault identification are output voltage, dB value, -6dB frequency and -20dB frequency. The following are the observations at each stage with the application of 1mv signal at the input of first stage:

STAGE 3:	output voltage (mv)	4.204
	dB (max)	-47.548
	(-6 db) frequency	1.0994 KHz
	(-20 db) frequency	1.469 KHz
STAGE 2:	output voltage (mv)	1.693
	dB (max)	-55.423
	(-6 db) frequency	0.8366 KHz
	(-20 db) frequency	1.633 KHz
STAGE 1:	output voltage (mv)	1.0679
	dB (max)	-59.429
	(-6 db) frequency	1.035 KHz
	(-20 db) frequency	3.0289 KHz

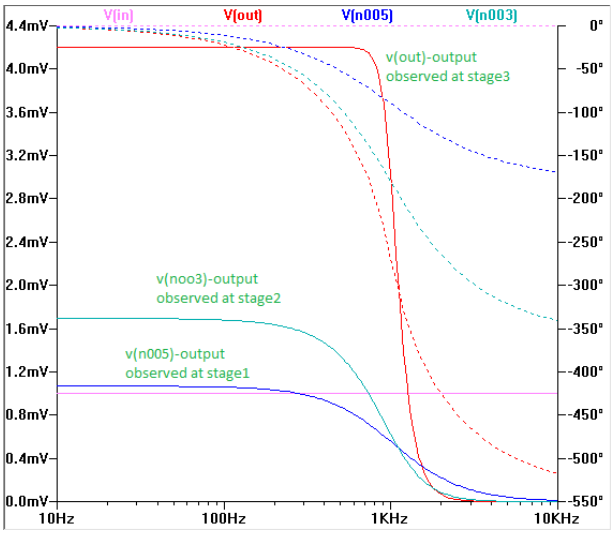

Figure-3. Fault free response of 6th order butterworth low pass filter.

3.3 Effect of single catastrophic fault on 6th order butterworth low pass filter

Each stage is consisting of an operational amplifier, resistors and capacitors. In this section, the effect of catastrophic faults is analyzed. All the possible combinations (short and open) of each resistor and capacitor for each stage have been analyzed. The first assumption made is single catastrophic fault at a time for the entire circuit. The second assumption is that the operational amplifier is considered fault free.

Table-1 showcases the result analysis mentioning the deviation with respect to fault free circuit when a single fault is considered in the entire circuit.

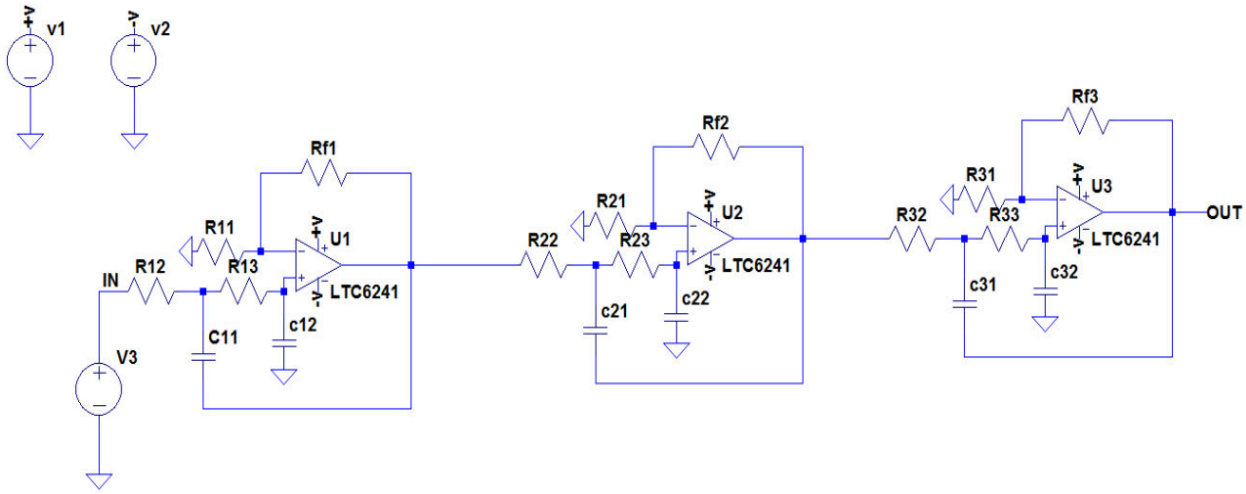

Figure-4. Butterworth low pass filter (6th Order) [12].

Table-1. BWLPF-6th order comparative analysis results with single fault (V_{in} =1mv).

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S. No	Analysis for	Stage3				Stage2				Stage1			
		output voltage (mv)	**dB** (max)	(-6 dB) **freq KHz**	(-20 dB) **freq KHz**	**output voltage** (mv)	**dB** (max)	(-6 dB) **freq KHz**	(-20dB) **freq KHz**	**output voltage** (mv)	**dB** (max)	(-6 dB) **freq KHz**	(-20 dB) **freq KHz**
1	**Fault free**	**4.204**	**-47.548**	**1.0994**	**1.469**	**1.693**	**-55.423**	**0.8366**	**1.633**	**1.0679**	**-59.429**	**1.035**	**3.0289**
Catastrophic fault analysis mentioned as percentage increment or decrement (compared with fault free)													
2	R11 Open	↓6.37	↑1.53	↓0.55	↑0.01	↓6.38	↑1.26	↓1.66	↓0.55	↓6.49	↑0.98	↓3.38	↓0.43
3	R12 short	No change	↓0.05	↑7.97	↑11.50	No change	No change	↑19.53	↑26.39	No change	No change	↑68.70	>100
4	R12 open	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100
5	R13 short	0.12	↓0.05	↑9.12	↑12.39	No change	No change	↑22.64	↑29.26	No change	No change	↑78.94	>100
6	R13 open	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100
7	RF1 Short	↓6.40	↑1.14	↓1.11	↓0.55	↓6.38	↑1.02	↓2.75	↓1.09	↓6.38	↑0.96	↓2.85	↓0.43
8	R21 open	↓37.11	↑8.40	↓9.04	↓4.90	↓37.05	↑7.61	↓21.32	↓8.52	↓0.53	↑0.27	↑1.58	↑0.69
9	R22 short	No change	↓0.05	↑1.31	↑5.92	No change	No change	↓5.45	↑18.22	No change	No change	No change	↑0.56
10	R22 open	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	No change	No change	No change	No change
11	R23 short	No change	↓0.05	↑9.32	↑16.88	No change	No change	↑14.87	↑51.93	No change	No change	↓0.10	↑0.10
12	R23 open	↓100	↓100	↓100	↓100	↓100	↓100	↓100	↓100	No change	No change	No change	No change
13	RF2 Short	↓36.96	↑8.39	↓9.55	↓4.90	↓37.24	↑7.25	↓20.88	↓7.53	↓0.37	No change	↑0.39	↑0.69
14	RF2 open	↓100	>100	↓49.25	↑13.68	>100	↓64.71	↓97.61	↓93.72	No change	No change	↑0.45	↑0.13
15	R31 short	>100	↓66.79	↓98.10	↓92.96	No change	↑0.10	No change	↑0.02	↓0.06	↑0.11	↑0.45	↑0.13
16	R31 Open	↓59.82	16.83	↓43.06	↓17.72	↓0.24	0.10	0	0.02	↓0.07	↑0.09	↓0.10	↑0.13
17	R32 short	↓0.02	↓0.04	↓35.69	↓6.64	No change	No change	↓0.19	0.31	↓0.01	No change	↓0.10	↑0.30
18	R32 open	↓100	↓100	↓100	↓100	No change	No change	No change	No change	No change	No change	No change	No change
19	R33 short	↓0.02	↓0.04	↓27.69	↑3.40	No change	No change	↓0.07	No change	↓0.01	No change	↑0.39	↑0.10
20	R33 open	↓100	↓100	↓100	↓100	No change	No change	No change	No change	No change	No change	No change	No change
21	RF3 Short	↓59.90	↑17.09	↓43.69	↓18.24	↓0.30	↑0.12	No change	No change	↓0.30	No change	↑0.45	↑0.13
22	RF3 open	>100	↓67.19	↓98.14	↓93.16	No change	No change	↓0.67	No change	↓0.08	No change	↑0.39	↑0.10
23	C11 short	↓100	>100	↓50.83	↓88.61	↓100	>100	↓65.87	↓97.12	↓100	↑96.08	>100	>100
24	C11 open	↓0.10	↓0.02	↓3.31	↓0.55	↓0.18	↑0.03	↓13.02	↑1.65	↓0.04	0	↓16.12	↑64.09
25	C12 short	↓100	>100	↓41.78	↓85.14	↓100	>100	↓37.60	↓92.39	↓100	>100	↓37.26	↓93.93
26	C12 open	↑33.90	↓5.38	↑11.79	↑20.15	0	↓0.01	↑57.08	↑92.03	↓0.18	↑0.02	>100	>100
27	C21 short	↓100	>100	↑79.55	>100	↓100	>100	↑22.88	↑84.68	↓0.08	No change	↓0.10	↑0.10
28	C21 open	↓0.05	↓0.04	↓13.50	↓4.90	↓0.24	↑0.01	↓30.41	↓8.01	↓0.08	No change	↓0.10	↑0.10
29	C22 short	↓100	>100	↓44.06	↓88.43	↓100	>100	↓45.73	↓94.36	↓0.01	No change	↓0.10	↑0.10
30	C22 open	↓0.02	↓0.04	↑6.91	↑13.69	No change	No change	↑8.53	↑39.53	↓0.01	No change	↓0.10	↑0.10
31	C31 short	↓100	>100	↓24.41	↑10.55	↓0.01	No change	No change	No change	↓0.04	No change	↓0.10	↑0.10
32	C31 open	↓0.10	↓0.03	↓49.43	↓20.01	↓0.01	No	No	No	↓0.04	No	↓0.10	↑0.10

							change	change	change		change		
33	C32 short	↓100	>100	72.64	>100	↓0.01	No change	No change	No change	↓0.04	No change	↓0.10	↑0.10
34	C32 open	↓0.05	↓0.03	↓42.79	↓14.02	↓0.01	No change	No change	No change	↓0.04	No change	↓0.10	↑0.10

4. RESULTS

The simulated result shown in Figure-5 is when the resistor R13 is shorted. The response obtained at stage 3 (V_{out}) has a spike when compared with fault free. This fault is in the stage1 but it is affecting stage 3, stage 2 and stage 1 parameters.

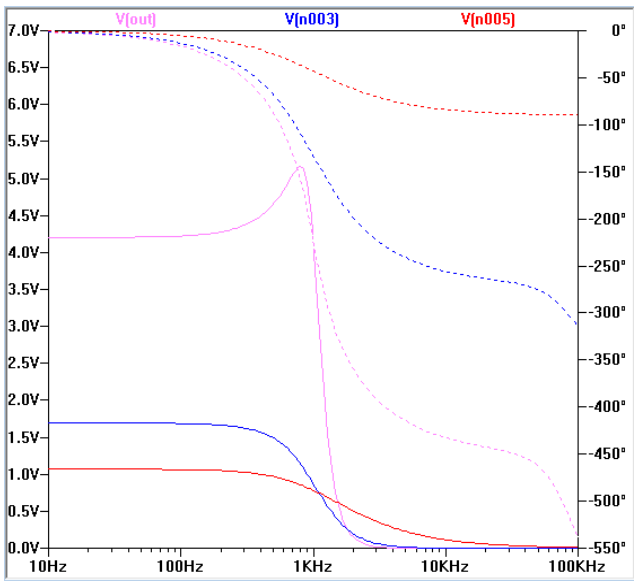


Figure-5. Response of the circuit at each stage if R13 is shorted.

In the similar method all the cases have been simulated. The following are the few simulated results:

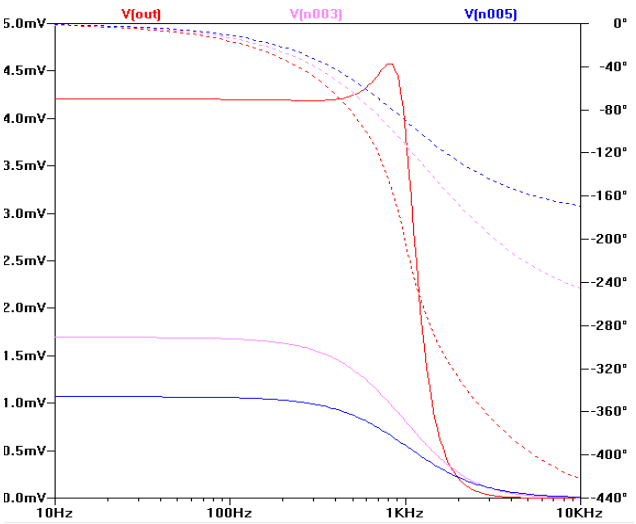


Figure-6. Response of the circuit at each stage if R23 is shorted.

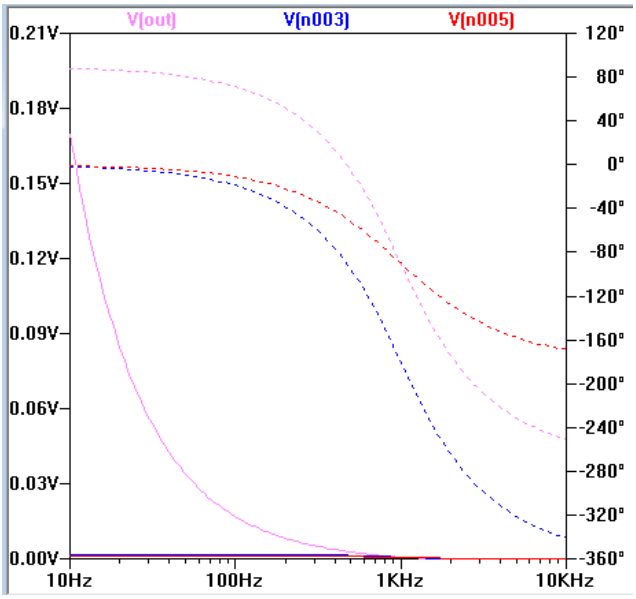


Figure-7. Response of the circuit at each stage if Rf3 is open.

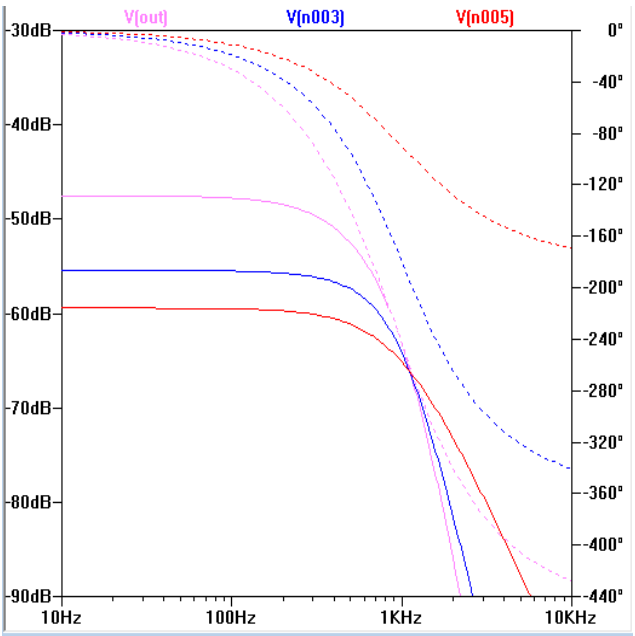


Figure-8. Response of the circuit at each stage if C31 is open.

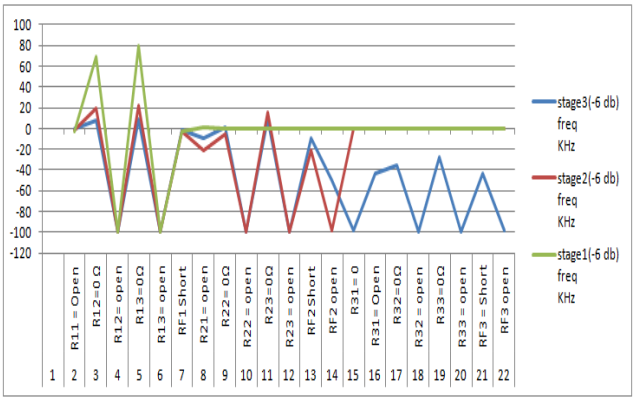


Figure-9. Analysis of each resistor affecting each stage -6dB frequency.

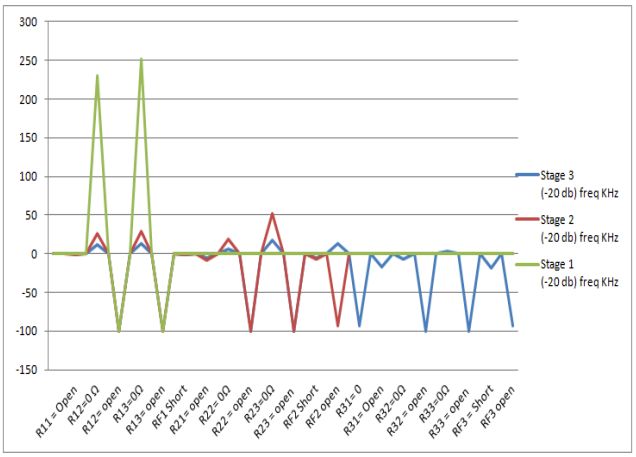
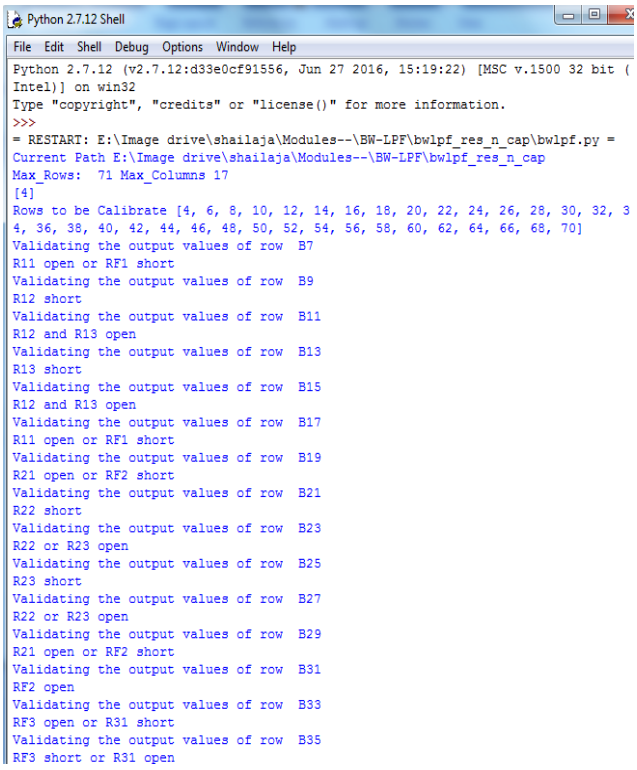


Figure-10. Analysis of each resistor affecting each stage -20dB frequency.



```
Python 2.7.12 Shell
File Edit Shell Debug Options Window Help
Python 2.7.12 (v2.7.12:d33e0cf91556, Jun 27 2016, 15:19:22) [MSC v.1500 32 bit (
Intel)] on win32
Type "copyright", "credits" or "license()" for more information.
>>>
= RESTART: E:\Image drive\shailaja\Modules--\BW-LPF\bwlpf_res_n_cap\bwlpf.py =
Current Path E:\Image drive\shailaja\Modules--\BW-LPF\bwlpf_res_n_cap
Max_Rows:  71 Max_Columns 17
[4]
Rows to be Calibrate [4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 3
4, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70]
Validating the output values of row  B7
R11 open or RF1 short
Validating the output values of row  B9
R12 short
Validating the output values of row  B11
R12 and R13 open
Validating the output values of row  B13
R13 short
Validating the output values of row  B15
R12 and R13 open
Validating the output values of row  B17
R11 open or RF1 short
Validating the output values of row  B19
R21 open or RF2 short
Validating the output values of row  B21
R22 short
Validating the output values of row  B23
R22 or R23 open
Validating the output values of row  B25
R23 short
Validating the output values of row  B27
R22 or R23 open
Validating the output values of row  B29
R21 open or RF2 short
Validating the output values of row  B31
RF2 open
Validating the output values of row  B33
RF3 open or R31 short
Validating the output values of row  B35
RF3 short or R31 open
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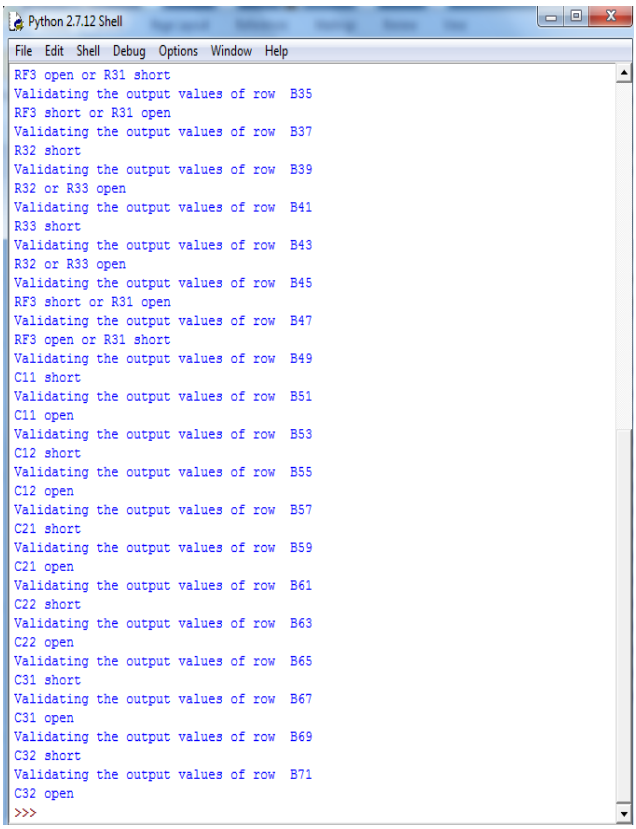

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Python 2.7.12 Shell
File Edit Shell Debug Options Window Help
RF3 open or R31 short
Validating the output values of row  B35
RF3 short or R31 open
Validating the output values of row  B37
R32 short
Validating the output values of row  B39
R32 or R33 open
Validating the output values of row  B41
R33 short
Validating the output values of row  B43
R32 or R33 open
Validating the output values of row  B45
RF3 short or R31 open
Validating the output values of row  B47
RF3 open or R31 short
Validating the output values of row  B49
C11 short
Validating the output values of row  B51
C11 open
Validating the output values of row  B53
C12 short
Validating the output values of row  B55
C12 open
Validating the output values of row  B57
C21 short
Validating the output values of row  B59
C21 open
Validating the output values of row  B61
C22 short
Validating the output values of row  B63
C22 open
Validating the output values of row  B65
C31 short
Validating the output values of row  B67
C31 open
Validating the output values of row  B69
C32 short
Validating the output values of row  B71
C32 open
>>>
```

5. CONCLUSIONS

The Active Butterworth low pass filter has been designed. The fault dictionary has been developed for the filter. The catastrophic fault identification has been done for the circuit by using fault dictionary using hierarchal method.

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