VOL. 13, NO. 9, MAY 2018 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

IMPROVED POWER QUALITY ZETA CONVERTER BASED SMPSFOR PC POWER SUPPLY

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ABSTRACT

The indices of power quality of the Multiple Output Switched Mode Power Supply (MOSMPS) implemented in personal computers are unacceptable by the power quality standards. The Total Harmonic Distortion (THD) of the source current is higher than 75%, the Power Factor (PF) at the input side is lesser than 0.6 and the voltage regulation at the output side is also poor thereby making the performance of the MOSMPS inefficient. The conventional MOSMPS does not meet the IEEE standard of Power Quality (PQ). In this paper, a zeta converter based Power Factor Correction (PFC) is proposed and implemented at the front end to improve the performance of SMPS and the PQ indices. The advantage of the proposed converter is that it mitigates the 100 Hz ripples at the output side of the converter which is fed as an input to the second stage converter. The best performance and efficiency of the proposed zeta converter is determined by analyzing the converter under three different modes of operation. The proposed Neural Network (NN) controlled zeta converter is modeled, designed and simulated using MATLAB Simulink software. The simulation results prove that %THD and PF at the input side meet the IEEE standard of power quality under fluctuating conditions.

Keywords: PQ, switched mode power supply, THD, PF.

1. INTRODUCTION

In the recent era, the personal computer (PC) plays an important role in many sectors like education, IT, business etc. The PC requires multiple DC output voltage levels from single ac source for the operation of various components like i) mouse, ii) keyboard, iii) CD driver and iv) display etc. The requirement of the PC power supply is accomplished by a SMPS. A Diode Bridge Rectifier (DBR), capacitor and dc-dc converter constitutes a SMPS. The input current of the MOSMPS has high %THD and crest factor due to the uncontrolled operation of capacitor under charging and discharging conditions. Due to this reason, the MOSMPS does not meet the IEEE standard for PQ [1-3]. In IT sectors more number of PCs are used, which increases the current in the neutral conductor and introduces noise and voltage distortion, due to which the performance of the transformer is derated [4-5].

To mitigate all the PQ problems related with MOSMPS, many research works are carried out to design and model an improved SMPS system. The improved MOSMPS maintains PF nearly unity, draws sinusoidal ac current from input mains and has tight output voltage regulation under varying load and source conditions. Single stage and two stage PFC converters are normally employed for PCs. The performance of single stage converter is exceptional, but a large value of capacitor is needed to filter out the ripple content. This limits the rating of the single stage converter to 220W. Two stage PFC converters are normally preferred in medium rating applications. The PQ indices at the PCC are improved by first stage and the output voltage regulation is taken care of by second stage [1-3] Two modes of operations are possible in the front end converter i) Discontinuous Conduction Mode (DCM) and ii) Continuous Conduction Mode (CCM). The DCM is preferred when the cost is considered as the key factor, since it requires only one sensor to sense the voltage and control it. For the operation of CCM, two sensors are needed for voltage sensing and one sensor for current measurement. This in turn increases the cost of the overall system, but the voltage stress in the device is reduced. In many industrial applications, boost converter is preferred for PFC, but the limitation is that it cannot operate for a wide variation in input voltage. Similarly, the buck converter cannot be employed when the variation in the output voltage is over a wide range. The drawbacks of the buck and boost (BB) converters are overcome by the non-isolated buck-boost PFC converters. In spite of less number of components, the conventional BB converter has more ripple content in the output voltage due to the pulsating output current. The BB cuk converter has various design limitations due to the reversed polarity of the output voltage. SEPIC converter also exhibits pulsating output current. The flyback converter has limitation on its rating due to leakage inductance [1],[3],[6-7]. The drawbacks of the above mentioned converters are overcome by Zeta converter and thus it is preferred in many industrial applications.

This paper deals with a NN controlled MOSMPS, that has improved PQ indices and tight output voltage regulation under wide variation of line and load parameters. A Zeta PFC converter with a NN controller is considered as MOSMPS, which satisfies the major requirement of all the SMPS applications. It draws sinusoidal input current from the input mains with unity PF and also has low ripple content on the output voltage. The Zeta PFC converter is analyzed for three different modes of operation. Based on the results, the best operating mode is selected and preferred for the PC application. The proposed NN controlled zeta converter is modeled, designed and simulated using MATLAB Simulink software. The simulation results prove that %THD, PF of the source and output voltage regulation

meet the IEEE standard of power quality under fluctuating conditions.

2. MOSMPS EMPLOYING ZETA CONVERTER

2.1 Operation and design of zeta PFC converter

Figure-1 depicts the proposed MOSMPS with PFC zeta converter at the front end and isolated half bridge converter for multiple isolated output voltages.

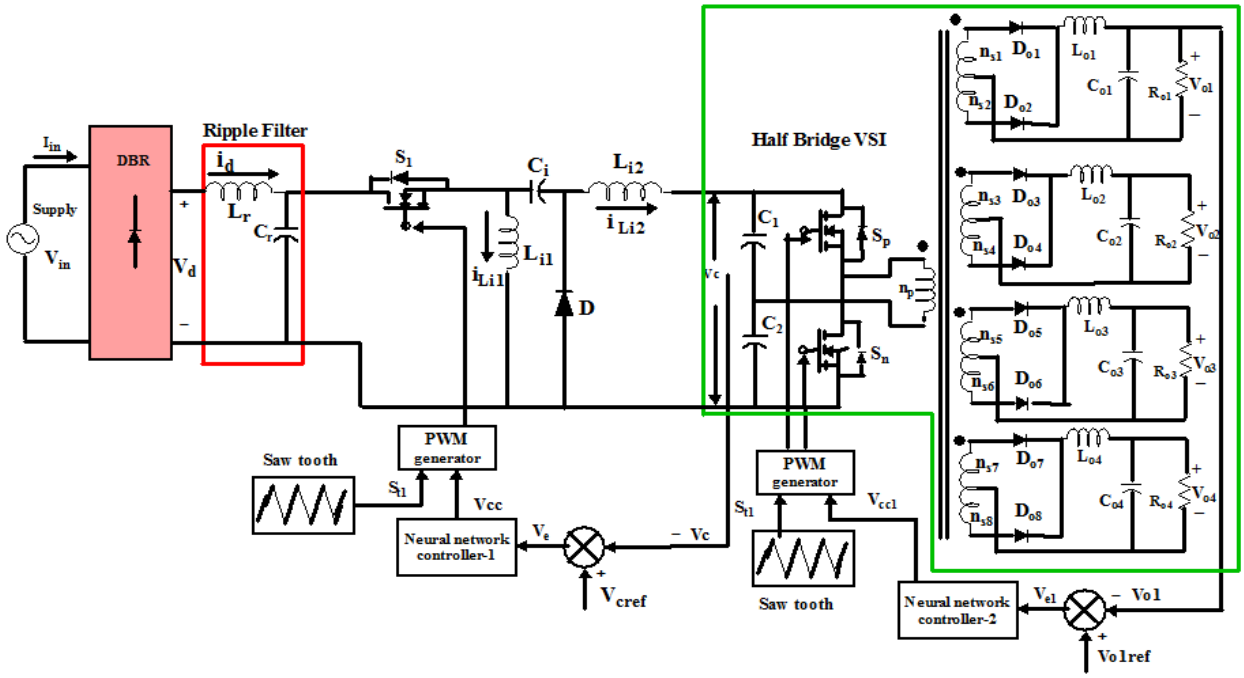

Figure-1. Circuit configuration of MOSMPS employing zeta PFC converter.

The PFC unit consists of a capacitor C_i, inductors L_{i1} and L_{i2}, diode D and switch S_1 that operates at high frequency. The main functions of the PFC unit are i) regulation of intermediate voltage V_c and ii) maintenance of PF to nearly unity by drawing sinusoidal current from the input side. The performance of the PFC unit at the front end is analysed based on the following three different DCM operating conditions: i) output inductor L_{i2} in DCM ii) inductor L_{i1} in DCM and iii) intermediate capacitor C_i in DCM. The regulated DC output voltage of the PFC converter is applied to an isolated half bridge converter that generates multiple output DC voltages at the output side.

The PFC zeta converter is analysed and studied for one switching cycle. The operation of the converter is analysed for three different DCM conditions in order to identify the best operating condition.

i) Operation of PFC converter under DCM of input inductor

Under this mode of operation, the values of intermediate capacitor voltage and output inductor current are non-zero, whereas the value of the inductor L_{i1} current is maintained at zero for a specific time during a switching cycle.

Mode I: When the switch S_1 in the PFC converter is turned on, the magnitude of the capacitor voltage is decreased and the current in the output inductor L_{i2} and input inductor L_{i1} begin to increase.

Mode II: The conduction of diode D is initiated, by switching off switch S_1 in the PFC circuit. Under this condition, the energy stored in the inductor L_{i1} begins to decrease. The dissipation of energy continues until the magnitude of the current in the two inductors L_{i1} and L_{i2} are equal. The voltage of intermediate capacitor C_i begins to increase.

Mode III: In this mode, diode D and switch S_1 are in off condition for the remaining period of the switching cycle. This mode prevails until the next switching cycle is initiated. DCM is ensured by maintaining the input inductor current as zero.

ii) Operation of PFC converter under DCM of intermediate capacitor

Mode I: When switch S_1 in the PFC converter is turned on, the output inductor L_{i2} provides the path for the intermediate capacitor to discharge. As a result, the voltage across it is decreased. At the same time, the voltage across output capacitors (C_1 and C_2) and the current in output inductor L_{i2} and input inductor L_{i1} start to increase.

Mode II: The switching device S_1 remains in on state during this mode of operation. The discharging action of the intermediate capacitor C_i continues until the capacitor is fully discharged and the voltage across the capacitor becomes zero. The energy stored in the output inductor L_{i2} is fed to the output capacitor.

Mode III: In this mode switching device S_1 is in off condition. The output inductor L_{i2} and input inductor L_{i1} discharge through the isolated converter and intermediate capacitor respectively. Thus, a continuous conduction is maintained.

iii) Operation of PFC converter under DCM of output inductor

Mode I: When the switch S_1 in the PFC circuit is turned on, the input inductor L_{i1} stores energy from input supply. The current in the output inductor L_{i2} starts to increase due to the discharging action of the intermediate capacitor. The output and input inductor currents vary linearly.

Mode II: Conduction in the diode D is initiated, by turning off switch S_1 in the PFC circuit. Under this condition, the energy stored in inductor L_{i1} starts to decrease. The dissipation of energy continues until the magnitude of the current in the two inductors L_{i1} and L_{i2} are equal. The voltage of intermediate capacitor C_1 starts to increase.

Mode III: In this mode, diode D and the switching device S_1 are in off condition for the remaining period of the switching cycle. This mode prevails until the next switching cycle is initiated. DCM is ensured by maintaining the output inductor current at a value of zero.
The variation of the inductor current during on and off states of the switch is a key consideration in the design of SMPS. Equation (1) establishes the relation between the input voltage V_d and output voltage $V_c$in a zeta converter with duty ratio D

$$\frac{V_c}{V_{in}(t)} = \frac{D}{1-D} \quad (1)$$

The instantaneous value of duty ratio is given by equation (2)

$$D(t) = \frac{V_c}{V_{in}(t)+V_c} \quad (2)$$

a) Selection of input inductor

$$L_{i1\,DCM} = \frac{D(t)T_sV_{in}(t)}{2I_{in}} = \frac{D(t)T_sR}{2} = \frac{D(t)T_sV_d^2}{2P_{in}} = \frac{T_sV_d^2}{2P_{in}}\left[\frac{V_c}{V_{in}(t)+V_c}\right] \quad (3)$$

where,

T_s = switching time = 50 µs

V_d = average voltage at the output of DBR = $\frac{2*\sqrt{2}*170}{\pi}$ = 153.1 V
V_c = output voltage of zeta converter = 300 V
V_{in} = input voltage of zeta converter = 1.414 x 170 = 240.38 V
P_{in} = input power = 175 W

The design of the inductor considers worst supply voltage conditions with an RMS value of 170 V. By substituting this value in equation (3), the inductor value is calculated as 1.85 mH. The value of the input inductor is chosen as 1.5 mH in order to operate under DCM under all varying conditions.

For the inductor to operate under CCM, the inductor value is calculated as 4.6 mH using equation (4)

$$L_{i1\,CCM} = \frac{D(t)T_sV_{in}(t)}{\Delta I_{in(t)}} = \frac{T_sV_{in}(t)}{\Delta I_{in(t)}}\left[\frac{V_c}{V_{in}(t)+V_c}\right] \quad (4)$$

b) Selection of output inductor

$$L_{i2\,DCM} = \frac{(1-D(t))T_sV_c}{2I_{dc}(t)} = \frac{V_cD(t)T_s}{2I_{in}(t)} = \frac{RV_cD(t)T_s}{2V_{in}(t)} = \frac{V_d^2\,T_sV_c}{2V_{in}(t)P_{in}}\left[\frac{V_c}{V_{in}(t)+V_c}\right] \quad (5)$$

When the supply voltage is minimum and the power is maximum, ripples in the inductor current are maximum. A minimum supply voltage condition of 170 V is considered. Substituting this value in equation (4), the inductor value is calculated as 2.3 mH. The output inductor value is chosen as 2 mH to operate under DCM for all varying conditions. For the inductor to operate under CCM, its value is calculated as 6 mH using equation (6)

$$L_{i2\,CCM} = \frac{(1-D(t))T_sV_c}{\Delta I_0} = \frac{V_cD(t)T_s}{\Delta I_{in}(t)} = \frac{T_sV_c}{\Delta I_{in}(t)}\left[\frac{V_c}{V_{in}(t)+V_c}\right] \quad (6)$$

c) Selection of intermediate capacitor

Equation (7) stated below is used to calculate the intermediate capacitor value.

$$C_{iDCM} = \frac{D(t)T_sV_c}{2V_{c1}R} = \frac{T_sV_c}{2\{V_c+V_{in}(t)\}\left(V_c^2/P_{in}\right)}\left[\frac{V_c}{V_{in}(t)+V_c}\right] = \frac{T_sP_{in}}{2(V_c+V_{in}(t))^2} \quad (7)$$

Substituting the values in equation (7), the capacitor value is calculated as 9.41 nF. A value of 7 nF is chosen to operate under DCM for all varying conditions. For the capacitor to operate under CCM, its value is calculated as 0.0628 µF using equation (8)

$$C_{iCCM} = \frac{D(t)T_sV_c}{2\Delta V_{c1}R} = \frac{T_sV_c}{2\{\Delta(V_c+V_{in}(t))\}\left(V_c^2/P_{in}\right)}\left[\frac{V_c}{V_{in}(t)+V_c}\right] = \frac{T_sP_{in}}{2\{\Delta(V_{in}(t)+V_c)\}(V_{in}(t)+V_c)} \quad (8)$$

2.2 Operation and design of Half Bridge Converter (HBC)

The regulated output voltage of the first stage forms the supply for the HBC. Multiple output voltages are provided by a High Frequency Transformer (HFT) with centre tapped secondary windings. The inductors (L_{o1} - L_{o4}) and capacitors (C_{o1} - C_{o4}) are utilized for filtering current and voltage ripples. The output voltage regulation is achieved using a ANN controller-2. The highest rated secondary winding voltage is sensed for voltage control and the duty cycle is altered to control all other output voltages.

Each switching cycle comprises of four operating stages. In the first stage the HFT primary winding is energized by turning ON S_p. The inductors (L_{o1} - L_{o4}) store energy with the help of forward biased diodes D_{01}, D_{03}, D_{05} and D_{07}. In this stage the load is fed from the capacitors (C_{o1} - C_{o4}) and the inductor current increases to reach the maximum value.

Stage II and IV form the freewheeling period during which (L_{o1} - L_{o4}) dissipate the stored energy through the diodes ($D_{01} – D_{08}$).

In the third stage the primary winding of the HFT is energised through C_1 by turning ON S_n. Inductors (L_{o1} - L_{o4}) store energy with the help of forward biased diodes D_{o2}, D_{o4}, D_{o6} and D_{o8}. The switch S_n is turned OFF when the inductor current attains the maximum value.

a) Selection of capacitor

In HBC, the value of the capacitor is chosen in such a way that they eliminate the 100 Hz ripple that is reflected from the AC input side. The power factor at the input side should be nearly unity. The input power drawn from the single-phase AC source is calculated using equation (9).

$$P_{in}=V_m\sin\omega t * I_m\sin\omega t = V_{in}I_{in}(1-\cos2\omega t) \quad (9)$$

The term cos2ωt represents the reflected 100 Hz ripple. If V_c is the capacitor voltage then the charging current $i_c(t)$ flowing in the input capacitors of half bridge Voltage Source Inverter (VSI) is calculated as

$$i_c(t) = -\frac{V_{in}I_{in}}{V_c}\cos2\omega t \quad (10)$$

The output voltage ripple (ΔV_c) across the capacitors C_1 and C_2 are calculated using equation (11)

$$\Delta V_c = \frac{1}{c}\int i_c(t)dt = \frac{I_0}{2\omega C}\sin2\omega t \quad (11)$$

As per the equation (11), the maximum voltage ripple across the capacitors appear when sin2ωt value is 1. Thus, the equation becomes

$$C = \frac{I_0}{2\omega\Delta V_c} \quad (12)$$

The 100 Hz ripples present in the input side of the half bridge VSI can be eliminated by calculating the capacitor value using the equation (12)

$$2C_1 = 2C_2 = \frac{I_0}{2\omega\Delta V_c}$$

Considering ω = 314 rad/sec, $\Delta V_c = 6$ V(2%) and$I_0 = 0.58$ A, the value of $C_1 = C_2 = 0.310$ mF. As the proposed converter is designed primarily for computer power supply applications, the capacitor value should be in such a way that the SMPS can withstand power failure at least for some time. The with-stand time is calculated as

$$T_{with-stand} = (V_{cm}^2 - V_{cmin}^2)\frac{C_{12}}{2P_0}$$

$$C_{12} = \frac{(T_{with-stand})(2P_0)}{(V_{cm}^2 - V_{cmin}^2)} \quad (13)$$

where,

$T_{with-stand}$ = with-stand time of capacitor during power failure = 10 ms

V_{cm} =minimum output DC voltage of the PFC converter = 294 V

V_{cmin} = minimum voltage at which the output is held regulated = 260 V

P_o = output power = 175 W

In order to have a 10 ms with-stand time, the capacitor value is calculated using equation (13) as C_{12} = 0.18 mF. As the input capacitors of the half bridge VSI are connected in series, the value of $C_1 = C_2 = 0.36$ mF.

b) Selection of inductor

The value of inductance at the secondary side of the HFT is calculated using equation (14).

$$L_{01} = \frac{V_{01}(0.5- D)}{f_s\Delta i_{Lo1}} \quad (14)$$

where,

ΔiL_{01} = output current ripple

By considering D = 0.4, f_s = 60 kHz and Δi_{L01} = 2% of 6A, the inductor value (L_{01}) is calculated as 0.12 mH. The value of inductors L_{02}, L_{03} and L_{04} in the secondary windings of the HFT are calculated using equation (14) as L_{02} = 0.023 mH, L_{03} = 1.3 mH and L_{04} = 1.25 mH.

c) Selection of turns ratio

In steady state, the current variation in the output inductor (i_{Lo1}) during the switching condition is equated to zero as shown below:

$$\frac{T_h(0.5nV_c\text{-}V_{01})D_h}{L_{01}} + \frac{T_h(0.5\text{-}D_h)V_{01}}{L_{01}} = 0 \quad (15)$$

where,
V_{01} = highest rated output voltage of +12 V
T_h = switching time of half bridge VSI
D_h = duty ratio of half bridge VSI = 0.4

The turns ratios are calculated by solving equation (15). They are calculated as n_1= 0.1, n_2 = 0.042, n_3 = 0.042 and n_4 = 0.1 for the secondary windings with voltage ratings V_{01} = 12 V, V_{02} = 5 V, V_{03}= -5 V and V_{04} = -12 V, respectively.

3. PROPOSED NEURAL NETWORK CONTROLLER

The output voltage of the front end converter and isolated converter are controlled by two different NN controllers [8-12]. NN based voltage follower and average current control techniques are implemented for front end and isolated converters.

3.1 NN Based voltage control for front end converter

The controller NN1 senses the output voltage of the converter and it is compared with the reference voltage. Based on the error, the pulse generator produce pulses for switching ON and OFF the switch S. The nth instant value of the voltage error signal (Ve) can be expressed as:

$$V_e(n) = V_{dcref}(n) - V_{dc}(n) \quad (16)$$

The error signal (Ve) is given as input to the NN controller 1 which produces the output voltage (V_{c0}) whereas in Conventional Controller (CC), PI controller is implemented instead of NN controller. The gate pulses for controlling the switching action of the switch are generated, by comparing the output voltage (V_{c0}) and a high frequency saw tooth waveform (S_{t1}). The switch is in ON state when $S_{t1} < V_{c0}$ and is in OFF condition when $S_{t1} > V_{c0}$. For any deviation in the output voltage the error voltage (V_{c0}) changes accordingly to modify the duty cycle.

3.2 NN based control for isolated converter

NN based average current control method is implemented for the control of multiple dc output voltages. The winding with highest voltage rating is controlled. Since all the secondary windings are wound on a common core, the output voltages of the other windings are controlled by the duty cycle of the converter. The NN controller 2 senses the output voltage (V_{01}) and it is compared with the reference voltage. The error signal (V_{e1}) is given as input to the NN controller 2 which produces the output voltage error, whereas in CC, PI controller is implemented instead of NN controller. The gate pulses for controlling the switching action of the switches S_1 and S_2 are generated, by comparing the output voltage V_{cc1} and a high frequency saw tooth waveform. The switches S_1 and S_2 are switched alternatively for every half cycle with proper delay in order to avoid short circuit. Based on the error in the output voltage the width of the pulses will be varied to maintain the output voltage constant. The controller maintains tight output voltage regulation in all other secondary windings by varying the duty cycle even when there is a load change in other secondary windings.

4. ANALYSIS OF SIMULATION RESULTS

The proposed zeta converter with ANN controller is modelled as per data given in Table-1 and simulated in MATLAB. The performance in terms of %THD of I_{in}, input PF, DF, DPF and ripple factor of the NN based converter is evaluated under fluctuating conditions such as i) V_{in}=220V rms), ii) V_{in}=170V and iii) V_{in}=250V and iv) with load variation under rated supply voltage. To highlight the performance of the converter with ANN controller it is compared with that of converter with CC.

Table-1. Parameters for MOSMPS.

S. No.	Parameters	Values
1.	Supply voltage	170-270 V rms
2.	Switching frequency	50 kHz
3.	Output voltage V_{01}	12 V/6 A
4.	Output voltage V_{02}	5 V/18 A
5.	Output voltage V_{03}	-5 V/0.3 A
6.	Output voltage V_{04}	-12 V/0.8 A
7.	Output power P_0	W

4.1Performance under V_{in} = 220V

Figure-2 shows the waveform of regulated multiple output voltages, supply voltage and current at V_{in}= 220 V and output currents. From the output voltage waveforms it is evident that V_{o1} to V_{o4} are well regulated by the NN controller. The source voltage and current waveforms depicts that current drawn from the supply is sinusoidal in shape and is in phase with Vin, thereby maintaining the power factor close to unity. As indicated in Table-2 the values of DF, DPF and PF are 0.994, 1 and 0.994 respectively. The THD of the supply current is maintained at 3.6%, which is within the limit suggested by the IEC 61000-3-2 standard. Performance of the NN controlled zeta converter is also analysed with conventional controller and the results are tabulated in Tables 2 and 3. With conventional control, the THD of the source current is reduced to 5.8% and PF at the supply side is maintained at 0.88.

4.2 Performance under increased supply voltage condition V_{in}= 250V

Figure-3 shows the waveform of regulated multiple output voltages, supply voltage and current at V_{in}= 250 V and output currents. From the output voltage waveforms it is evident that V_{o1} to V_{o4} are well regulated

by the NN controller. The source voltage and current waveforms depicts that current drawn from the supply is sinusoidal in shape and is in phase with Vin, thereby maintaining the power factor close to unity. As indicated in Table-2 the values of DF, DPF and PF are 0.992, 1 and 0.992 respectively. The THD of the supply current is maintained at 3.98%, which is below the limit suggested by IEC 61000-3-2 standard. Performance of the PFC zeta converter is also analysed with conventional controller and the results are tabulated in Tables 2 and 3. With conventional control, the THD of the source current is 6.2% and PF at the supply side is maintained at 0.87.

4.3 Performance under decreased supply voltage condition V_{in}=170 V

Figure-4 shows the waveform of regulated multiple output voltages, supply voltage and current at V_{in}= 170 V and output currents. From the output voltage waveforms it is evident that V_{o1} to V_{o4} are well regulated by the NN controller. The source voltage and current waveforms depicts that current drawn from the supply is sinusoidal in shape and is in phase with Vin, thereby maintaining the power factor close to unity. As indicated in Table-2 the values of DF, DPF and PF are 0.996, 1 and 0.996 respectively. The THD of the supply current is maintained at 2.85%, which is within the limit suggested by the standard IEC 61000-3-2. Performance of the NN controlled zeta converter is also analysed with conventional controller and the results are tabulated in Tables 2 and 3. With conventional control, the THD of the source current is 5.1% and PF at the supply side is maintained at 0.94.

4.4 Performance under rated supply voltage with load variation

Figure-5 shows the waveform of regulated multiple output voltages, output currents, supply voltage and current at V_{in}= 220 V and load variation at V_{o2}. From the output voltage waveforms it is evident that V_{o1} to V_{o4} are well regulated by the NN controller even under load variation at terminal 2 from 50% to 100% at 0.5 s. The load variation at terminal 2 from 50% to 100% at 0.5 s is clearly depicted in the output current waveform. From the source voltage and current waveforms, it is evident that supply current drawn from the utility is sinusoidal and in phase with the supply voltage, thereby maintaining the PF nearly unity. When the load at terminal 2 is 50% the values of DF, DPF and PF are 0.980, 1 and 0.980, respectively.

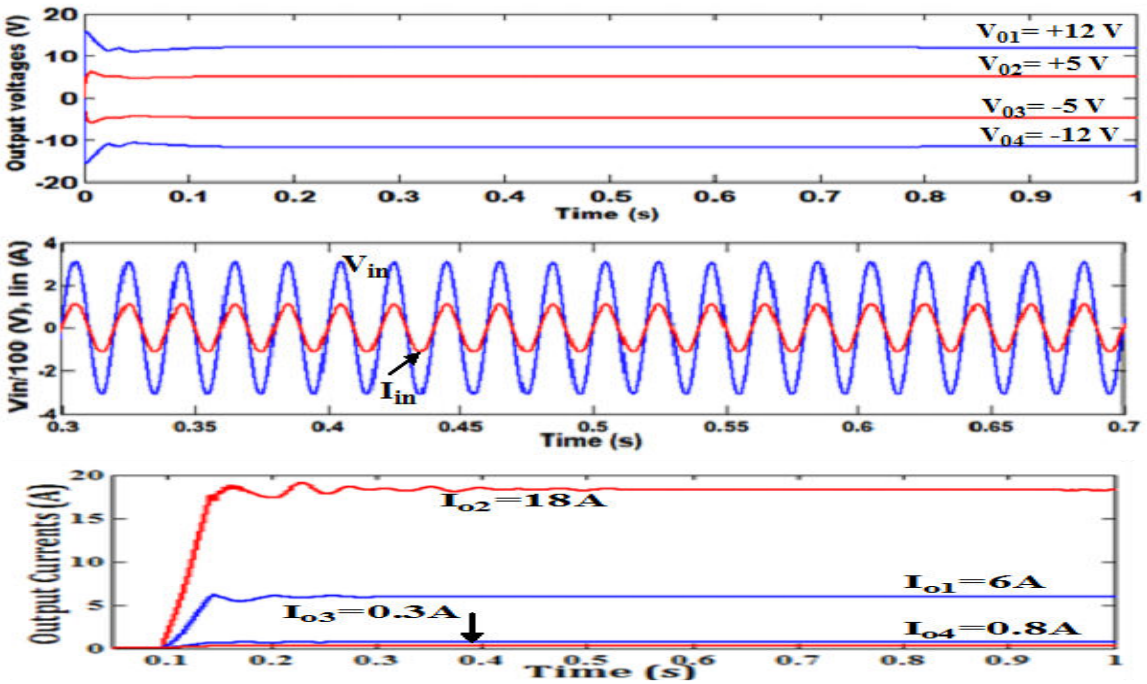

Figure-2. Waveforms of NN controlled zeta converter with V_{in} = 220 V. (a) Output voltages (V), (b) V_{in}/100 (V) and I_{in} (A) and (c) Output currents (A).

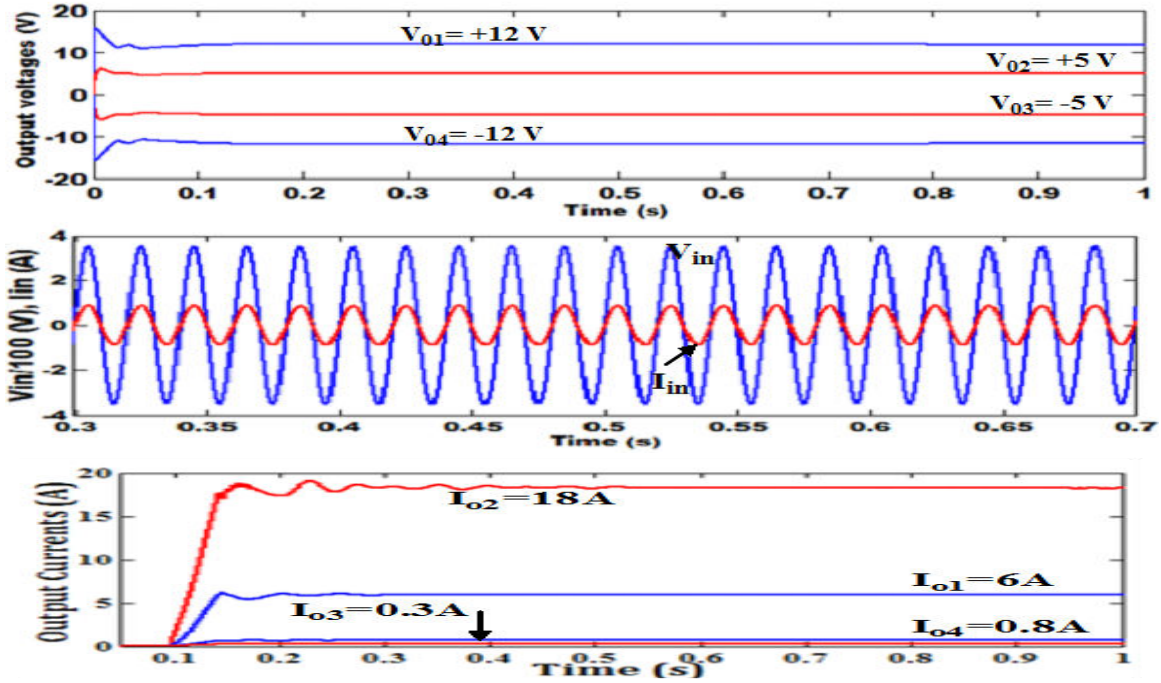

Figure-3. Waveforms of NN controlled zeta converter with V_{in} = 250 V. (a) Output voltages (V), (b) V_{in}/100 (V) and I_{in} (A) and (c) Output currents (A).

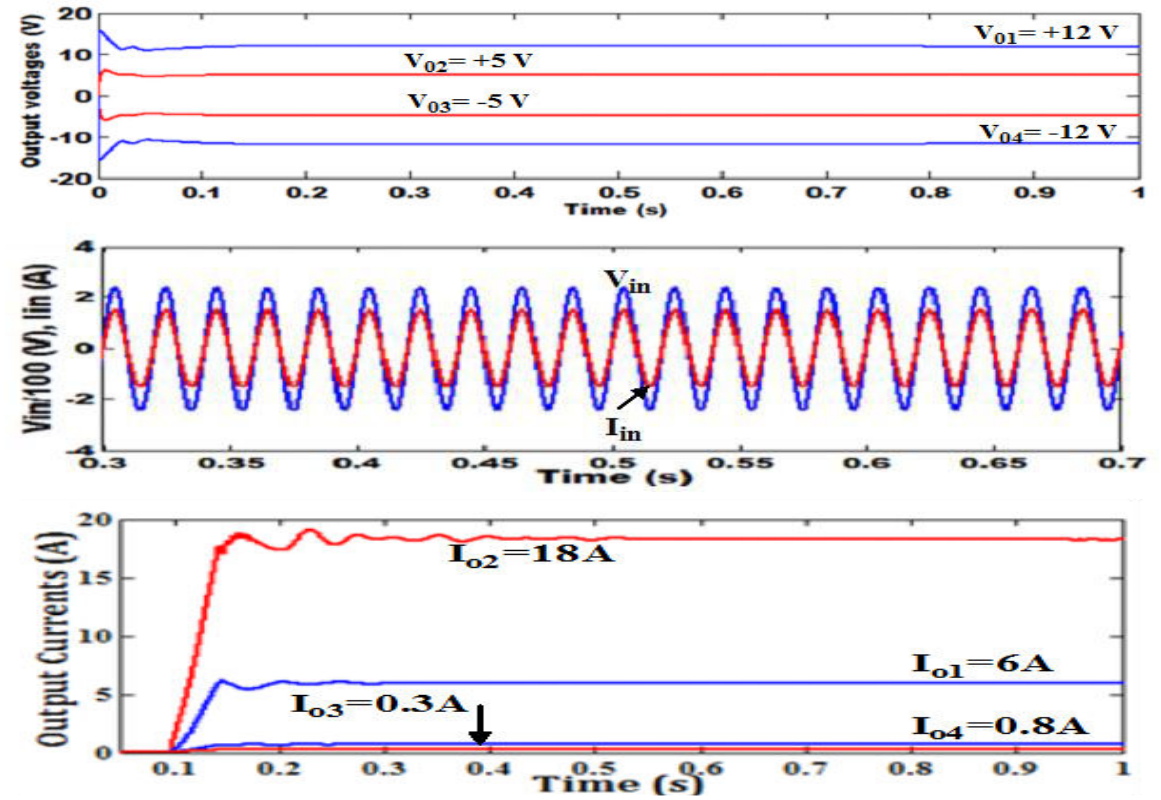

Figure-4. Waveforms of NN controlled zeta converter with V_{in} = 170 V. (a) Output voltages (V), (b) V_{in}/100 (V) and I_{in} (A) and (c) Output currents (A).

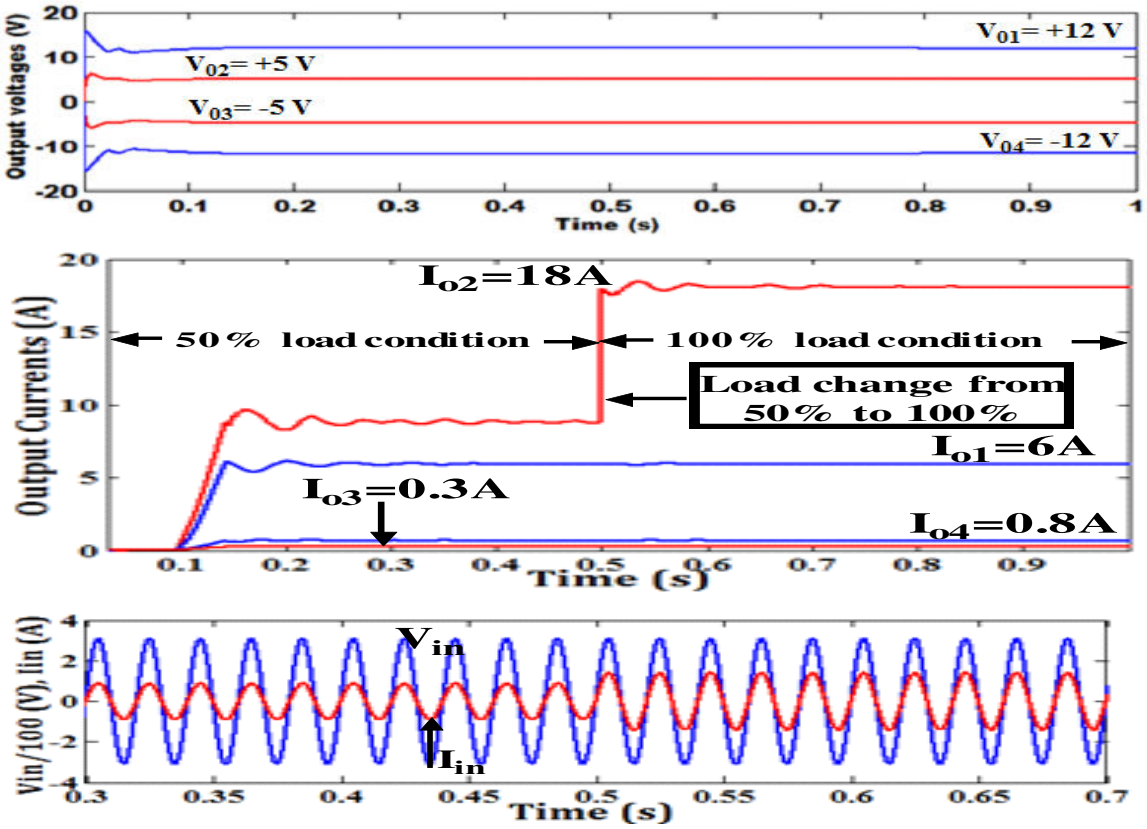

Figure-5. Waveforms of NN controlled zeta converter with V_{in} = 220 V and load variation at V_{o2}. (a) Output voltages (V), (b) Output currents (A) and (c) V_{in}/100 (V) and I_{in}(A).

The THD of the supply current is maintained at 4.5%, which is within the limits suggested by the IEC 61000-3-2 standard. Performance of the PFC zeta converter based SMPS is also analysed with conventional controller and the results are tabulated in Tables 2 and 3. With conventional control, the THD of the source current is reduced to 6.2% and PF at the supply side is maintained at 0.85. It is inferred that PFC zeta converter based SMPS with NN controller takes 0.21 s to attain steady state and the % overshoot of V_{o1} is 2.52 during transient response.

Performance comparison tabulated in Tables 2 and 3, Comparison chart shown in Figures 6, 7 and 8 highlight the superior performance of NN controller over conventional controller. Figure-6 shows the comparison of % THD of source current which infers that the THD achieved with proposed controller is lesser than that achieved with conventional controller under fluctuating conditions. Figure-7 shows the comparison ofinput PF. When compared to CC, the proposed NN control performs better in maintaining the PF close to unity.

Table-2. Parameter values of MOSMPS at different supply voltage conditions.

Supply voltage (V)	DF	DPF	PF		% THDof I_{in}		Output voltage ripple1*				Output voltage ripple2*			
			1*	2*	1*	2*	V_{01} (%)	V_{02} (%)	V_{03} (%)	V_{04} (%)	V_{01} (%)	V_{02} (%)	V_{03} (%)	V_{04} (%)
Performance at 100% load														
170	0.996	1	0.996	0.94	2.85	5.1	1.8	2.3	2.6	2.4	2.6	2.9	3.2	3.7
220	0.994	1	0.994	0.88	3.6	5.8								
250	0.992	1	0.992	0.87	3.98	6.2								
Performance at 50% load														
220	0.980	1	0.980	0.85	4.5	6.2	1.9	2.5	2.6	2.4	2.7	3.0	3.2	3.8

Table-3. Parameter values of MOSMPS at different supply voltage conditions.

Settlingtime (s)		**Transient response of V_{o1} with NN control**		**Transient response of V_{o1} with conventional control**	
NN control	Conventional control	Overshoot (%)	Undershoot (%)	Overshoot (%)	Undershoot (%)
0.21	0.28	2.52	2.6	4.00	4.21

1*- NN controller, 2*- Conventional controller

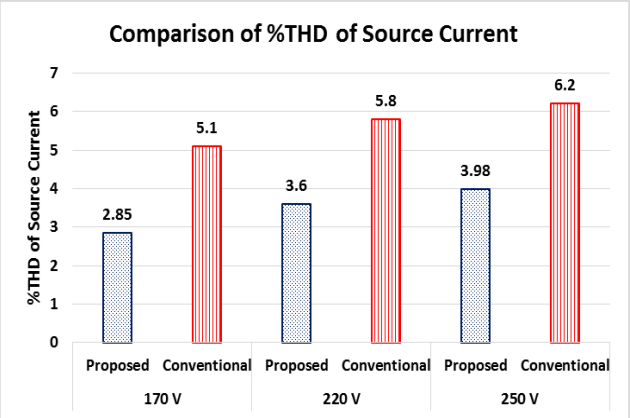

Figure-6. Comparison of THD of source current.

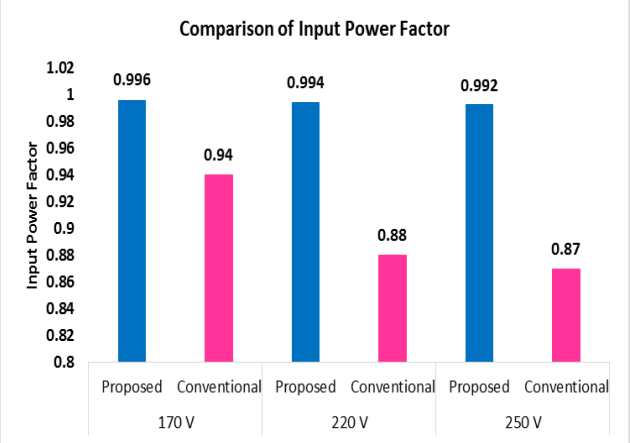

Figure-7. Comparison of input PF.

Figure-8 gives the comparison of % overshoot and undershoot of V_{01} at V_{in}=220 V. The performance of NN controlled MOSMPS is superior when compared to MOSMPS with conventional controller in terms of THD, input PF, settling time, output voltage ripple, overshoot and undershoot.

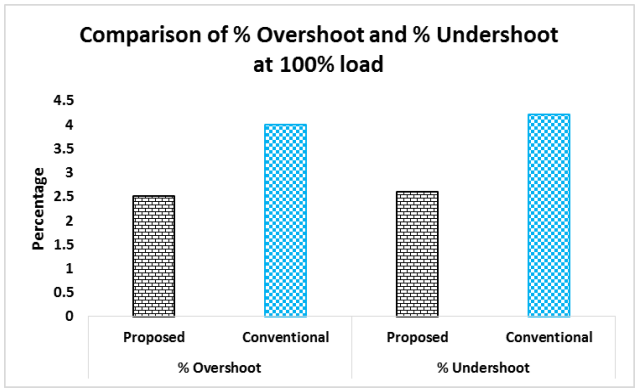

Figure-8. Comparison of % overshoot and undershoot of V_{01} at V_{in}=220 V.

5. CONCLUSIONS

A zeta converter based PFC circuit is implemented at the front end of 175 W MOSMPS to improve the performance and PQ indices. The proposed neural network controlled zeta converter based MOSMPS is modeled, designed and simulated using MATLAB Simulink software. The performance of the MOSMPS is also analysed with CC in terms of THD of I_{in}, input power factor, output voltage ripple, overshoot, undershoot and settling time. Simulation results and tabulated performance prove that NN controller performs better when compared to CC under fluctuating conditions. As the %THD and PF at the input side meet the IEEE standard of power quality, the proposed MOSMPS is best suited for PC power supply application.

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