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DESIGN AND PERFORMANCE ANALYSIS OF LOW POWER SRAM USING MODIFIED MTCMOS

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ABSTRACT

Present day mobile communication devices equipped with large capacity memories in order to fulfil all the multimedia needs of customers. Now a days, design engineer mainly concentrating not only to equip high capacity memories, but also high bandwidth and low power consuming memories. This paper presents a low power structure for an SRAM cell by modifying the Multi-threshold CMOS architecture. Multi-threshold CMOS architecture is a technique in which transistors with different threshold voltages are used to reduce power consumption and also to reduce delay. This paper presents a more interesting method to reduce power consumption by reducing leakage current in idle condition. This method depicts how the voltage, temperature and transistor size effecting the power consumption in an SRAM cell. This paper presents a novel architecture for SRAM cell to reduce power consumption in the memory structure. SRAM cell is designed with 45 nm technology and is compared with standard 6T SRAM structure. Simulation results shows that power consumption reduced to around 21% when compared with standard 6T SRAM structures.

Keywords: complementary metal oxide semiconductor, low power, leakage power, multi-threshold CMOS, static random access memory.

INTRODUCTION

Moore predicted that the number of transistors that can be integrated on a single chip can be doubled for every one and half years (Moore, 1995). VLSI (Very Large Scale Integration) industry success can be measured by the scaling of transistors (AI-Mutairi *et al*., 2015). Smaller and smaller transistors manufactured, fulfils the Moore prediction. Scaling of transistor size not only reduces channel length but also the supply voltage. Now we are in the era of saturation of all the transistor parameters scaling. It is very difficult to scale further. There may be possibility of altering the system behaviour. There may be induced EMF when two power rails passing very near. These effects need to be addressed while scaling integrated circuits.

With the increasing demand of portable digital systems, VLSI industry much concentrating on the low power consuming devices (Devadas *et al*., 1995). This is because of the need of portable device is increased enormously. It is difficult for charging portable device frequently. They should be equipped with large capacity batteries in order to avoid frequent charging. Large battery packs carrying on portable device is difficult again and also expensive (Mutoh *et al.*, 1995). Some of the new battery techniques like lithium nickel batteries, Nickel metal hydride able to meet the energy requirements in portable devices. But the size and weight must be further lowered to make the portable device must simple. In order to overcome these difficulties, design engineers proposed many low power design techniques. Low power circuit design is a basic requirement in portable device (Ko *et al*., 1995) (Benini *et al*., 2000).

Memories used in portable device are main sinks for battery power (Rani *et al*., 2012). Compared with normal functional mode power consumption during read and write cycles is more. In order to reduce power consumption while accessing memories low power memory structure proposed in this paper. In the field of low power system design one of the most important factor need to be considered is circuit reliability. As the circuits working with very small supply voltages and small transistor lengths and narrow wirings and tiny vias, the probability of malfunctioning is very high (Leung *et al*., 2002). Keeping this in mind the design engineers give a proper solution to address the high power needs in the portable devices.

As technology is changing year by year the VLSI device parameters are scaling accordingly. VLSI device parameter scaling is in turn responsible for exponential growth of power consumption. Not only in portable device, but also in many complex systems low power VLSI system design is the primary requirement. Power dissipation in VLSI circuits is of two components namely Static power and Dynamic power. Static Power Ps can be obtained by the product of supply voltage and leakage current,

$$P_s = V_{dd} * I_{Leakage} \quad (1)$$

And the dynamic power can be expressed as,

$$P_d = \alpha C_l V_{dd}^2 f \quad (2)$$

Where Vdd is the supply voltage, ILeakage is the leakage current, α is the switching activity factor, CL is load capacitance and f is the operating frequency. Up to now VLSI design engineers mainly concentrated on the dynamic power, which is responsible for maximum portion of the system power. Now the static power is also playing predominant role in system total power. Static power is nothing but the product between system voltage source and the leakage power. So the leakage power reduction is a main solution to reduce static power. In this

paper MTCMOS based SRAM structure is modified to reduce leakage power there by reducing overall power consumption.

LOW POWER MEMORY DESIGN REQUIREMENT

Memory requirement in present day embedded systems is greatly increased due to increase in multimedia data transfer raise. This scenario is mainly because of the 4G and 5G technology developments. According to the need of 4G and 5G technology requirements, VLSI industry is increasing the memory capacity of the digital systems (Bushnell *et al.*, 2004) . Because of this more than fifty percent of the die area is occupied by memories. This results in the high power consumption of the embedded systems. High power consumption in VLSI circuits leads to the increase in heat dissipation. In order to reduce heat dissipated because of high power consumption additional heat sinks are required. Also special packaging techniques must be adapted there in turn system cost increases (Alfailakawi *et al.*, 2015). Low power memory design technique proposed by industry are concentrating on the power consumption reduction during memory read and write cycles (Mai *et al*., 1998) (Karlsson *et al*., 2005). Here is a technique which concentrates on memory read and write time power consumption and also the circuit complexity.

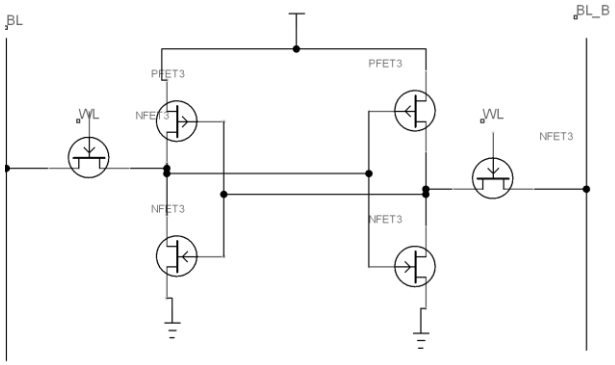


Figure-1. Schematic diagram of standard 6T SRAM cell.

Static Random Access Memory is the main memory block in cache memories. Figure-1 shows the schematic diagram of standard 6T SRAM cell. Low power SRAM construction greatly affects the power performance gain in any embedded circuits (Yamaoka *et al.,* 2004). As per Moore predictions year by year the supply voltage reduction because of technology scaling greatly effects the power consumption. But the significant increase in static leakage current is observed due to scaling (Nii *et al*., 1998). If the technology scaled beyond 10nm there are some other parameters which are altering the system behaviour. So the design engineers looking efficient solutions other than technology scaling for low power system design.

RELATED WORK

Previously, power dissipation is a major design factor in portable system design only. Now the scenario is changed. Now power dissipation is the major design factor in all the digital circuits. Power dissipation in memories is mainly because of switching activity of the cells and the leakage power in the idle condition. These power factors are termed as dynamic power and static power respectively. Dynamic power is nothing but the power consumption due to switching activity of the SRAM cells. Whereas, static power is mainly because of the leakage power when the circuit is in idle case (Karandikar *et al*., 1998). Static power is the major contribution in power consumption in memories (Wang *et al*., 2012). Baghel, *et al*., 2015 proposed memristor based SRAM using MTCMOS technique for low power consumption.

Static power can be calculated with the help of leakage current during idle phase. During idle mode the access transistors are in cut-off and the bitlines are charged to VDD. The proposed SRAM structure has minimum width and the small VDS (Drain- Source Voltage). During standby mode, WL, WR, RD are all maintained at 0V logic zero.

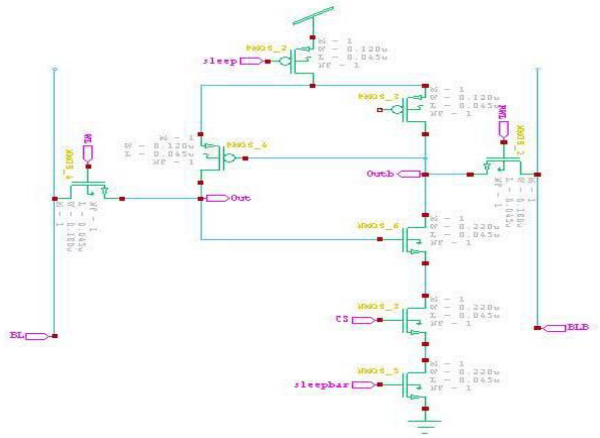


Figure-2. Modified MTCMOS with sleep transistor architecture.

Supply voltage reduction is one method followed to get low power structures. But the SRAM reliability is very much reduced when the supply voltage reduced further (Indumathi *et al*., 2006). At low voltages the noise margins also reduce there by it is very difficult to distinguish the two stable states. Stability can be quantified with Static Noise Margin (SNM). The least required voltage to change a logic cell from one logic state to other is called the Static Noise Margin. Along with supply voltage threshold voltage also reducing as technology is scaling year by year. Lower threshold voltages may lead to increase in leakage power (Madhusudhan *et al*., 2018). When the technology scaled beyond 90nm the leakage power is very much comparable to dynamic power. And when it is scaled beyond 75nm the static power is the major contribution in total power. This is because of the small lengths and widths of the transistors.

PROPOSED SOLLUTION

Static power can be figured with the assistance of leakage current during the SRAM circuit is in idle state. During this state the access transistors are in cut-off and the bitlines are charged to V_{DD}. The proposed SRAM structure has low V_{DS} and minimum width when standby mode, WL, WR, RD are altogether kept up at 0V rationale zero. The proposed architecture has a sleep transistor which is useful for reducing leakage power when in idle mode. The proposed design has transistors with multiple threshold voltages in order to reduce leakage power. Lower threshold voltage (V_{Th}) devices can reduce power consumption nearly 30 percent when compared with higher threshold voltage circuits.

Figure-2 shows the modified MTCMOS Static Random Access Memory architecture. All the transistors used to implement logic have low threshold voltage. Low threshold voltage transistors are used for quick switching activity. The transistors connected to the supply node are of high threshold voltage. Sleep transistors with high threshold voltage are used to reduce the leakage current. Low threshold voltage transistors are used in the logic. Pull up and pull down logic blocks are implemented with low threshold voltage transistors. Figure-3 shows the 8X8 SRAM schematic implemented with modified MTCMOS architecture.

EXPERIMENTAL RESULTS

Simulation results shown in Table-1 depict the total power and static power consumption of different SRAM structures. Comparison is made between standard SRAM, Memristor based SRAM (Baghel *et al.*, 2015), MTCMOS based Memristor SRAM and Proposed SRAM architecture. Comparative results show that a considerable reduction in total power and static power is observed in proposed SRAM structure. Figure-4 shows the graphical representation of the comparative results of both static and total power consumption for different SRAM structures. These results obtained for different SRAM structures at room temperature. Table-2 shows the comparative results of power consumption of different SRAM structures at different temperatures. Figure-5 shows the graphical representation of power consumption of different SRAM structures at different temperatures. Experimental results show that at low temperatures there is no much change in the power consumption of different SRAM structures but at high temperatures there is a considerable reduction in proposed structure.

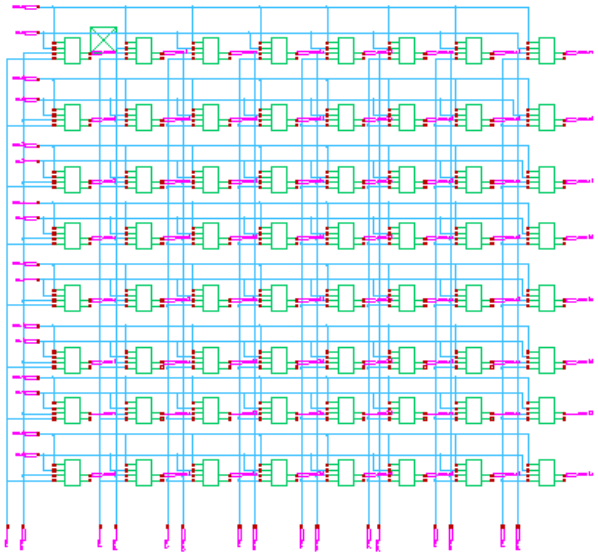
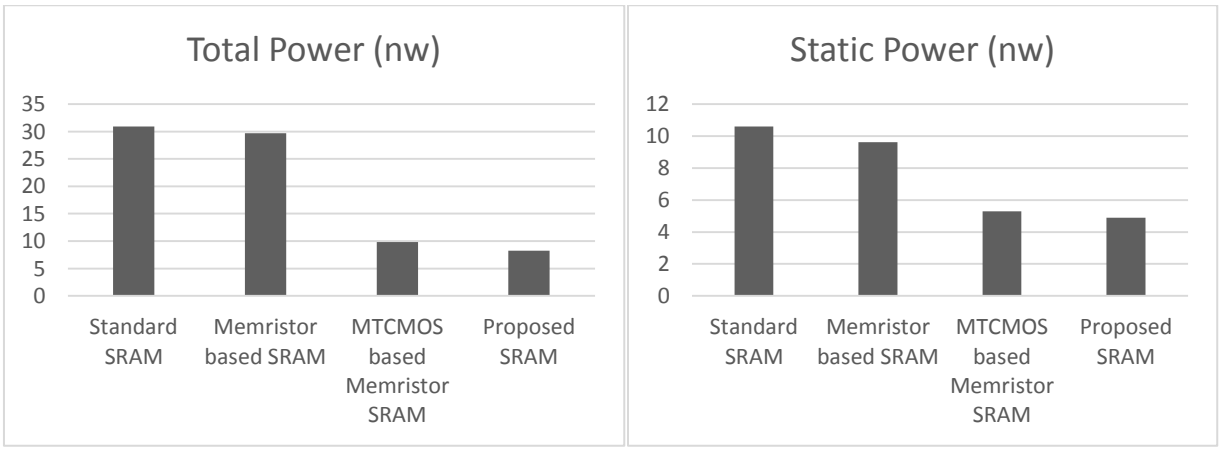


Figure-3. 8X8 SRAM schematic with proposed SRAM architecture.



(a) (b)

Figure-4. Comparison of total power and static power for different SRAM structures.

Table-1. Total power and static power for different SRAM structure.

SRAM	Voltage (v)	Total power (nw)	Static power (nw)
Standard SRAM	**0.7**	**30.90**	**10.59**
Memristor based SRAM (Baghel *et al.*, 2015)	0.7	29.69	09.61
MTCMOS based Memristor SRAM	0.7	09.84	05.30
Proposed SRAM	0.7	08.28	04.89

Table-2. Total power of different SRAM cells at different temperatures.

SRAM	Temp 10 ºC nw	Temp 25 ºC nw	Temp 40 ºC nw	Temp 55 ºC Nw
Standard SRAM	06.79	06.90	30.90	48.10
MTCMOS SRAM	04.90	06.43	09.84	18.12
Proposed SRAM	03.05	03.47	08.28	12.08

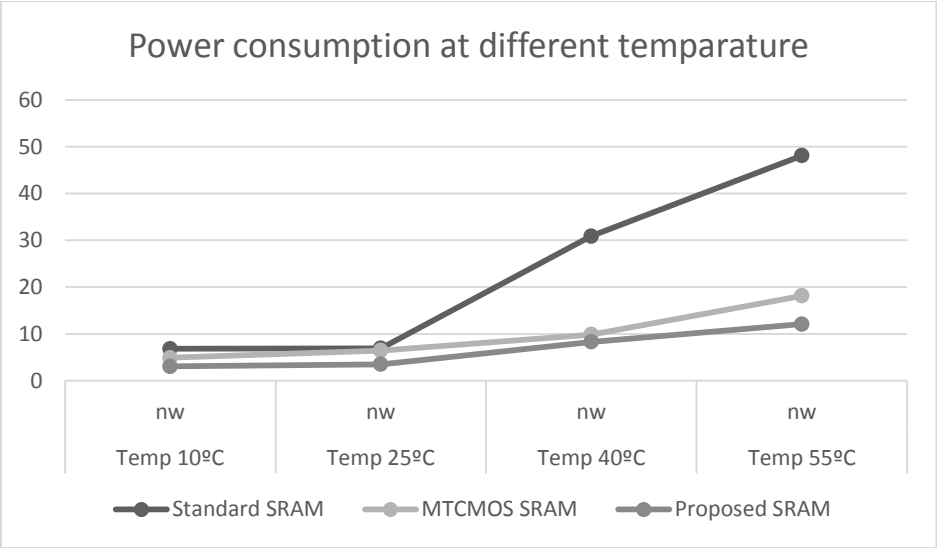


Figure-5. Graph representing power consumption of different SRAM structures.

CONCLUSIONS

This paper presents a novel architecture for SRAM construction. Power consumption in memories has two components. One is static power and the other component dynamic power. When the SRAM is in idle condition leakage current is responsible for static power, whereas the switching of any cell from 0 to 1 or 1 to 0 is responsible for dynamic power. When the technology is scaled beyond 75nm due to small lengths and widths of the transistors, leakage current has main contribution in total power consumption. Proposed technique is to construct a modified MTCMOS architecture to reduce leakage current. Proposed architecture is checked at different temperatures and is compared with standard 6T SRAM structure. Experimental results show that nearly 21% reduction in power consumption is observed in proposed 8X8 SRAM architecture when compared with standard architecture at rated temperature. Further proposed SRAM architecture can be improved by adopting double gate CMOS structures.

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