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# NOVEL 11-T FULL ADDER IN 65NM CMOS TECHNOLOGY

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**ABSTRACT**

In this paper, we propose an improved 11-T full adder circuit design for minimum power consumption. A novel adder cell is designed with new top-down approach using total number of 11 transistors, thereby, known as 11-T cell. After simulation of the circuit, a clear view of the circuit performance is studied. The proposed adder circuit is compared with reported cells and observed consumed lower in power consumption. The proposed cell gives faster response for the carry output and can be used at higher temperature with minimal power loss. The drawback of the circuit is that it occupies larger area on the chip.

**Keywords:** low power consumptions, delay, full adder, leakage current, area.

## INTRODUCTION

Adder is one of the fundamental arithmetic circuit blocks used in digital signal processing. Low power adders help to improve the performance of the circuit in computing application and digital device. Enhancement of performance is critical for the VLSI design in present. The speed, performance and power are the major constraints in VLSI. Some approach Transmission gate, Static Energy Recovery Full adder (SERF), Shannon based or bridge style adder has been proposed [1-6].Power dissipation and area are the vital role in portable devices [7-10]. Very large scale integration has increased rapidly with a reduced delay and power consumption characteristics [1]. Higher control utilization leads to abbreviated battery life and moreover expanded on chip temperatures, which may diminish the working life of the IC [2]. Bringing down the voltage shows up to be the most well-known implies to diminish power dissipation. In any case, bringing down supply voltage moreover increments circuit access time and debase the cells drivability planned with certain rationale styles.

From the past few years a long time assortment of reported adders has been proposed to decrease the power dissipation of VLSI systems. The adders are vital role in engineering and applied sciences. Standard CMOS 1-bit adder has 28 transistors and also dissipates more power. The advantage of standard CMOS adder is it has high stability, but the disadvantage is high number count of transistor and high output load and more consumption in power and area [3]. Transmission gate adder has 12 transistors [5]. The advantage is it has high speed and the design is simpler than the CMOS adder. The disadvantage is more power dissipation [3, 5]. The bridge style adder (BSA) has two different sum and carry outputs with 26 transistors. The advantage of this adder circuit is operating at high frequencies. In the transmission function principle is introduced in transmission function adder and 16 transistors are used. Due to this adder, the performance is improved as well as power consumption minimized. In the SERF adder circuit, a low logic level is introduced to remove the ground [3].Sleepy Keeper Approach adder (SKAA), the design approach consists of mainly the modified XNOR block, sum block, carry generation block and the sleepy keeper approach which was one of the most efficient power consumption methods and also reduces leakage power in the circuit.

In the present paper, we have proposed a novel 11-T adder for lower power consumption and gives best performance. A novel 11-T adder has 11 transistors and called as 11-T adder. To minimise the leakage power in the circuit, pMOS ($P_{st}$) transistor and a tail nMOS transistor are added into the circuit. The rest of the paper is structured as follows. A novel 11-Tcircuit is explained in section 2. In Section 3, results and comparison are discussed. Section 4 concludes the paper.

### Design of proposed adder circuit

A novel adder cell is designed based on following SUM and Carry Boolean expressions;

$$SUM = \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\overline{BC} \quad (1)$$

$$CARRY = AB + AC + BC \quad (2)$$

The proposed 11-T adder cell has three inputs A, B and C. It is implemented using XOR, inverter, and MUX is as shown in Figure-1. When the inputs A and B are low, the XOR gate will introduce 1-$V_T$ loss. Due to this, the N1 transistor (N1) not to be completely off (weak inversion) and results in leakage current. To avoid this problem, a T6 (Pst) is introduced in the inverter and also nMOS (tail transistor) transistor is added as shown in Figure-1. Due to these extra transistors, overall area is increased.

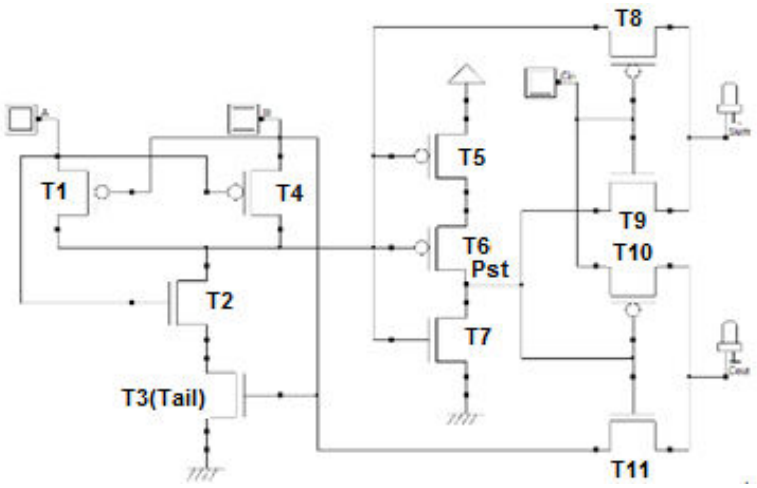


**Figure-1.** Proposed adder design.

## RESULT AND DISCUSSIONS

The proposed full adder circuit as well as other reported circuits is simulated by using MICROWIND tool for power consumption, area, and delay at 120nm and 65nm technologies with appropriate supply voltages are given in Table-1. Figure-2 shows the 11-T full adder cell dissipates lower power compared to other reported circuits and also gives faster response for carry out but occupies larger space on the chip and degrades sum output response compared to other design. Figure-2 shows the maximum power saving is reported to be 82 % at65nm compared to Standard CMOS adder circuit.

**Table-1.** Power and delay at different technology.

| | **65nm** | **120nm** |
|---|---|---|
| **Power consumption** | **0.321 µw** | **0.731µw** |
| Size | W:24µm H:7µm | W:26µm H:8µm |
| Sum Delay | 1.30ps | 3.00ps |
| Cout Delay | 1.90ps | 3.00ps |

Power consumption of proposed full adder cell is classified into two types of static and dynamic power. Static power dissipation can be due to subthreshold leakage through OFF transistors, and for dynamic dissipation can be due to load capacitances or "short-circuit" current through partially ON transistors. Most of the power is consumed by sum block. Dynamic power consumption is more when compare with the static power consumption because of discharging and charging of the load capacitance in transistor [6]. It can be formulated in Equation (3) as

$$C_{load}=C_{fix}+C_{var}. \quad (3)$$

Fixed capacitance ($C_{fix}$) is technology and interconnection dependent. It can be reduced by effective design and transistor size plays important role in reducing the dynamic power consumption. Inverter in full adder should be weak and transmission gate should be strong.

**Table-2.**Comparison between different types of full adder.

| | Technology | |
|---|---|---|
| **Design style** | **65nm** | **120nm** |
| Proposed 11T Adder [3] | 0.321µW | 0.731µW |
| Standard CMOS adder [3] | 1.771 µW | 18.75 µW |
| BSA [3] | 2.520µW | 29.79 µW |
| TGA [3] | 1.303 µW | 13.272 µW |
| TFA [3] | 0.648 µW | 7.39 µW |
| Square root based adder [3] | 0.516 µW | 6.73 µW |
| SERFA [3] | 0.345 µW | 4.291 µW |
| Ex NOR [1] | 3.18 µW | |
| 13T full adder [1] | 2.18 µW | |
| SKAD [1] | 1.28 µW | |

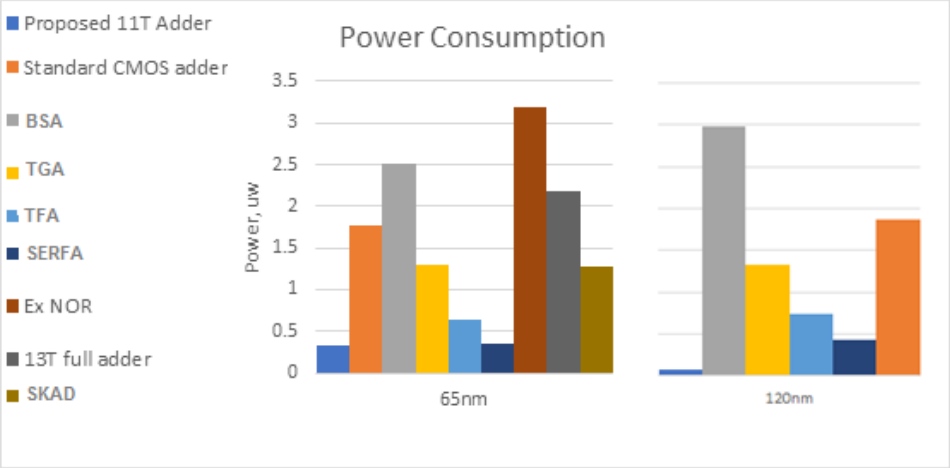


**Figure-2.** Power consumption at different technology.

The delay of the adder decides the speed of the circuit. Propagation of the carry signal is mainly responsible for the speed response of the adder. To reduce the propagation delay of the carry signal, the path length of this signal should be minimized. Area of the layout is also a condition to reduce the power consumption. Shorter path in the layout will reduce the resistance when the current go through the metal in different connection. By reducing the transistor count, the proposed adder reduces significantly in term of the area usage. Compared with other approach of design standard MOSFET used the larger area due to it having the more transistor in the design, the proposed adder only consume of (24X7) in 65nm and (26X8) in 120nm technology are given in Table-3. Figure-3 shows the layout of novel 11T adder circuit.

**Table-3.** Area and transistor count.

| **Design style** | **Area** (µm2) | **Transistor count** |
|---|---|---|
| Proposed 11T Adder | 168.0 | 11 |
| Standard CMOS adder (1) | 517.1 | 28 |
| BS adder(3) | 649.3 | 32 |
| TG adder(2) | 414.5 | 20 |
| Transmission functional adder (5) | 299.4 | 16 |
| Square root based adder (4) | 133.2 | 15 |
| SERF adder(6) | 168.7 | 10 |

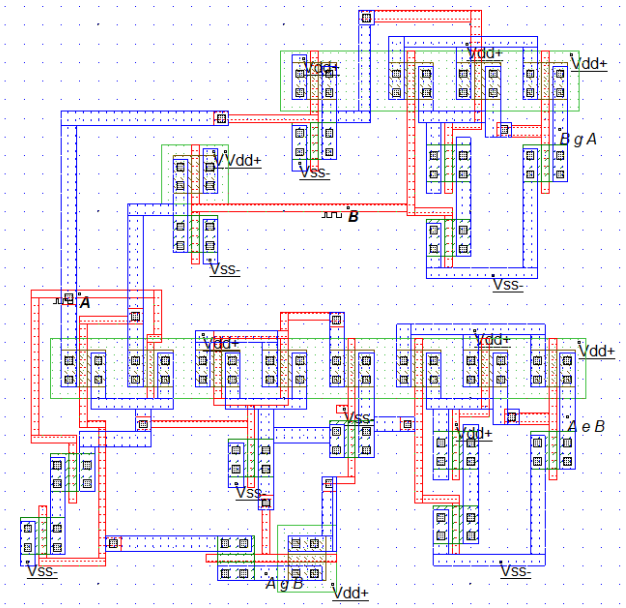


**Figure-3.** Proposed adder layout diagram.

This Analog simulation result is simulated over the period 20ns interval. The power dissipation results are obtained in each style using two different process technology foundries (65nm and 120nm). Figure-4 shows the output form of the 11-T Full Adder is based on it truth table shown as below (in Table-4).

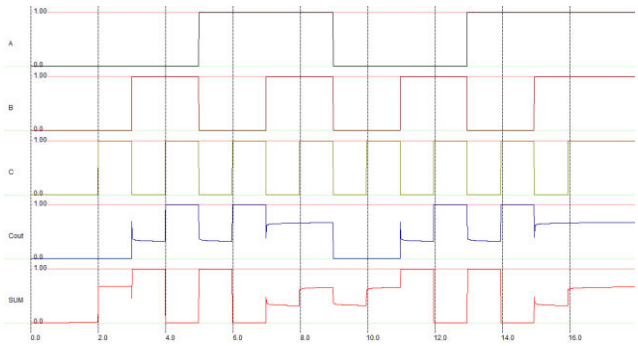


**Figure-4.** Proposed adder output waveform.

**Table-4.** Truth table of 1-bit full adder.

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **A** | **B** | **C** | **Sum** | **Cout** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## CONCLUSIONS

The proposed 11T full adder cell includes a stacking effect to reduce the leakage power of the circuit. The proposed adder is having low power consumption and size compared with other design. From the power analysis, it can be concluded that 11T Full adder cell consumes 82 % and gives fast response for the carry out at 65nm lower than Standard CMOS adder circuit. The only drawback of the proposed 11T adder circuit is area overhead.

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