IMPACT OF PROCESS VARIATION ON MULTIPLE-TUBE GAA- CNTFETS

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ABSTRACT
As miniaturization of conventional MOSFETs leading to its scaling limits, novel nano-scale devices are studied and developed. To improve $I_{on}/I_{off}$ ratio gate controllable wrap-around gate CNTFETs are recently investigated. The Gate-All-Around (GAA) CNTFET is one of the best types of CNTFETs which gives the environment for technological scaling beyond 10 nm because of its electrical and physical properties. In nano-scale device design, ultrathin body with GAA-CNTFET is an ideal choice to improve the performance. As device dimensions minimizes, new processing steps increases the source of variation. To address these issues during scaling, there is a necessity for device engineering and new nano devices based on different principles of physics. In this paper, we have studied the effect of diameter, chiral vector, Gate oxide thickness, different dielectric material constant, number of CNTs on threshold voltage ($V_{th}$) devices based on different principles of physics. In this paper, we have studied the effect of diameter, chiral vector, Gate oxide thickness, different dielectric material constant, number of CNTs on threshold voltage ($V_{th}$). It is observed that chiral vector ($n,0$) with increasing values of $n$ is more sensitive towards reduction in threshold voltage and also in our simulation it is analysed that when the number of CNTs are equal to N, drain current increases in the same order. In addition to this, the effects of quantum capacitance on these parametric variations have also been plotted. From the simulation, we analysed that chiral vector is very crucial parameter for CNTFET devices to control threshold voltage of the transistor.

Keywords: multi-tube GAA CNTFET, threshold voltage, quantum capacitance, chiral vector, process variation.

INTRODUCTION
Metal-oxide semiconductor field-effect transistors (MOSFETs) are one of the main devices which have been used in most of the circuit designs in VLSI. As forecasted by International Technology Roadmap for Semiconductors (ITRS) 2020, the industry needs transistors whose channel length is smaller than 10 nm. This size of the transistors will not be reached using MOS technology due to characteristics of silicon. For nano-scale transistors large portions of short-channel effect (SCE) for example drain-induced barrier lowering (DIBL) and high leakage current cannot be appropriately controlled any longer [1-2].

Then again, compact electronic gadgets are developing quickly. A few applications, for example mobile phones and handheld PCs expend a more amount of energy through leakage current. Moreover, in some of this application for example biochips and sensor organize hubs batteries are difficult to be charged or replaced. Therefore, low power devices are highly demand of interest to limit the power utilization and working for a more time without battery charging. The other critical challenge of the recent chip is high power density which is the outcome of improper scaling of the size and power utilization in VLSI technology. Thus the supply voltage should be reduced and it is very close to the threshold voltage of the transistor which is minimum energy required of any transistor. In conventional MOSFET transistors supply voltage cannot be degrade excessively because of performance and functionality of device might be demolished. In recent years some of the devices such as Fin-based Field Effect Transistors (FinFETs) lead by Intel, Fully Depleted Silicon On Transistors (FD-SOI) lead by STMicroelectronics, the Carbon Nanotube Field Effect Transistor (CNTFET) lead by IBM, the Resonant Tunnelling Diode (RTD) and the Single Electron Transistor (SET) but all devices which are introduced to replace the CMOS transistor, CNTFET is one of the promising candidate beyond 10 nm node for their properties such as high mobility of ballistic transport, high mechanical and thermal stability, high resistance to electro migration [3-5].

Carbon nanotubes (CNTs)
S. Iijima found Carbon Nanotube (CNT) was at the NEC Fundamental Research Laboratory in Tsukuba, Japan in 1991 [6]. Carbon Nanotubes (CNTs) are hollow cylinders having diameter one to tens of nanometres and length up to centimetres. Carbon Nanotubes (CNT) have $Sp^2$ hybridization, the same structure as graphite. Carbon Nanotube (CNT) is rolled up sheet of graphene.

GAA-CNTFET
Carbon nanotube can be considered as a sheet of graphene which is hollow cylindrical structural. The property of CNT can be either semiconductor or metallic it depends on chirality (n, m) of carbon nanotube. If n-m=3K ($K \in Z$) and n=m, the property of CNT is metallic otherwise it is semiconductor and can be utilized as the channel region of CNT based transistor. Now a days there are several types of CNTFET introduced [7]. The Schottky-barrier CNTFET has been working on the work function difference between metallic source or drain and CNT. It has a low Ion/Ioff ratio [8]. The MOSFET like CNTFET having top gate and highly doped source and drain are still some challenges such as potential barriers and tunnelling effect at the contact and need doping technique. Higher gate control is required for any transistor beyond 10 nm size so that the GAA CNTFET has been researched [9-12]. The structure of the GAA
The CNTFET device is as shown in Figure-1(a). In this device, the channel region is made using intrinsic CNTs and CNTs channel region is surrounded by gate and gate oxide. The CNTs are put on a thick layer of insulator to overcome body effect so it is assumed that there is no body terminal effect. The mobility of electron and holes in CNTs is the same. The gate width of GAA-CNTFET can be derived by Equation 1 where N is the number of CNTs and S is the spacing distance between two CNTs.

\[ W_{\text{gate}} \approx (W_{\text{Litho}}, N \times S) \]  

The model of this device is given by Stanford University as Virtual Source (VS) CNTFET [9-12]. The diameter of CNT can be depended on chirality \((n, m)\) and determined by Equation 2.

\[ D_{\text{CNT}} = \frac{\sqrt{3a\sqrt{n^2+m^2+nm}}}{\pi} \]  

The effect of chiral vector \((n,m)\) on threshold voltage

The property of CNT can be either metallic or semiconductor, its depends on chiral vector of CNT. The chiral vector of CNT is shown as the pair of integer \((n, m)\). If chiral vector is \(n=m\) or \(n-m=3K\) \((K \in \mathbb{Z})\) then the property of CNT will be metallic otherwise semiconductor. The diameter of CNT is also depend on chirality of CNT as shown in Equation 2. Diameter increases when the chiral vector increase as shown in Figure-3. The direction of the CNT chiral vector is denoted by chiral angle \(\theta\). The formula of chiral angle \(\theta\) is as shown in Equation 3.

\[ \cos \theta = \frac{n+m}{\sqrt{n^2+m^2+nm}} \]  

For the property of the CNT, the difference of the chiral angle and diameter are very important parameters. The threshold Voltage \(V_{th}\) of CNTFET devices is as shown in Equation 4.

\[ V_{th} \approx \frac{W_{\text{Litho}}}{2} \left( \frac{W_{\text{Litho}}}{2} + \frac{L_{\text{eff}}}{2} \right) \]  

RESULT AND SIMULATION

This section shows the simulation result of GAA-CNTFET. The cadence tool and nanoHUB tool is used for the simulation. We also changed the different dielectric material as a gate oxide layer which has different dielectric constant as shown in Table-1.

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Material</th>
<th>Dielectric value (K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Silicon dioxide ((\text{SiO}_2))</td>
<td>3.9</td>
</tr>
<tr>
<td>2</td>
<td>Zirconium Silicate ((\text{ZrSiO}_4))</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>Hafnium Silicate ((\text{HfSiO}_4))</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>Hafnium dioxide ((\text{HfO}_2))</td>
<td>16</td>
</tr>
<tr>
<td>5</td>
<td>Zirconium dioxide ((\text{ZrO}_2))</td>
<td>25</td>
</tr>
</tbody>
</table>
varying with respect to chiral vector of CNT as shown in Figure-4. Threshold voltage decrease when increase the chiral vector as shown in Table-2. We considered eight combinations of chiral vector and analysed the result. When the chiral vector is small, threshold voltage is high and when chiral vector is small, threshold voltage is less. The reason of threshold voltage decrease with respect to chiral vector is as shown in Equation.4.

\[ V_{th} = \frac{a(\pi)}{\sqrt{3(\pi R_{CNT})}} \]  

(4)

**Effect of thickness of oxide layer on threshold voltage**

We have carried out the detail analysis for varying the thickness of oxide layer to see the effect of threshold voltage of GAA-CNTFET device. A relation between the thickness of oxide layer vs. threshold voltage is shown in Figure-5. In fact when the thickness of oxide layer increases, threshold voltage decreases.

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**Table-2. Threshold voltage of GAA-CNTFET w.r.t. chiral vector.**

<table>
<thead>
<tr>
<th>GAA-CNTFET parameter</th>
<th>Chiral vector (n,m)</th>
<th>( V_{th} ) (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(8, 0)</td>
<td>654,468</td>
</tr>
<tr>
<td></td>
<td>(10, 0)</td>
<td>515,874</td>
</tr>
<tr>
<td></td>
<td>(11, 0)</td>
<td>465,92</td>
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<tr>
<td></td>
<td>(13, 0)</td>
<td>393,596</td>
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<tr>
<td></td>
<td>(16, 0)</td>
<td>327,969</td>
</tr>
<tr>
<td></td>
<td>(19, 0)</td>
<td>262,04</td>
</tr>
<tr>
<td></td>
<td>(22, 0)</td>
<td>222,69</td>
</tr>
<tr>
<td></td>
<td>(25, 0)</td>
<td>194,136</td>
</tr>
</tbody>
</table>

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**Effect of high-K dielectric on threshold voltage**

\( SiO_2 \) has been used as a gate dielectric material since the discovery of the MOSFET in 1960 due to its electrical and thermal stability between Si and \( SiO_2 \). High speed and small size in integrated circuit are obtained by reducing the physical thickness of \( SiO_2 \) and gate length. If the physical thickness of dielectric is so thin, mainly when it is less than 1.5 nm then direct tunnelling and circuit power dissipation will increase [13]. The possible solution to overcome this problem is to use High-K dielectric material as a gate oxide.

Threshold voltage of different dielectric material of GAA-CNTFET device is as shown in Figure-6. Higher
the value of dielectric material, high will be threshold voltage as same physical thickness.

**Figure-6.** Dielectric material vs. threshold voltage of CNTFET.

**Effect of number of CNT on threshold voltage**

Carbon nanotube (CNT) is single sheet of graphite layer which rolled into cylinder structure. In GAA-CNTFET structure, CNT is used as a channel material. If number of CNT increased as a channel material, it is not affected threshold voltage of the device but it is affected on drain current. Drain current will increase as same order of CNT. If number of CNT is equal to N then drain current will increase N time as shown in Figure-7.

**Figure-7.** Gate voltage vs. drain current of CNTFET.

**CONCLUSIONS**

As the device scaled down, threshold voltage is very important parameter for any device because of its affect leakage power. One of the best part is for GAA-CNTFET, threshold voltage can be controlled by changing some parameter. Our simulation study shows that chiral vector of CNT is very crucial parameter for controlling threshold voltage. We analysed that threshold voltage is high at lower chiral vector and threshold voltage is low at higher chiral vector. We have also seen that thickness of oxide layer also affects threshold voltage. As increase the thickness of oxide layer, threshold voltage will be decrease.

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**REFERENCES**


