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DESIGN AND IMPLEMENTATION OF EMBEDDED TRUE PARALLELISM JAMMER SYSTEM USING FPGA-SoC FOR LOW DESIGN COMPLEXITY

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ABSTRACT

The condition that drives a system to complete the processing of a number of functions within a given amount of time is called the real-time system. A projective missile system's processing platforms face two major issues: high cost and structural complexity. The system structure's complexity is a result of various reasons that include the mechanism utilised in the system in order to perform the system functionality. This mechanism can lead to delays in data processing because various factors, such as the synchronisation of the system modules' signals, the processing unit's architecture, and the unit's computational power. In order to lessen system complexity and system cost, true parallelism mechanism is applied over the embedded system, along with a concurrent structure. The FPGA platform (DE1-SoC) was used as the implementation environment for this system. This led to an enriched implemented system that had low costs. Furthermore, the system complexity is lessened since the system uses a concurrent structure. Some of the modules that are closely related to the system are implemented to support main processing module. In this system, the signals covered were in four directions. The total logic element was (5032) and total registers was (5180). The Phase Locked Loop up to (1.6) GHz was manipulated in order to allow the system cover a wide spectrum of signals with high accuracy of computing process. Furthermore, the laser projective frequency jamming system is capable of processing multiple frequencies at a time. The implementation was able to obtain acceptable levels of throughput and it also lowered the complexity. Furthermore, the structural design methodology also makes it possible for the embedded concurrent computing architecture to be scalable while the entire system grows.

Keywords: embedded system, field programmable gate array, true parallelism, frequency jamming.

INTRODUCTION

Embedded systems are also considered as reactive systems, which means that they continuously react to the environment and mostly have the real-time respond characteristic. Recent trends in the development of embedded systems have moved away from being restricted to a specific function. Instead, alternative trends have more flexibility that will allow one to modify, add, and even delete some of the embedded system's sub-functionality units. In fact, changes are already taking place in the field of embedded systems even while this research is being conducted. As such, the goal is to make these embedded systems as fast and small as possible. One of the areas of application that the embedded systems encompass is the mission critical area which includes avionic, frequency jammer, and spacecraft [1].

The need for big companies to meet customer requirements has made them consider certain key features during the design and implementation of their systems. The most important features that need to be considered are the re-configurability, power consumption, cost, and time to market. The FPGA possesses all these features and even some more characteristics like reliability and the capacity to process data in a parallel manner [2]. Although the focus of this thesis was on enhancing system performance and improving the throughput through the application of true parallelism, the relative complexity was also considered. Thus, the mapping tasks of the high-level designing stages could be transformed into lower-level sub-tasks to lessen the complexity of the functionality units. The design that was proposed aimed to simplify the complicated tasks in order to come up with a system that had as much real-time responses as possible.

Currently, FPGA-based systems have the capacity to merge the advantages of both ASIC and DSPs. This leads to systems that are capable of rapid development cycles, high reliability, easy upgrading, high flexibility, and moderate costs[3]. This project utilised the FPGA in the design and implementation of its functional units in order to take advantage of these features. Harnessing the FPGA resources within this project led to better performance and higher throughput since true parallelism was utilised in its implementation.

This paper aims to achieve the ability to process multiple signals at a time instead of just processing a single signal. Other aspects like the power consumption, cost, reconfigurability, and portability were improved with the use of the FPGA platform as the proposed system's implementation environment. It has been proposed that less than four aircraft fighters must utilise their laser missiles during the attack of a single target because a laser beam interference situation might take place if more than four laser missiles are launched to destroy a single target. As such, a laser missile frequency jamming system that can process four frequency signals at a time and control four defused plates was proposed. This will allow the system to direct the frequencies that have been captured towards attacking aircraft fighters.

Additionally, supported modules are designed and implemented such as the input signal unit manager that can synchronise four input signals, the signal emulator module that produce test signals to check the functionality of the system when there are no available signals, the

output data buffer module that is responsible for storing the captured and processed signals for later studies, and the address generation unit which generates addresses for the processed data so that they can be stored within the output data buffer.

The HT-decoder pins are linked to receive signals, as the codes are distributed into discrete portions, where each part is considered an independent process by concurrently executing operation for various modules. True parallelism was employed in this case. This suggests that each calculation is independently treated from the computation values of all other cells to maintain an interpolated value for every grid cell in the lattice. First, the spectrum of the signal is analysed by the jammer, sent by the frequency hopped transmitter. Then, the extraction of the features of the signal is carried out. The frequency synthesiser then picks up these features to create the same hopping frequency. Finally, the display units on board such as the Seven Segment and LCD pick up the narrow-band interference signals for display.

RELATED WORK

In scientific and engineering applications, a design philosophy that has now become mainstream is the embedded multiprocessor core. Recent FPGA devices offer increased performance and enhanced gate capacity that allow integrating complex logic systems on a single programmable device. However, a new problem has been created with these embedded multiprocessors regarding thread safety [4].

This is caused due to the shared memory, where multiple processors get access to the same value at the same time due to thread safety violation. Basically, micro architectural enhancements and clock scaling technique[5]can be adopted to improve the performance of the processor. This led to development of a new architecture known as Embedded Concurrent Computing (ECC), which uses VHDL to integrate with the FPGA chip. Simultaneous use of both distributed and parallel computing can be achieved through this Embedded Concurrent Computing (ECC) architecture. An embedded multiprocessor core's complete architecture is designed to perform realistic logical, arithmetic, bit manipulation and shifting operations. The proposed embedded quad processor core is geared with Homogeneous Embedded RISC processors[2] that include multibus organisation, pipelined processing units and I/O ports along with additional functional elements needed for implementing embedded SoC solutions. The Xilinx tool is employed at 90nm process technology to analyse the performance issues associated with the designed quad core, including speed, area, power dissipation and propagation delay.

To produce jamming signals, each range of the jamming signal's bins is determined by the system. These are then re-transmitted to the directions of the missile borne SAR. Implementing this with the TMS kit could help the system counter some of the difficulties.

Based on Krishnaiah & Brundavani (2013), the FPGA architecture was employed for jamming the wireless signals that were sent from a mobile base station by preventing the signals from reaching the mobiles, especially in regions where the use of mobile phone is banned. The same frequencies are employed by the proposed mobile jammer as that of the base station for transmitting radio waves, which create interference alongside base station and mobiles and cause disabling of these phones, making them unstable to jam the whole operation.

The FPGA pins have replaced the Holtek encoder switches for FPGA outputs and for sending the signals. These pins also allow selecting another pin to facilitate a binary form for the transmission function[6].

Huabao *et al*. (2013) proposed a digital signal processing unit design employing the Constant-False-Alarm-Rate (CFAR) algorithm to identify signals in the Frequency Modulated-Continuous Waveform (FMCW) radar system. The proposed design uses 1,625 LUTs, 857 logic slices and 499 FFs. Also, this design can operate at a speed of 121.33MHz, which allows saving a lot of available resources. Authors in Ref.[7]have harnessed the SoC technology to design a general method that can be employed in the universal control system of tactical missile. For the industry category, one of the high throughput circuits is the mobile phone jammer PRO45 high power manufactured by Jammer Store. This device can generate jamming signals for the mobile operator's mobile frequencies within 100 metres. It offers jamming signals with frequencies ranging up to 950 MHz but these features cost more and power consumption is high as well. At the same time, such type of system cannot be reconfigured as the design is not based on the FPGA chip providing such features.

Based to Muataz Hameed Salih *et al,* 2016, Design and Implementation of Laser Missile Jamming System, in this paper the advantages of applying the spatial parallelism over the Altera Nios II Embedded Evaluation Kit (NEEK) board are presented. The spatial parallelism was used to design and implement a laser missile frequency jamming system. The spatial parallelism is combined with the FPGA features, which improves designed system in many aspects such as increasing the system throughput, decreasing the system cost, the power consumption of the system, and the system complexity[8].

Altera design and implementation environment

Since the success of any embedded system begins right from the evaluation phase, selecting the right platform is a significant step in the design of any embedded system. The following paragraphs shall present the strength and platforms and why FPFAs are considered the best in the design of Qsys.

The DE1-SoC Development Kit presents a robust hardware design platform built around the Altera System-on-Chip (SoC) FPGA as shown in Figure1, which combines the latest dual-core Cortex-A9 embedded cores with industry-leading programmable logic for ultimate design flexibility. Users can now leverage the power of tremendous re-configurability paired with a high-performance, low-power processor system. Altera's SoC integrates an ARM-based hard processor system (HPS)

consisting of processor, peripherals and memory interfaces tied seamlessly with the FPGA fabric using a high-bandwidth interconnect backbone. The DE1-SoC development board includes hardware such as high-speed DDR3 memory, video and audio capabilities, Ethernet networking, and much more.

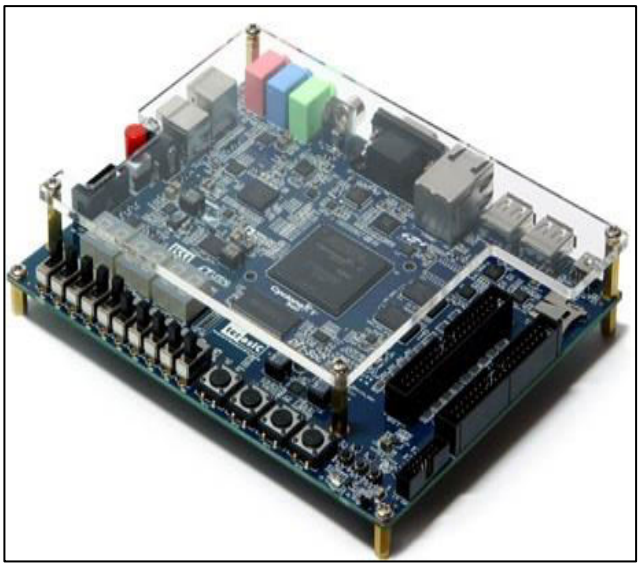

Figure-1. The Altera cyclone® V embedded evaluation Kit (DE1-SoC).

The DE1-SoC board has many features that allow has many to implement a wide range of designed circuits, from simple circuits to various multimedia projects [9].

Cyclone® V SoCs provide the industry's lowest system cost and power. The SoC FPGA high-performance levels are ideal for differentiating high-volume applications, such as industrial motor control drives, protocol bridging, video converter and capture cards, and handheld devices. SoC FPGAs come in a wide range of programmable logic densities with many system-level functions hardened in silicon - a dual-core ARM* Cortex*-A9 Hard Processor System (HPS), embedded peripherals, multiport memory controllers, serial transceivers, and PCI Express* (PCIe*) ports. The Cyclone® V GX Kit presents a robust hardware design platform built around the Altera® Cyclone V GX FPGA, which is optimized for the lowest cost and power requirement for transceiver applications with industry-leading programmable logic for ultimate design flexibility. The Cyclone V Starter Kit, development board includes hardware, such as Arduino Header, on-board USB-BlasterTM, audio and video capabilities and much more. In addition, an on-board HSMC connector with high-speed transceivers allows for an even greater array of hardware setups. By leveraging these capabilities, the Cyclone V Starter Kit is the perfect solution for showcasing, evaluating, and prototyping the true potential of Altera Cyclone V GX FPGAs.

Frequency jamming system design

As the modern embedded systems get larger, sophisticated, and even complicated, it will be easier for the designers and developers to perform their design at a higher level of abstraction and using or even reusing the customized the HDL components and this what was this project involved in its mechanism to provide the full functionality of the frequency jamming system as can be seen in Figure-2.

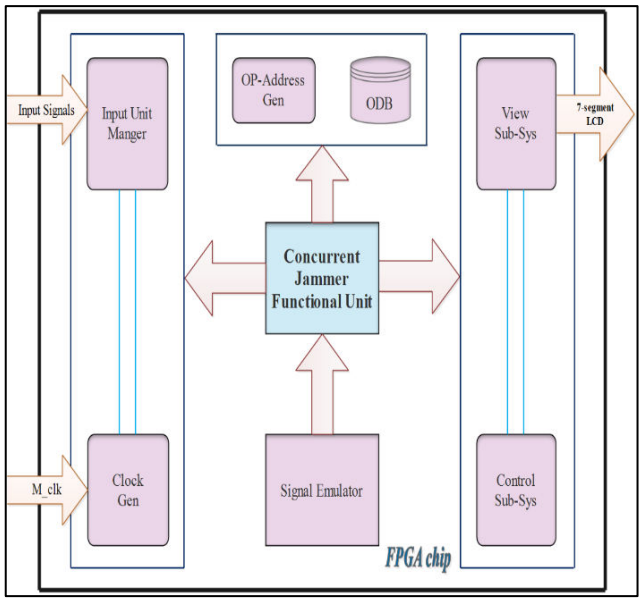

Figure-2. System top-level design.

The first part of the project includes associated function units which are required to accomplish the full functionality of this system; the second part consists of multiple functional modules that will detect in the beginning the frequencies which will be emitted from the transmission unit in general and specifically from the missiles launchers and continue processing the input data until passing these data to the LCD and seven segment. The other units within the first part are responsible for processing the detected frequencies until the result shown on LCD and seven segment. The detected frequency will be distributed over many platforms to direct these frequencies away from their targets. The control over these platforms will be done via a pulse width modulation unit and the last part which will be the contribution in this project is focusing on first to duplicate similar subtasks of the main system functionality which will be executed in simultaneously manner on the SoC environment and distribute tasks between the core processors. The Frequency Jamming system design harnessed some core concepts like true parallelism, locality and reuse in embedded application in order to integrate the desired improvement aspects like efficiency and performance.

A. Signal emulator

This module's key functionality is to check if the functionality of frequency jamming is on the right track, in cases the signals are not available, which were emitted

from the launchers, as presented in Figure-3. One of the functions of signal emulator is to produce signals to test the system when there is no activity of input signal. This action is performed to observe the behaviour of the system.

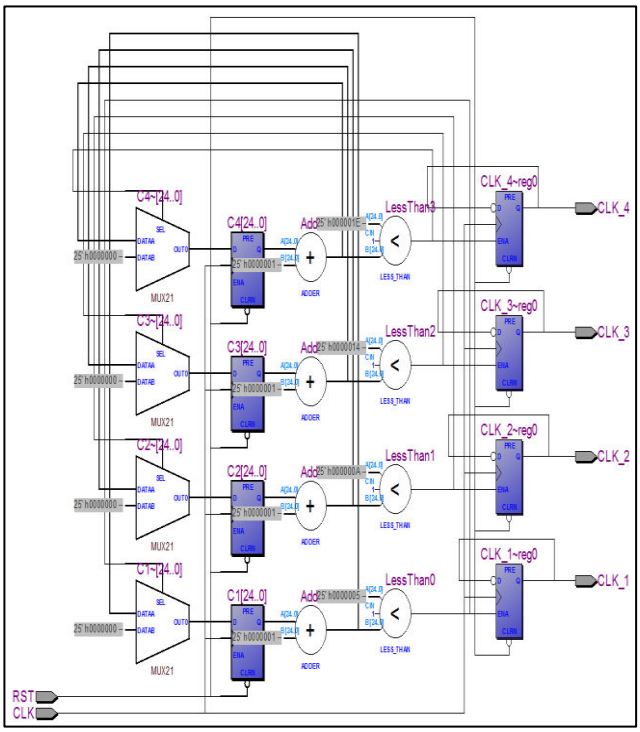

Figure-3. RTL view for the signal emulator.

The output of this module is the four input signals which have been used to check the system response and these signals are (50KHz, 90KHz, 166KHz, and 25 KHz) to be assigned to the assumed directions (front, back, left, and right) respectively.

B. Output data buffer

The system design is aimed at improving the performance as well as the overall throughput by employing true parallelism. However, whenever I/O data get access to the memory, deterioration of the system speed is caused. To avoid such a situation, data are temporarily stored by using an output data buffer, which allows processing of several data transmissions concurrently with the data processing.

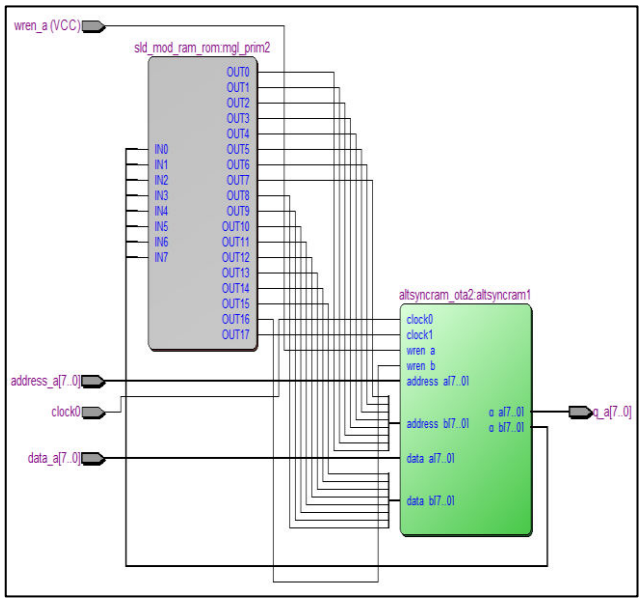

Figure-4. RTL view for the output data buffer.

This module employs the dual channel technique for performing functionality to enable reading/writing operations simultaneously. The ODB's size is 1 KB and indicates the module's capacity to store up to 1024 data, which constitutes this module's total memory addresses.

C. Output address generator

A memory unit of (1 KB) size is created to store the processed data or the frequencies detected by the system. In a system design, it is clear that getting access to the memory is a costly issue both in terms of power and time. Since data access is sometimes deemed as vectors indexed access stored in the memory, the output address generator creates a memory address for each one of the processed data, which is of the same memory size with each clock cycle to make sure that a unique memory address is assigned to each one of the frequencies.

D. Control sub-system

This module's functionality revolves around controlling motor that corresponds to every jamming platform. The design of the system was aimed at catering to numerous signals emitted my multiple laser missile launchers, where each signal is processed and then directed towards a single platform. The module controls each platform where motor drivers direct it towards the missile direction. The pulse width modulation (PWM) can be used to effectively control these multiple motor drivers, which employ digital signals rather than continuous signals for controlling motors. In general, the PWM input could either be 16-bits or 8-bits. This module employs an 8-bits input. The energy flowing towards the motor shaft can be organised by decreasing or increasing the pulse width. Controlling of motors through the pulse width modulation ensure lower jitter time [10].

The control unit's behaviour can simulate four combat aircraft attacks from different directions of the target for a single target; these directions include the back,

front, left and right, where this system suggests the aircraft to launch the laser missile in the direction of the target only from these directions. Else, an overlap situation is created amongst the attacking aircraft, which will make the attack to the targets useless if executed from more than these directions. Each laser missile that has been launched will have its own frequency to hit the target. These signals are processed by the main system functionality modules and the identified frequency of each laser missile is sent to different diffused platforms. Controlling these platforms would help in preventing the attackers from shooting the target. The system's reference clock is 50MHz and the module divides this clock as 1KHz duty cycle to maintain the same number as that of the system clock pulses in a single pulse width modulation period.

E. Concurrent jammer functional unit

Pursuit of the designers and researchers to improve the performance by speeding up the computation and increase throughput. The frequency jamming system is focusing on monitor the emitted frequency of the missile launcher and then processing the received signal in order to transmit on the same modulation a wrong data which is result in nontarget hitting. Usually more than one launcher is used at each sortie to destroy a specific target. The proposed system is capable of processing up to four signals at a time and control four diffused surfaces via the pulse width modulation module to direct each one of these diffused surfaces towards presumed laser missile launcher. To process more than a signal at a time, the true parallelism concept has been harnessed here as shown in Figures 5, 6. The harnessing of this concept result in various benefits starting from capability of processing more than a signal per time, improving the overall system performance, and increasing the system throughput. After the overall system functionality, has been designed and implemented using the VHDL and the Quartus II and verified via the DE1-SOC board, the true parallelism scheme has been applied on the overall system.

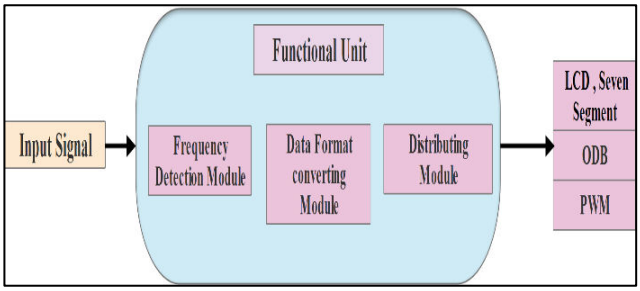

Figure-5. Concurrent frequency jammer functional units for temporal parallelism.

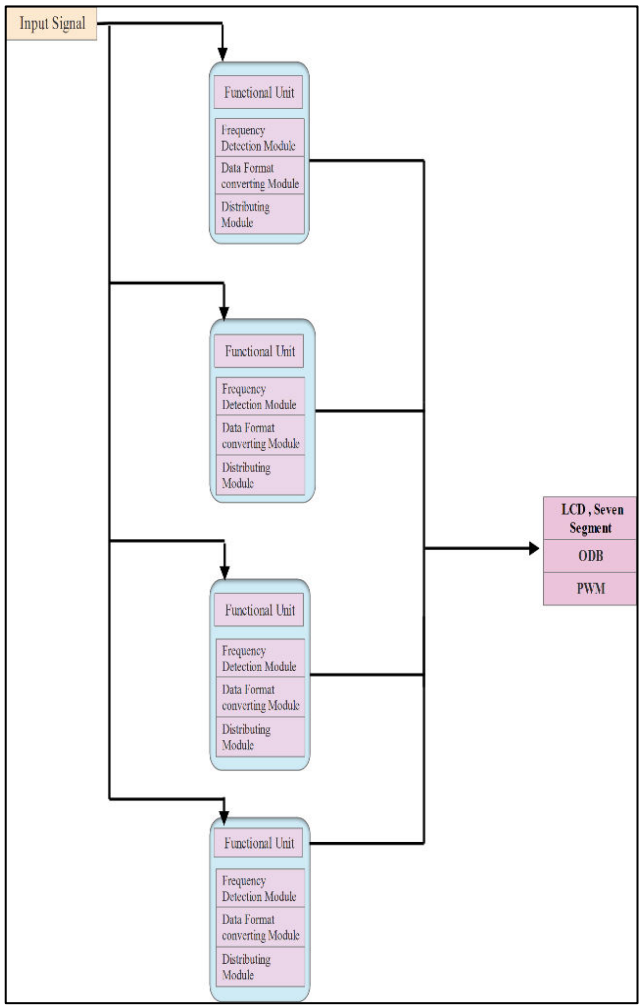

Figure-6. Concurrent frequency jammer functional units for spatial parallelism.

The mechanism of the true parallelism used to split the multi-functional units of the system into several parts and each sub-functionality unit be processed by different processing element. The core advantage of the true parallelism in this system is that more than subtask is processed in simultaneously manner so that multiple signals can be processed at the same time and then distributed to the other modules like the platforms which will direct the processed signals towards the signal emission source in order to jam this source and prevent it from the target, this platform is controlled by the pulse width modulation. The other modules which be the processed signals send to is the output data buffer to be stored and finally to the LCD and Seven Segment to be viewed.

F. View sub-system

In order to show the obtained results on the LCD and Seven segment, this module was designed for this purpose where it's responsible to transmit the overall results to the LCD and Seven segment unit mentioned earlier. In this section focus on reconfigurability, it can be used on more than board.

The first one the LCD, the first step in this module is to initialize the LCD Figure-7. This action is required for preparing the LCD to receive the commands. The beginning of this preparation stage represented in enabling the LCD itself first using internal signal as well as initializes the LCD. This was done with consideration of (27KHz) master clock. The mechanism in viewing the characters which includes both letters and digits is all about the use of the finite state machine (FSM) whereas the module structure based on dividing the result shown on the LCD to three partial stages.

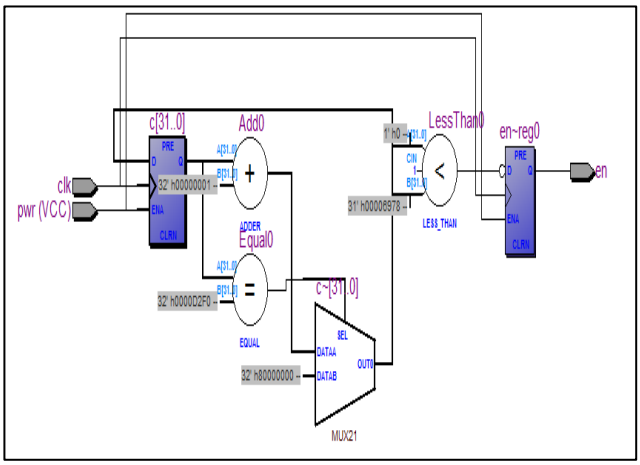

Figure-7. LCD enabling logic circuit.

When the LCD is in the entry mode and ready to receive data, the display step on the LCD module begin. The second state machine was to display the first the first four letters (FREQ) of the word "Frequency" and the special character (=) to have a final result like (FREQ= 50000). The entire internal view of the view sub-system is shown in the Figure-8.

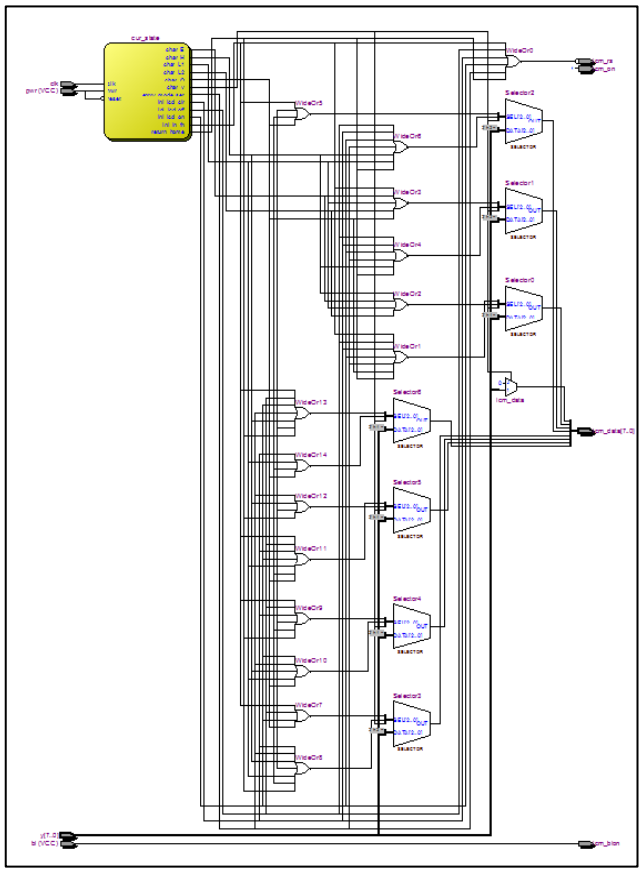

Figure-8. RTL View of the LCD (state machine).

Once the first "fixed" characters state machine is processed, the next state machine will begin to display the digits which represent the emitted frequency which is the result of the all previous stages. Another state machine is used to assign values to be shown in LCD at enabling state machine where the first four values is assigned to the control signals. When the control signal values are settled, the values of the characters and the 8-digits be assigned to each state of the corresponding state machine. Figure 9 the LCD state machine.

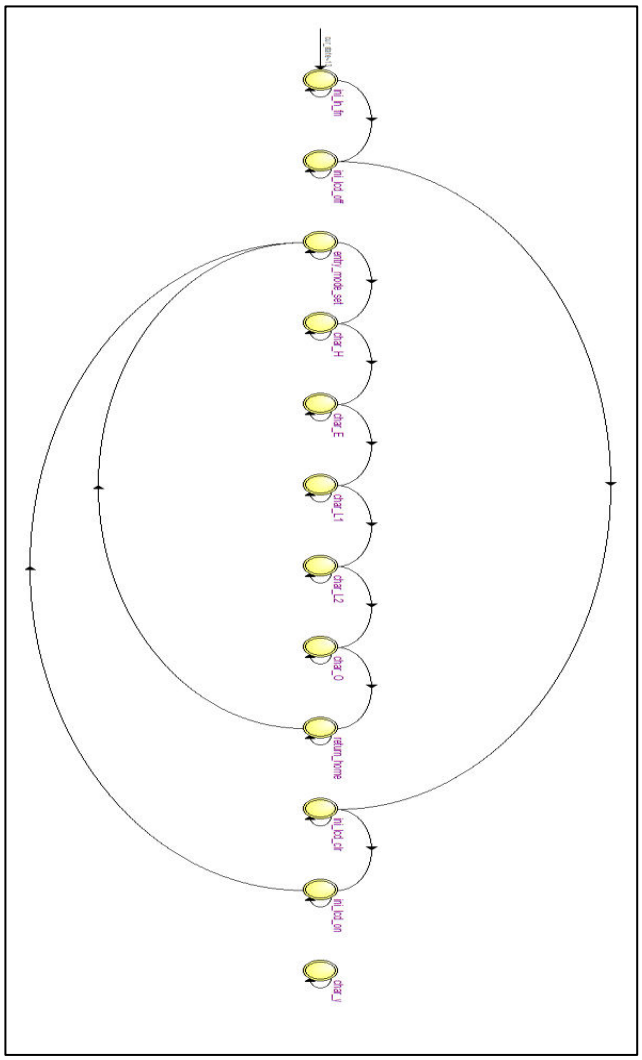

Figure-9. View of LCD state diagram cycle.

The second on Seven segment, the board contain 6-digit from seven segment. This action is required for preparing the seven segment to receive the commands (Read).

The name 7 segment is based on the fact that it has 7 LEDs that form the number 8 should all of them are 'on'. To form numbers from 0 to 9 as well as some alphabet letters, the 7 LEDs can be individually lit. The LED has 2 parts: the positive part called the anode and the negative part called the cathode. If a positive voltage is applied to the anode and the cathode is put to the ground (0V), then lighting up of the LED occurs. One of the LED's sides must be common to all of them (either the cathode or anode) and the other should be individual (7 data lines) for individually lighting up the 7 segments and make use of just the minimum pins as possible. The display having one anode is known as the common anode and the other is known as the common cathode.

A binary coded decimal (BCD) is a 4-bit number representing the numbers 0–9 (0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001). A BCD to 7 segment decoder allows mapping each of these 10 codes to 7bit codes (one bit for each segment) for controlling the display. The decoder 4 inputs employ one input of type std_logic_vector (3 down to 0) employing std_logic_vector or a type of std_logic. The output will be a std_logic_vector (6 down to 0). The selected signal assignment statement is used for the decoding as presented in Figure-10.

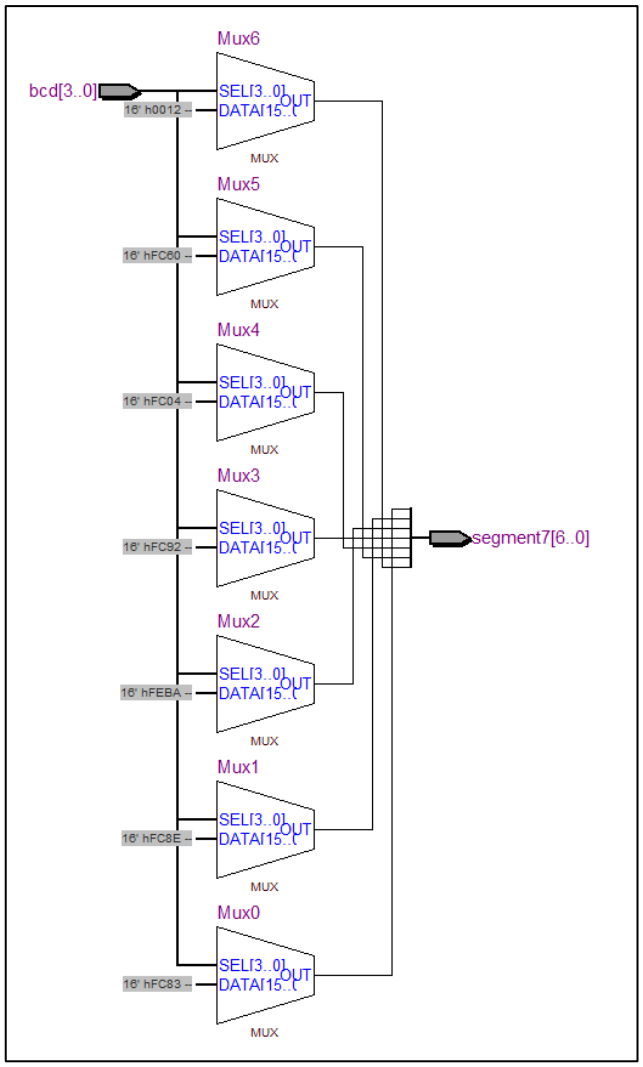

Figure-10. RTL for seven segment.

G. Distribution module

In logical circuits, a common scheme used is the multiplexing technique to send many data to multiple units through a single set of wires. In general, this functionality depends on the sequence timing in which the signals should be sent in a correct manner while simultaneously identifying the final destination of the signals. principle used via the multiplexing module to send multiple BCD digits to 7-segment which this approach is the same mechanism used to send the multiplexed data to the LCD. The 6-BCD digits which have been converted in the last stage will be multiplexed in this module to send a single digit at a time using control signals as declared briefly in Figure-11. In the same time, the selected digit to be sent

will be in the ASCII form in order to be viewed on the LCD.

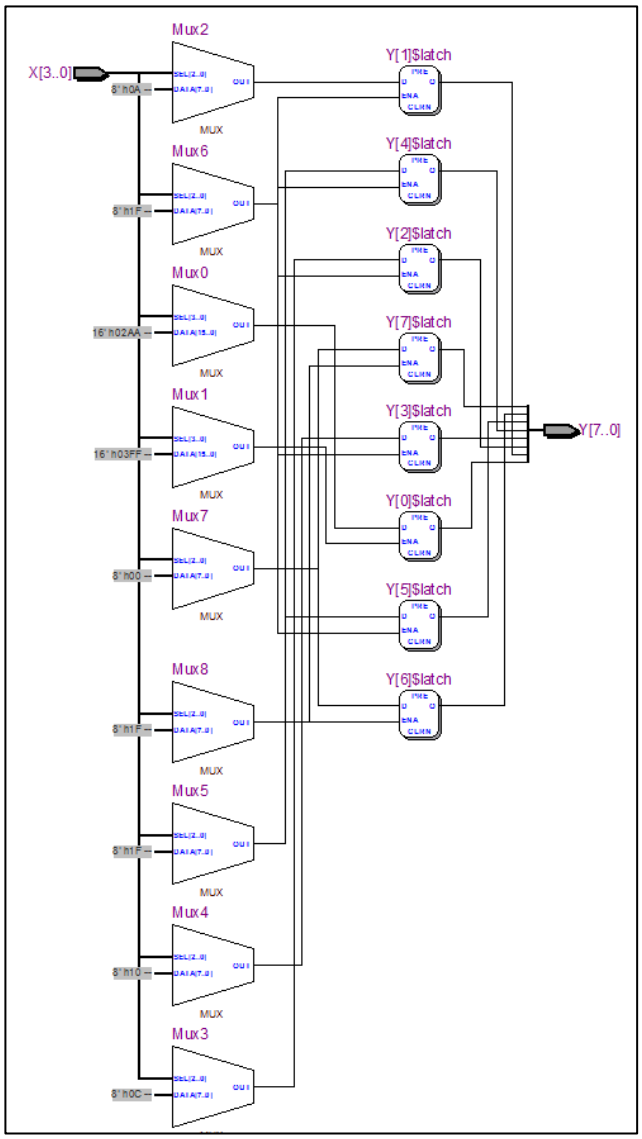

Figure-11. Distribution module.

The initial step in this module is to make the output be in the high impedance state (Z) such that only one entity writes to the bus. Next step is to control which BCD-digit will be sent to the LCD view unit and this was done via two control signals. At each state of the 6-states of the control signals, only one digit will be assign to a temporal signal. Now, the selected digits at each state of the temporal signal will be assigned to the final output but in the ASCII form and not in the BCD form.

RESULT AND EVALUATION

The modules were tested and the results are obtained via the vector waveform tool which presents primary idea about the results of each module as well as proving that the modules are performing the right functions. Via one of the Quartus II software features which is the waveform tool, it can simulate the designed modules to have a clear idea about the results obtained from each module individually until the system overall performance presented using the DE1-SOC board. The summary of each module components also presented in this volume to declare the used resources for each module. The results obtained via the frequency detection module for the signals (25 KHz, 50 KHz, 90 KHz, and 166 KHz) are shown below respectively:

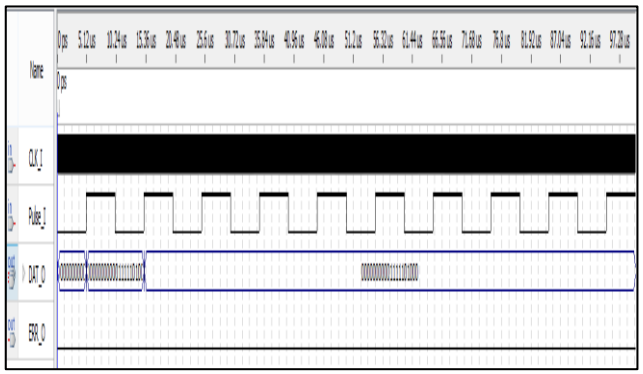

Figure-12. The detected frequency for the input signal 50 KHz.

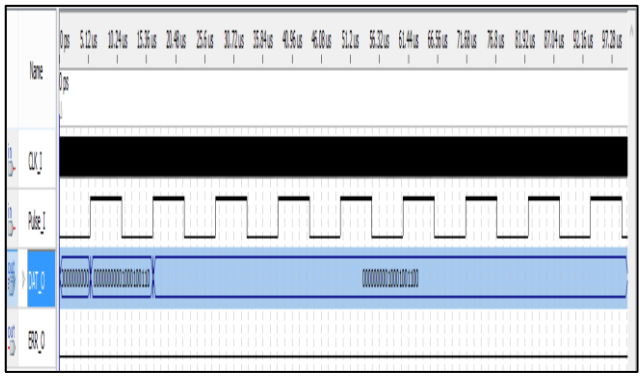

Figure-13. The detected frequency for the input signal 90 KHz.

Table-1 presents a brief view about the binary representation for each result obtained from this module.

Table-1. Frequency capturing calculations.

FRQ.	Pulse	bits	pulse, width (ns)
50000	1000	00000000001111101000	20
90000	2000	00000000010001001100	20

As can be seen from the Figures 12, 13, the results are in the binary form, and they are converted into the BCD form. Figures 16, 17, 18 and 19 show the signal conversion module bits' stream.

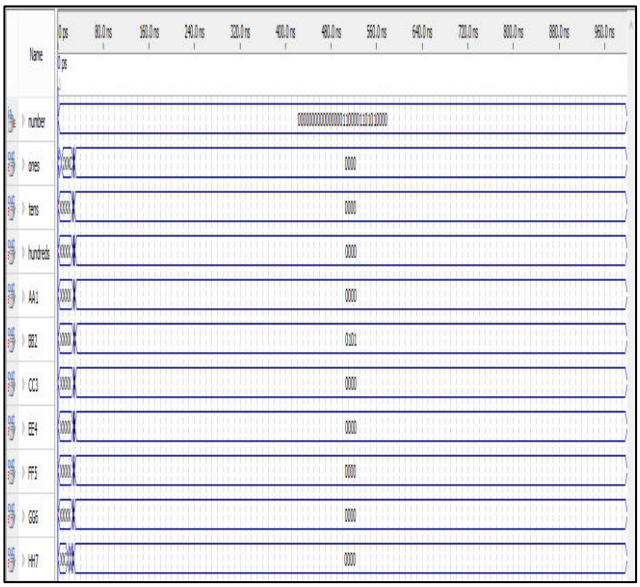

Figure-14. Binary coded decimal representation for signal.

Table-2. BCD representation of signal 50000 kHz.

Signals									
Binary	Decimal	Binary coded decimal							
		FF5	EE4	CC3	BB2	AA1	hundred	tens	Ones
00000000000000001100001101010000	50000	0000	0000	0000	0101	0000	0000	0000	0000

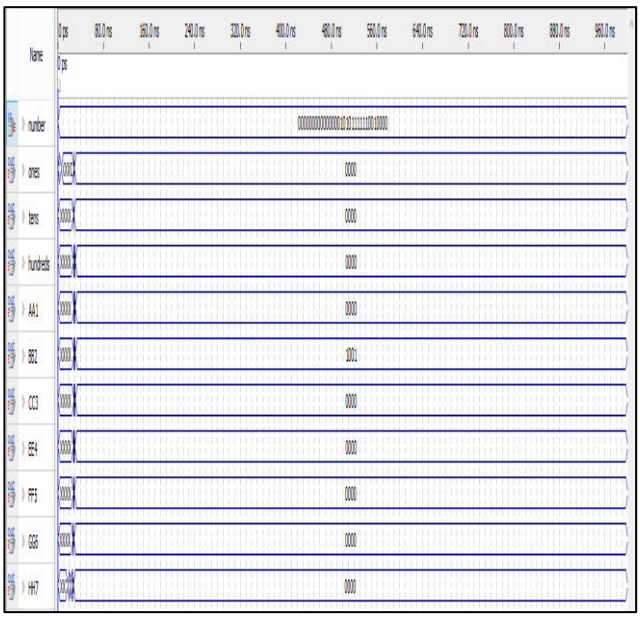

Figure-15. Binary coded decimal representation for signal.

Table-3. BCD representation of signal 90000 kHz**.**

Signals									
Binary	Decimal	Binary coded decimal							
		FF5	EE4	CC3	BB2	AA1	hundred	tens	Ones
00000000000000010101111110010000	90000	0000	0000	0000	1001	0000	0000	0000	0000

The results above were all obtained during the verification phase via the Altera CAD tool Quartus II web edition software. For the results which have been shown over the LCD and Seven segment using (DE1-SoC) and (DE2-115), all will be illustrated in this section:

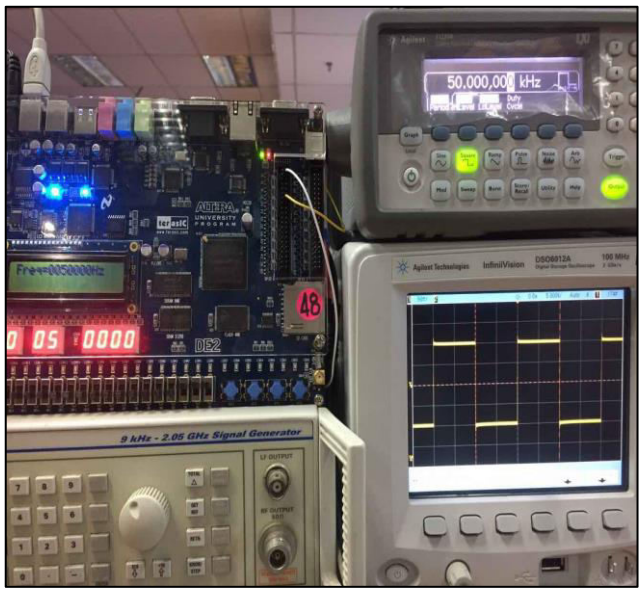

Figure-16. System outcome for the input (50000Hz) on DE2.

Figure-17. System outcome for the input (50000Hz) on DE1-SoC.

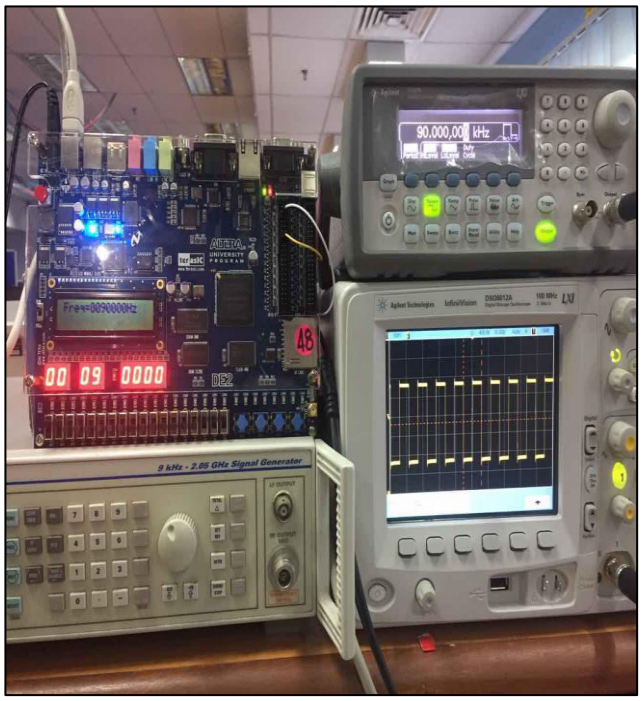

Figure-18. System outcome for the input(90000Hz) on DE2.

Figure-19. System outcome for the input (90000Hz) on DE1-SoC.

CONCLUSIONS

The project objectives have been successfully, a study of on how to perform jamming for the emitted frequencies and Decreased system overall complexity level, improved operating frequency, consumed chip resources, and improved throughput. Speed up the processing time, increase the processing cores utilities, and reduce the delay occurring in the processing modules. Implementing this scheme on FPGA has been investigated. It started from the frequency detection itself background, which is based on how to detect the pulses within the signal. Many features within the Altera® Cyclone V have been harnessed to implement this project such as the LCD and seven segments alongside with the switch inputs and LEDs. A quantum leap was associated with the system performance when applying the unique characteristics of FPGA chip and true parallelism principle over the system. The FPGA chip provides abilities such as flexibility, reliability and configurability to the system. Considering the obtained results, it can be clearly concluded that applying the true parallelism principle allowed the system modules to process multiple data each time to give multiple outputs, which reduced the entire complexity of the system as well as increased utilisation of the modules.

Based on the results as declared, the performance of the system was seen to increase with the exploitation of DE1-SoC board in many aspects in terms of speed and the flexibility in implementing the design, whereas the desired results could be achieved with the DE1-SoC even if the input signals were disturbed by a noise. Total registers were 5,180 and total logic elements were 5,032. To enable the system to cover a wide spectrum of signals with high-accuracy computing process, the Phase Locked Loop up to 1.6 GHz was adjusted. The research results demonstrated that real-time processing of multiple signals could be done simultaneously and it could be concluded that the true parallelism could be a solution option for those embedded systems requiring real-time processing feature. Moreover, it was common for many embedded systems facing real challenges due to constraints over system resources such as the power consumption, allowed memory size within the system and speed. Considering all these and other factors, the FPGA chip was chosen as the hardware platform for addressing these issues.

Lastly, it needs mentioning here that the proposed laser missile frequency jamming system's hardware design, the system's high throughput in identifying the frequencies (as confirmed through the results), and processing these frequencies for sending them to the defused platforms as well as to be shown on the seven-segment and LCD, all these were done with low utilisation of hardware resource.

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