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DESIGN AND ANALYSIS OF A SEPIC CONVERTER FOR PV APPLICATIONS

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ABSTRACT

This paper presents analysis and design of a SEPIC Converter. Operation of the single ended primary inductor converter (SEPIC) is analyzed, leading to mathematical expressions that can be used to design the converter. The SEPIC converter allows a range of dc voltage to be adjusted to maintain a constant voltage output. SEPIC converter is used to overcome the limitation of conventional buck boost converter like inverted output, pulsating input current, high voltage stress make it unreliable for wide range of operation. MATLAB simulation is being used to validate the method and show the effectiveness of the design.

Keywords: DC-DC converter, SEPIC converter.

1. INTRODUCTION

Circuits run best with a steady and specific input. Controlling the input to specific sub-circuits is crucial for fulfilling design requirements. AC-AC conversion can be easily done with a transformer; however dc-dc conversion is not as simple. Diodes and voltage bridges are useful for reducing voltage by a set amount, but can be inefficient. Voltage regulators can be used to provide a reference voltage. Additionally, battery voltage decreases as batteries discharge which can cause many problems if there is no voltage control. The most efficient method of regulating voltage through a circuit is with a dc-dc converter. There are 5 main types of dc-dc converters. Buck converters can only reduce voltage, boost converters can only increase voltage, and buck-boost, Cúk, and SEPIC converters can increase or decrease the voltage. A DC-DC converter with a high voltage gain is desirable in many modern applications, such as a front-end stage for fuel cell and solar cell, an HID lamp ballast for automobiles, and a power supply for computer servers in telecommunication industry.

Some applications of converters only need to buck or boost the voltage and can simply use the corresponding converters. However, sometimes the desired output voltage will be in the range of input voltage. When this is the case, it is usually best to use a converter that can decrease or increase the voltage. Buck-boost converters can be cheaper because they only require a single inductor and a capacitor. However, these converters suffer from a high amount of input current ripple. This ripple can create harmonics; in many applications these harmonics necessitate using a large capacitor or an LC filter. This often makes the buck-boost expensive or inefficient. Another issue that can complicate the usage of buck-boost converters is the fact that they invert the voltage. Cúk converters solve both of these problems by using an extra capacitor and inductor. However, both Cúk and buck-boost converter operation cause large amounts of electrical stress on the components, this can result in device failure or overheating. SEPIC converters solve both of these problems.

2. ANALYSIS OF SEPIC

2.1 Operation of SEPIC converter

The Schematic diagram for a basic SEPIC is shown in Figure-1. The SEPIC converter exchanges energy between the capacitors and inductors in order to convert from one voltage to another. The amount of energy exchanged is controlled by switch S1, which is typically a transistor such as a MOSFET. MOSFETs offer much higher input impedance and lower voltage drop than BJT, and do not require biasing resistors as MOSFET switching is controlled by differences in voltage rather than a current, as with BJTs.

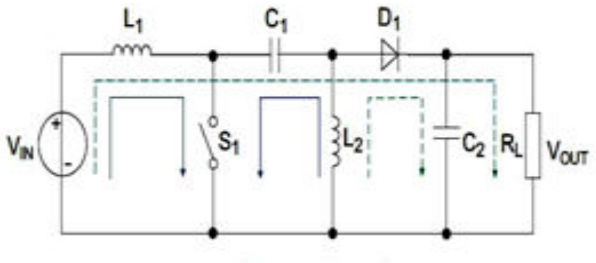

Figure-1. Schematic of SEPIC converter.

--------- Current flow, S_1 open
_____ Current flow, S_1 closed

When switch S1 is turned on, current I_{L1} increases and the current I_{L2} goes more negative. (Mathematically, it decreases due to arrow direction.) The energy to increase the current I_{L1} comes from the input source. Since S1 is a short while closed, and the instantaneous voltage V_{L1} is approximately V_{IN}, the voltage V_{L2} is approximately $-V_{C1}$.Therefore, the capacitor C1 supplies the energy to increase the magnitude of the current in I_{L2} and thus increase the energy stored in L2.

When switch S1 is turned off, the current IC1 becomes the same as the current IL1, since inductors do not allow instantaneous changes in current. The current IL2 will continue in the negative direction, in

fact it never reverses direction. It can be seen from the diagram that a negative I_{L2} will add to the current I_{L1} to increase the current delivered to the load. Using KCL it can be shown that $I_{D1} = I_{C1} - I_{L2}$. It can then be concluded, that while S1 is off, power is delivered to the load from both L2 and L1. C1, however is being charged by L1 during this off cycle, and will in turn recharge L2 during the on cycle.

Because the potential (voltage) across capacitor C1 may reverse direction every cycle, a non-polarized capacitor should be used. However, a polarized tantalum or electrolytic capacitor may be used in some cases, [2] because the potential (voltage) across capacitor C1 will not change unless the switch is closed long enough for a half cycle of resonance with inductor L2, and by this time the current in inductor L1 could be quite large.

The capacitor C_{IN} is required to reduce the effects of the parasitic inductance and internal resistance of the power supply. The boost/buck capabilities of the SEPIC are possible because of capacitor C1 and inductor L2. Inductor L1 and switch S1 create a standard boost converter, which generates a voltage (V_{S1}) that is higher than V_{IN}, whose magnitude is determined by the duty cycle of the switch S1. Since the average voltage across C1 is V_{IN}, the output voltage (V_O) is $V_{S1} - V_{IN}$. If V_{S1} is less than double V_{IN}, then the output voltage will be less than the input voltage. If V_{S1} is greater than double V_{IN}, then the output voltage will be greater than the input voltage.

2.2 Design calculation of SEPIC converter

a) Duty cycle consideration

For a SEPIC converter operating in a continuous conduction mode (CCM), the duty cycle is given by:

$$D = \frac{Vout+VD}{Vin+Vout+VD} \quad [1]$$

Where, V_D is the forward voltage drop of the diode D1. The maximum duty cycle is:

$$Dmax = \frac{Vout+VD}{VIN\ (min)+Vout+VD} \quad [2]$$

b) Inductor selection

A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 40% of the maximum input current at the minimum input voltage. The ripple current flowing in equal value inductors L1 and L2 is given by:

$$\Delta I_L = I_{IN} \times 40\% = I_{OUT} \times \frac{Vout}{Vmin} \times 40\% \quad [3]$$

The inductor value is calculated by

$$L1 = L2 = L = \frac{Vin\ (min)}{\Delta I_L\ f_{sw}} \times Dmax \quad [4]$$

fsw is the switching frequency and Dmax is the duty cycle at the minimum Vin. The peak current in the inductor, to ensure the inductor does not saturate, is given by:

$$I_{L1}\ peak = I\ out \times \frac{Vout+VD}{Vin\ (min)} x\ (1 + \frac{40\%}{2})$$
$$I_{L2}\ peak = I\ out \times\ (1 + \frac{40\%}{2}) \quad [5]$$

If L1 and L2 are wound on the same core, the value of inductance in the equation above is replaced by 2L due to mutual inductance. The inductor value is calculated by:

$$L_1^1 = L_2^1 = \frac{L}{2} = \frac{Vin(min)}{2x\Delta I_L x f_{sw}} x\ Dmax \quad [6]$$

c) Power MOSFET selection

The parameters governing the selection of the MOSFET are the minimum threshold voltage Vth(min), the on resistance RDS(ON), gate-drain charge QGD, and the maximum drain to source voltage, VDS(max). Logic level or sub logic-level threshold MOSFETs should be used based on the gate drive voltage. The peak switch voltage is equal to Vin + Vout. The peak switch current is given by:

$$I_{Q1}\ (peak) = I_{L1\ (peak)} + I_{L2\ (peak)} \quad [7]$$

The RMS current through the switch is given by:

$$I_{Q1\ (rms)} = I_{OUT} \sqrt{\frac{(V_{OUT} + V_{IN\ (min)} + V_D) \times (V_{OUT} + V_D)}{V^2_{IN\ (min)}}}$$

The MOSFET power dissipation PQ1 is approximately:

$$P_{Q1} = I^2_{Q1(max)} \times R_{DS(ON)} x D_{max} + V_{IN(min)}$$
$$+V_{out} \times I_{Q1(peak)} x\ \frac{QGD \times fsw}{IG} \quad [8]$$

P_{Q1}, the total power dissipation for MOSFETs includes conduction loss (as shown in the first term of the above equation) and switching loss as shown in the second term. IG is the gate drive current. The RDS (ON) value should be selected at maximum operating junction temperature and is typically given in the MOSFET data sheet. Ensure that the conduction losses plus the switching losses do not exceed the package ratings or exceed the overall thermal budget.

d) Output diode selection

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current IQ1 (peak). The minimum peak reverse voltage the diode must withstand is:

$$V_{RD1} = V_{IN(max)} + V_{out(max)} \quad [9]$$

Similar to the boost converter, the average diode current is equal to the output current. The power dissipation of the diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diodes are recommended in order to minimize the efficiency loss.

e) SEPIC coupling capacitor selection

The selection of SEPIC capacitor, Cs, depends on the RMS current, which is given by

$$I_{cs(rms)} = I_{OUT} \times \sqrt{\frac{Vout+VD}{Vin(\min)}} \quad [10]$$

The SEPIC capacitor must be rated for a large RMS current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum and ceramic capacitors are the best choice for SMT, having high RMS current ratings relative to size. Electrolytic capacitors work well for through-hole applications where the size is not limited and they can accommodate the required RMS current rating. The peak-to-peak ripple voltage on Cs (assuming no ESR):

$$\Delta Vcs = \frac{IOUT \times Dmax}{Cs \times fsw} \quad [11]$$

A capacitor that meets the RMS current requirement would mostly produce small ripple voltage on Cs. Hence, the peak voltage is typically close to the input voltage.

f) Output capacitor selection

In a SEPIC converter, when the power switch Q1 is turned on, the inductor is charging and the output current is supplied by the output capacitor. As a result, the output capacitor sees large ripple currents. Thus the selected output capacitor is,

$$Cout\ (rms) = I_{OUT} \times \sqrt{\frac{Vout+VD}{V\ in\ (\min)}} \quad [12]$$

The ESR, ESL, and the bulk capacitance of the output capacitor directly control the output ripple. As shown in Figure-4, assume half of the ripple is caused by the ESR and the other half is caused by the amount of capacitance. Hence,

$$ESR \leq \frac{V\ ripple\ x\ 0.5}{IL1(peak)+Il2\ (peak)} \quad [13]$$

$$C_{out} \geq \frac{I\ OUT\ x\ D}{V\ ripple\ x\ 0.5\ xfsw} \quad [14]$$

The output cap must meet the RMS current, ESR and capacitance requirements. In surface mount applications, tantalum, polymer electrolytic, and polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

g) Input capacitor selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$ICin\ (rms) = \frac{\Delta IL}{\sqrt{12}} \quad [15]$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 µF or higher value, good quality capacitor would prevent impedance interactions with the input supply.

3. SIMULATION RESULTS

The open loop SEPIC converter is analyzed and the circuits are given in Figures 2 and 3 and 4.

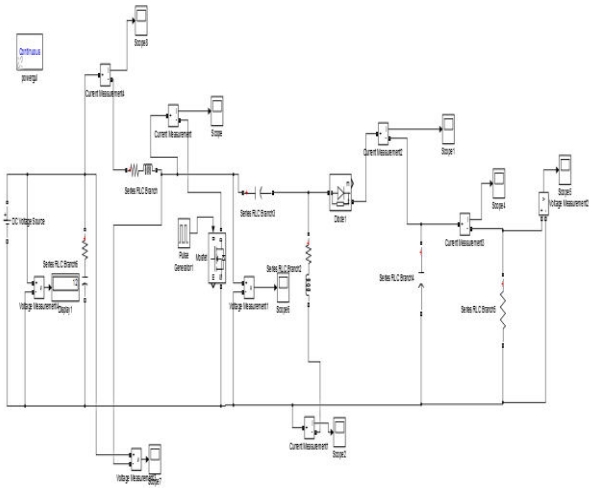

Figure-2. Open loop simulation of SEPIC converter.

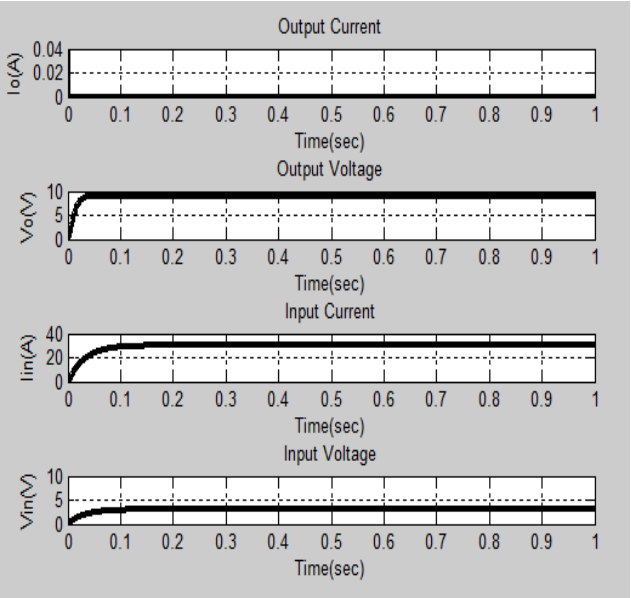

Figure-3. Simulation result for proposed SEPIC converter.

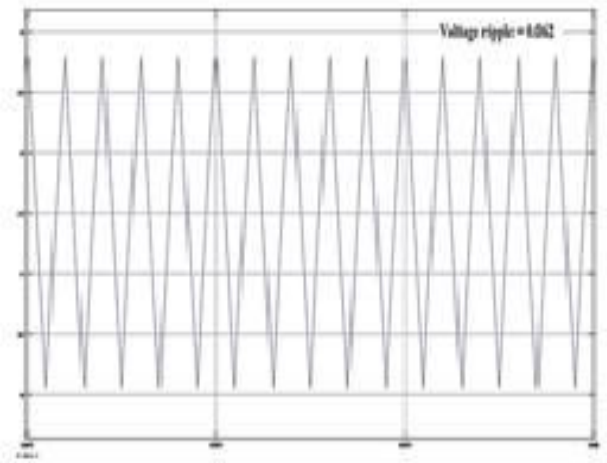

Figure-4. Output voltage ripple of SEPIC converter.

4. CONCLUSIONS

The analysis and simulation of SEPIC converter has been carried out using MATLAB. The resistances in the inductors and the capacitors can also have large effects on the converter efficiency and ripple. Inductors with lower series resistance allow less energy to be dissipated as heat, resulting in greater efficiency (a large portion of the input power being transferred to the load). It is hoped that these techniques will contribute to future development of low-power converters operating over wide ranges and extreme high frequencies to meet the increasing demands of modern portable electronics for PV applications.

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