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HIGH PERFORMANCE DATA AWARE (HPDA) SRAM CELL FOR IOT APPLICATIONS

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ABSTRACT

Low power and high performance of static random access memory (SRAM) are the main key issues and has become vital components in modern VLSI systems.The system power, performance and reliability can be significantly improved by controlling the power dissipation in SRAM. In this paper, the new technique is introduced in the High Performance Data Aware (HPDA) SRAM design to reduce the power dissipation and access delay for read/write operation. The proposed new technique employed in the HPDA SRAM cell has proved to minimize the write power dissipation about 83% and read power consumption about 50%than the 6T cell. The read access time and stability of the HPDA cell are also improved in the new design SRAM cell.

Keyword: SRAM cell, power, performance, standby mode, leakage current, SNM.

1. INTRODUCTION

Memory content in System-on-Chip (SoC) was increasing dramatically over the last 10 years.

Internet-of-Things (IoT) applications in portable devices require an enormous amount of memory to store and process the data.Due to requirement of the portable devices and larger battery life span, new on-chip memory implementations must be found to improve energy efficiency for SoC design andthe chip's area. The power-efficiency, performance, reliability and overall cost of the system design can be improved significantly by controlling the power dissipation in memories. Reducing the power dissipation in a chip doesn't only increase the battery's life span, but it also decreases the chip's failure rate. The portable gadgets such as smart phones, PDAs, WSN and other mobile appliances are becoming part and parcel in every aspect of our daily life. Mobile devices are fascinating and highly attractive with various significant improvements day by day in every new release demanding the sustainability and success of the device [2]. There is continuously increasing higher demand in fixed memory access in video, audio and image implementations affect its consumption of power and battery lifetime to reach its limitation. In most of the battery operated appliances and tools, power dissipation has become a main consideration and an important aspect [3, 4].Low power and high speed SRAM cells are being consistently designed and evaluated to meet the constant industry requirements with respect to the latest developments of VLSI circuits [1,2].The reduction of power consumption is essential for both read/write operations of cache memory. Many researchers have concentrated on minimizing the power consumption either for write operation or for read operation [3-7].The existing ZA [3] and 7T [4] SRAM cells have proved to minimize the write '0' power. But, theextra signal influences a significant hardware burden in these cells.The feature size is drastically reduced in the same pace together with the threshold and supply voltage in the latest technologies. Though the supply voltage and power consumption are decreased proportionally, the respective speed and static noise margin (SNM) are degraded. There were many SRAM cells proposed earlier [7-10] to improve the SNM.

We have proposed a new High Performance Data Aware (HPDA) cell in this paper. To enhance performance andstability, the proposed SRAM is designed with two circuits for read and write operations. The latch circuit is disconnected to switch the data quicker on the nodes and the lower discharging activity at the bit lines causes low power consumption during write mode. The other sections are organized as follows. The architecture of the proposed cell is explained in section 2. In section 3, the simulation results and comparisons are discussed. The conclusion is given in section 4.

2. PROPOSED HPDA SRAM DESIGN

The aim of this proposed HPDA cell is to decrease the power consumption without any tradeoffbetween the read access time and stability. The HPDA cell is designed using eight transistors with a separate read circuit. The architecture of HPDA cell is shown in Figure-1 which consists of two inverters; inverter invL, uses transistors P1 and N1, and inverter invR, uses transistors P2 and N2. Access transistors N3 and N4 are used to connect nodes QB and Q with bit-lines BL and BLB. The WL1, WL2, WS and W signals are used to perform write mode in the HPDA cell. Signal W is set to low during the write mode which breaks the feedback connection of the cell so that data can be transferred on the nodes QB and Qfaster. To improve the cell's read stability the read operation is performed through a separate read circuit which consists of transistor N6. The read pass-transistor N6 is controlled by RWL. During read and hold mode, W is set to high to store the latch property of the cell. The isolation of the nodes from bit-lines during hold/read improves the SNM of the cell.

Write mode: In the write mode, N5 transistor is used to disconnect the feedback connection of the inverters and the cell performs as a dynamic

cell.Switching of the data at the nodes is easy due to the dynamic nature of the cell. Once the data is set on the bit-lines (BL/BLB), the Word line WL1 or WL2 is asserted to high.The bit-line (BL or BLB) charging/discharging activity is controlled by the WL1/WL2 and WS signals.The WS signal plays a major role instead of WL1/WL2 to enhance the write ability. In order to write "1", BL is set to high, set WS=1 and then assert WL1=V_{DD}. Therefore, the transistor P2 is turned off as shown in Figure-2, hence the connection exists between the ground and QB so that the voltage at QB=0 without allowing BLB to discharge. To write "0", BLB is set to high, set WS=0 and assert WL2=$V_{DD.}$ Therefore, thetransistor N2 is turned off as shown in Figure-1, hence there is no connection exists between node QB and ground so that the voltage at node QB=1 without allowing BL to discharge.With the influence of WL1/WL2 and WS signal, bit-lines (BL/BLB) discharging activity are minimized so that the active power consumption is considerably saved as well as write performance is improved.

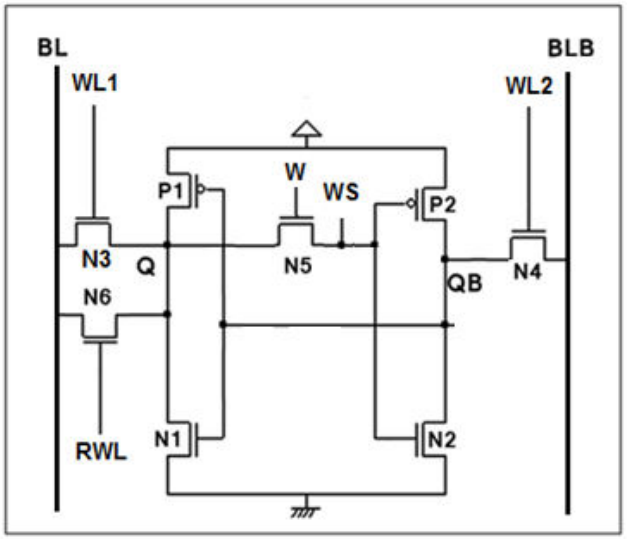


Figure-1. HPDA SRAM cell.

Read operation: For the read mode, WL1/WL2=0 and W=1 and assert RBL to V_{DD}. Transistors N6 and N1 comprise the read circuit as shown in Fig.1. The transistor N1 is controlled by node QB and then asserting RWL to high. The read operation is performed now.

In read '1' operation, the stored data at Q = 1(QB=0)N1 is OFF, flips the node Q to high, results minimum power dissipation. When Q stores data '0', N6 turns ON. Transistor N1 connects the read path to the ground. Since, nodes Q and QB are fully isolated from bit lines during read operation; the voltage of the node which stores '0' is strictly maintained at the ground level.

3. RESULT AND DISCUSSIONS

The HPDA SRAM cell's simulation results are analyzed in terms of power consumption, area, read/write delay and SNM by using 65nm CMOS technology and presented in the section. Due to bit-lines discharging activity of the 6T cell, the write power dissipation is high. In contrast, the 7T cell [4] uses thesingle bit-line and thus the power is saved during write "0" operation than the write "1" operation. In the proposed HPDA SRAM cell, any one of the bit-line (BL/BLB) discharging activity is prevented and thus saves power as well as delay considerably during write "1" and write "0" operations as shown in the Tables 1(a) and 1(b).

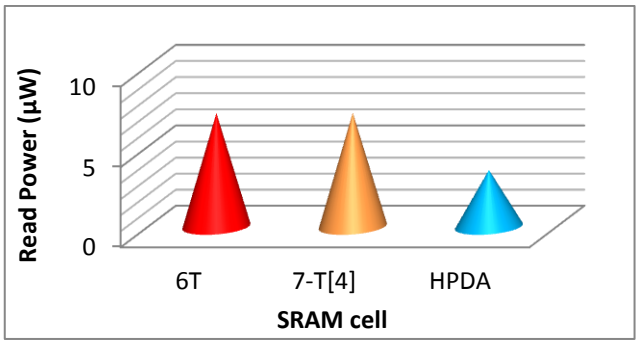
Table-1. (a) Write power for different input and (b) Access time.

(a)

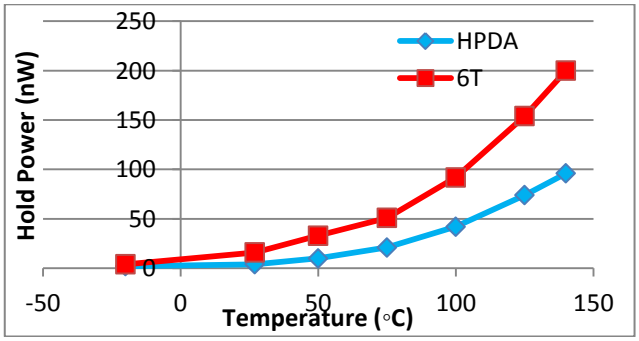
Write Power consumption (µw)			
Transitions	**6T**	**7T**	**HPDA**
0->1	4.938	5.073	0..844
1->1	0.017	0.018	0.004
1->0	4.944	0.987	0.793
0->0	0.016	0.004	0.004

(b)

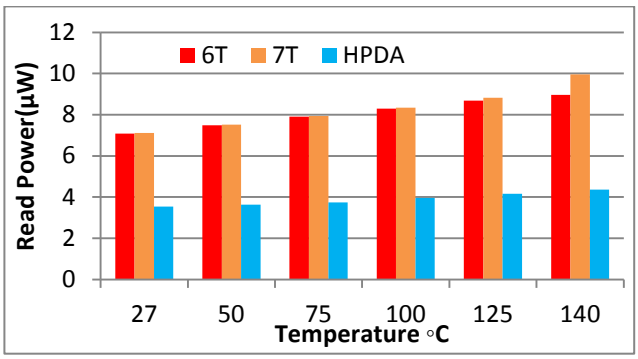
SRAM cell	**Read delay** *(ps)*		**Write delay** *(ps)*	
	Read '0'	**Read '1'**	**0→1**	**1→0**
6T	80	80	128	128
7T [6]	80	91	62	136
HPDA	81	16	32	32



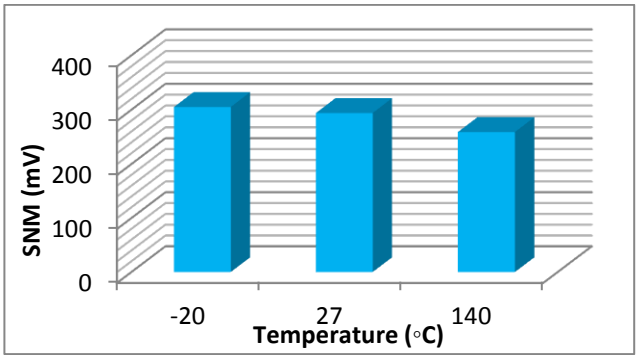
(a)



(b)



(c)

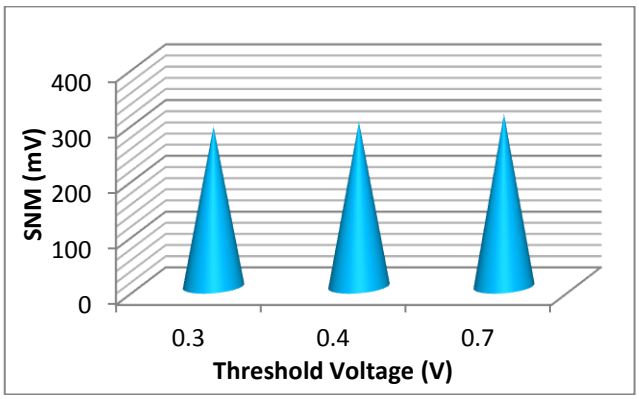


(d)

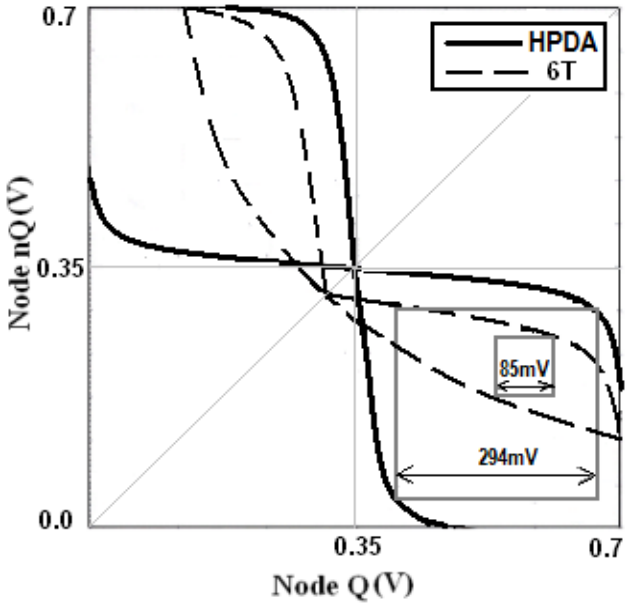
Figure-2. (a) Read power (b) Read power withtemperature,(c) Read power with temperature and (d) Static noise margin.

The transistor N1 turns off during the read "1" operation (Q=1 & QB=0). Therefore, there is no discharging read path which reduces the power consumption. The BL discharges through transistors N6 and N1 during the read "0" operation (Q=0& QB=1). Due to the low BL voltage reduction on the bit-line, the average read power is reduced about 50% compared to other cells as highlighted in Figure-2(a) and also the average read speed is faster than the 6T cell.

The HPDA cell can be applied even in worse condition (T=137^{0}C) with minimum power loss (Figure-2(b)).Due to the seperate of write and read circuits and absence of leakage paths, there is a small variation in the read power consumption.The HPDA cell is suitable for low power cache design because of its hold power is less even at 137^{o}Cas shown in Figure-2(c). The Static noise margin of the HPDA cell varies with different threshold voltage as well as different temperaturesare depicted in Figure-2 (c) and (d).Due to the separate read circuit, the read SNM is 2.45x higher than the 6T cell as seen Figure-3(a).As the temperature increases from 27^{o}C to 137^{o}C, the SNM value decreases about 15% (Figure-2(d)). Due to low leakage current in the HPDA cell, there is a slight variation in SNM with Vth.



(a)



(b)

Figure-3. (a) SNM for different threshold voltage (b) Static noise margin.

4. CONCLUSIONS

The HPDA SRAM cell has proved to minimize the write power about 83% and read power about 50% compared to the conventional cell. By decoupling feedback link of the two inverters, the discharging activity is minimized at the write bit line and saves dynamic power in the cell.The isolated write and read ports in the cell enhances the read stability as well as restrict the leakage current in the cell which results in lower power consumption with temperature during hold mode and read operation. The HPDA cell is an attractive choice for IoT applications due to lower power dissipation and leakage current.

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