A NOVEL DUAL ELECTRODE AND GATE ENGINEERED DOPING-LESS TFET FOR PERFORMANCE ENHANCEMENT

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ABSTRACT

Tunnel FET (TFET) is a promising device for ultra-low power applications because it has the benefits of band to band tunneling (BTBT) behavior of operating mechanism and achieving the sub-threshold swing (SS) value of less than 60mV/dec. However, it suffers from low ON state current and ambipolar in nature. In addition, it also has poor analog/RF performances. To address these problems, a novel dual electrode and a double metal gate Doping-less TFET (DE-DMGDLTFET) is proposed in this work by using charge plasma technique. To improve the BTBT rate and ON-state current, a tunneling gate length (L_{tg}) of proper work function is created at the source-channel junction. The distance between the source and gate electrode (L_{gs}) is kept at a minimum of 2 nm significantly, to reduce the ambipolar behavior. To enhance the analog/RF performance, a dual electrode structure is proposed on both sides of source and drain regions to induce the carriers uniformly. By using Silvaco TCAD simulator, different n-type DLTFET structures are designed and compared. The overall DC and analog/RF performance of all the DLTFETs are investigated. The proposed DE-DMGDLTFET achieved a higher ON current of 5.26 x 10^{-7} A/µm at V_{gs} and V_{ds} =0.5 V, SS of 30.27 mV/dec, Cut-off frequency range from MHZ to GHz and suppress the ambipolar order of 10^{10} effectively.

Keywords: tunnel FET, band to band tunneling, sub-threshold swing, doping-less charge plasma.

INTRODUCTION

With the technology scaling is moving towards nanometer regime, CMOS is facing a major problem of short channel effects. Alternate to CMOS, TFETs are becoming more attractive in recent years because of its high-energy efficiency and better switching performance even at a reduced voltage level [1], [2]. Besides, in principle, it obeys the band to band tunneling movement of electrons in the source-channel junction which creates more immune to short channel effects eg. Threshold voltage V_T rolls off [3]. It can able to achieve a steeper sub-threshold slope with a SS of less than 60 mV/dec with very less off state leakage current (in femto amperes) [4]. Despite these merits due to quantum-mechanical tunneling in conventional Si-TFET, it has suffered with limited low ON-state current owing to the indirect and large energy gap [5]. There are lots of methods that can be used to solve it, for instance- by using III-V low band gap materials [6], hetero-gate dielectric [7], dual material gate [8], strain engineering [9], nanowires [10], high-k dielectric and gate stacking [11]. However, all these methods in the nano-scale region requires a stringent complex fabrication process with high thermal budget [12], [13] because it needs an expensive thermal annealing technique and ion implantation process for the formation of abrupt junctions, which is very essential for tunneling in TFETs. In fact, the effect of random dopant fluctuations becomes significant in aggressive scaled TFET, which affects the transistor performance and produces a huge increase in the OFF state current.

To overcome the above problems, recently Doping less TFET (DLTFET) is proposed in which drain and source regions are formed over the intrinsic silicon body due to the charge plasma (CP) technique without the need of doping [14], [15]. The first CP technique was initially proposed in P-N junction [16], later it was extended to MOSFETS, BJTS and TFETs [17], [18]. According to this technique, metal electrodes with suitable work function Φ (eV) are chosen to induce p+ source and n+ drain regions instead of conventional doping, ion implantation and thermal annealing techniques. Hence the effect of random dopant fluctuation effect is highly suppressed in CP technique. Conversely, it is suffered from low ON-state current, poor RF performance and high ambipolar nature of conduction. From the literature review, it is noted that all previous works related to the design of DLTFET mainly used different gate misalignment structure [19], hetero gate dielectrics [20], different metal work function (Φ) placed either on drain or source electrodes [21] to suppress the ambipolar behavior and improve the analog/RF performances. Alternately, in this research, the proposed shape and space gap modulated between source, drain and gate electrodes itself is able to suppress the ambipolar behavior. To improve the ON-current tunneling rate and DC performances, a tunneling gate length (L_{tg}) of different metal along with control gates structure is designed. Besides, the dual metal electrode is formed on both top and bottom of drain and source region, which will fully control the induced uniform holes /electrons to improve the analog performances. It also offers a very low gate to drain capacitances, which leads to improvement in the high-frequency response. Further, comparative characteristics of all the proposed DLTFET devices are discussed. The overall analog and RF performance parameters such as Transconductance (g_m), Transconductance to current ratio (g_m/I_d), Unity gain cut-off frequency (f_T) and Gain bandwidth product (GBP) are investigated in this work.

DEVICE STRUCTURE AND SIMULATION SETUP

According to CP concept, the metal electrodes with suitable work functions are deposited on intrinsic Si body, which can induce a P-type or N-type carrier-based source and drain regions at a desired level without doping.

To induce electron concentration using CP, the source and drain metal electrode work functions should be less than the intrinsic silicon by satisfying the equation:

$$\phi_m < X_{si} + \left(\frac{E_g}{2q}\right) \qquad (1)$$

Where ϕ_m is the work function of a metal electrode, X_{si} is the electron affinity of silicon (4.17 eV), E_g is the bulk silicon energy band gap and q is the charge of the electron. Similarly, the holes concentration can be induced only when the source/drain metal electrode work functions is greater than the intrinsic silicon by satisfying the equation:

$$\phi_m > X_{si} + \left(\frac{E_g}{2q}\right) \qquad (2)$$

Another requisite for CP is that the intrinsic Si film thickness should be less than the Debye length as shown in the equation (3) below. Where ϵ_{si} is silicon dielectric constant, V_T is the thermal voltage and N is the body carrier concentration

$$L_D = \sqrt{\frac{\epsilon_{si} V_T}{q.N}} \qquad (3)$$

Hence, there is no need of external doping to form a P+ and N+ source/drain regions. It also makes the fabrication process very simple and relaxed with low temperature budget requirements. The CP technique involves only the intrinsic film of different regions, which makes it relaxed from the effect of random dopant fluctuations with less leakage of current. After forming a P+ and N+ source/drain regions, the basic operating mechanism of TFET is based on BTBT. It involves tunneling of carriers from the valence band into the conduction band through the forbidden bandgap or vice versa. Here in this research; Platinum (Pt) metal with work function of 5.93 eV is used for the formation of p+ source region. The Hafnium (Hf) metal with work function of 3.9 eV is used for the formation of n+ drain region. The schematic presentation of different n-type DLTFET devices (a) Conventional Si doping less TFET (Si-DLTFET) (b) InGaN based doping less TFET (InGaN-DLTFET) (c) Dual Electrode InGaN doping less TFET (DE-DLTFET) (d) Dual Electrode and Double Metal Gate doping less TFET (DE-DMGDLTFET) considered in this work are shown in Figure 1(a) to 1(d). A common double gate structure which acts as a control gate with a metal work function of 4.5 eV (Chromium) is selected for all the DLTFET devices. To improve the BTBT across the source-channel junction, a tunneling gate length L_{tg} (7 nm) with different work function of 3.9 eV (Hafnium) is created in DE-DMGDLTFET as shown in Figure 1d (dark pink color). A high mobility and direct band gap feature of InGaN material is used as a body substrate instead of conventional Si (see Figure-1(b) to 1(d)). This will reduce the energy barrier at source-channel junction, which improves the BTBT rate and SS.
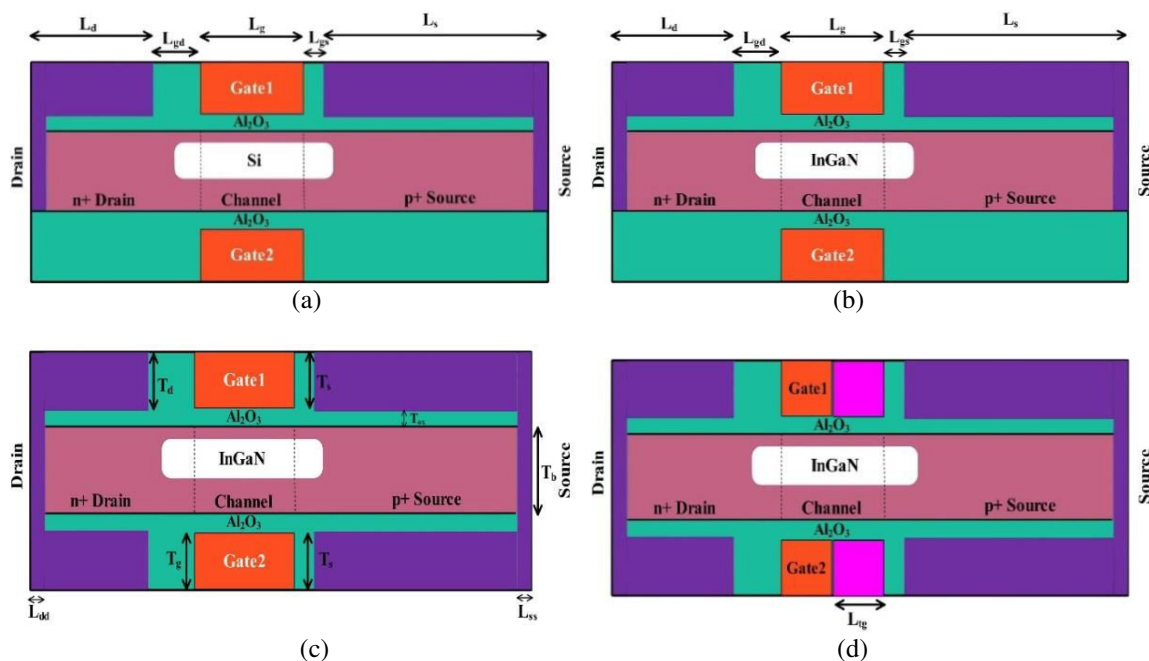

Figure-1. The cross sectional view of DLTFET devices (a) Conventional Si doping less TFET (Si-DLTFET) (b) InGaN based doping less TFET (InGaN-DLTFET) (c) Dual Electrode InGaN doping less TFET (DE-DLTFET) (d) Dual Electrode and Double Metal Gate InGaN doping less TFET (DE-DMGDLTFET) (proposed device).

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Table-1. Device design parameters used in the simulation.

Parameters	(Si-DLTFET)	(InGaN-DLTFET)	(DE-DLTFET)	(DE-DMGDLTFET)
Source length (L_s)	28 nm	28 nm	28 nm	28 nm
Drain length (L_d)	14 nm	14 nm	14 nm	14 nm
Gate length (L_g)	14 nm	14 nm	14 nm	7 nm
Tunneling gate length (L_{tg})	-	-	-	7 nm
Gap length between gate and drain (L_{gd})	6 nm	6 nm	6 nm	6 nm
Gap length between gate and source (L_{gs})	2 nm	2 nm	2 nm	2 nm
Drain, source contact length on body (L_{dd}&L_{ss})	2 nm	2 nm	2 nm	2 nm
Body thickness (T_b)	10 nm	10 nm	10 nm	10 nm
Source thickness (T_s)	7 nm	7 nm	7 nm	7 nm
Gate thickness (T_g)	7 nm	7 nm	7 nm	7 nm
Drain thickness (T_d)	7 nm	7 nm	7 nm	7 nm
Oxide thickness (T_{ox})	2 nm	2 nm	2 nm	2 nm

Moreover, InGaN material has an advantage of reduced effective mass values of holes and electrons for tunneling when compared to Si. InGaN material of 10 nm body thickness and gate oxide material of Al_2O_3 with high K dielectric value of ε=9 are chosen in this study. The device design parameters used in the TCAD simulations for the proposed devices are shown in Table 1.To do an extensive simulation of our proposed DLTFET devices, Silvaco 2D Atlas device simulator is used in this work [22]. The overall simulation steps involved in this work is shown in Flow chart 1. The non-local BTBT model is employed in this simulation for modeling the tunneling process accurately as well as considering the spatial variation of energy band. The tunneling probability across the junction is calculated by using Wentzel-Kramers-Brillouin (WKB) method. Shockley-Read-Hall (SRH) generation and recombination model are adopted to include the effect of carrier recombination and account for the leakage currents. To account for the transfer of electrons and holes in the simulation, drift-diffusion transport model is considered. To incorporate the temperature-dependent carrier mobility, Lombardi constant voltage temperature (CVT) mobility is used. Since the body thickness of our proposed devices is more than 5 nm, the quantum transport model and band gap narrowing (BGN) is not considered in our work.

SIMULATION RESULTS AND DISCUSSIONS

DC performance analysis

To clearly understand the BTBT behavior of DLTFET, Energy band diagram is the best one to observe how the tunneling width distance is getting reduced. Figure 2(a) to 2(d) shows the valence band (VB) and conduction band (CB) energies of the devices considered in this work under the condition of both OFF (V_{gs} =0V & V_{ds}= 1V) and ON (V_{gs} =1V & V_{ds}= 1V) states. It is noticed that in OFF state; all the devices has high tunneling width distance between valence and conduction band due to the existing large potential barrier. Therefore, the tunneling probability of electrons moving from VB of source to CB of channel is very low. However, in ON state under positive gate bias, the CB and VB of channel are aligned with CB and VB of drain causing reduction in the tunneling width distance. Therefore, it provides a less potential barrier and more tunneling probability of electrons moving from VB of source to CB of channel is taken place. Compare to other devices (Figures 2(a) to 2(c)), the proposed DE-DMGDLTFET energy band diagram exhibits a lateral narrow gap tunneling distance at the source-channel junction (Figure 2(d)) because of the inclusion of extra tunneling gate on both sides. The dual electrode architecture at the bottom of source and drain region in DE-DLTFET and DE-DMGDLTFET also has an impact of increasing the tunneling rate.

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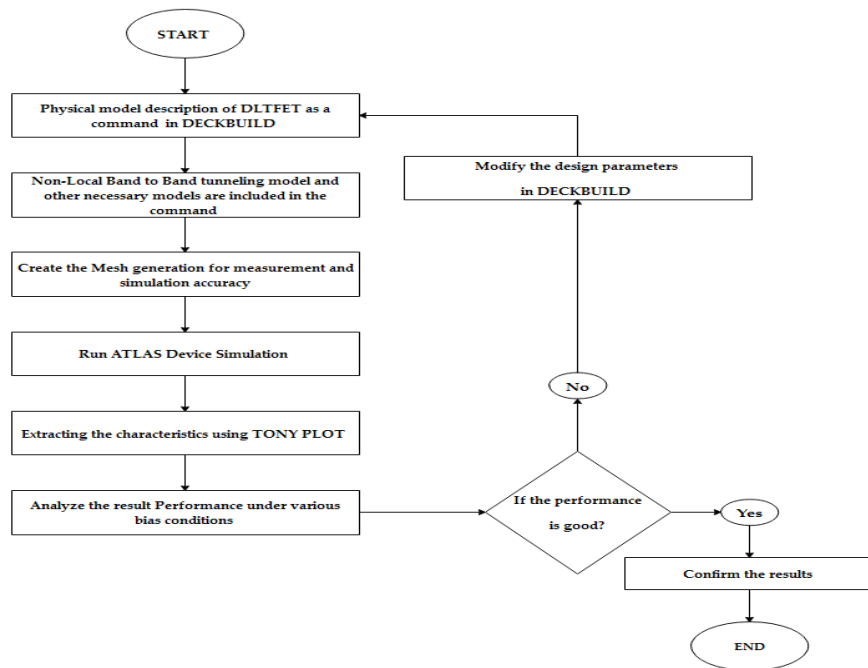
Flowchart-1. Overall simulation method involved in the design of DLTFET using Silvaco 2D Atlas.
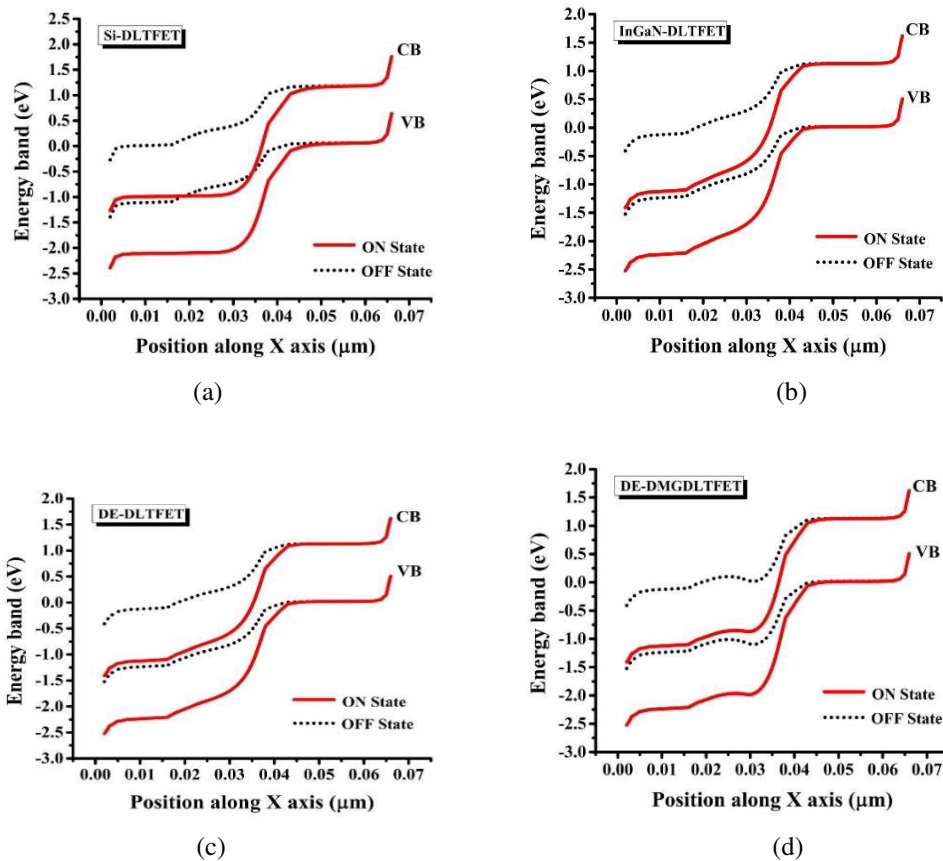

(a)

(b)

(c)

(d)

Figure-2. Energy band diagram of devices at OFF-state and ON state (a) Si-DLTFET (b) InGaN-DLTFET (c) DE-DLTFET (d) DE-DMGDLTFET (proposed device).

From Figure-3(a), it is observed that the proposed DE-DMGDLTFET is having a higher BTBT tunneling rate of 1.76×10^{31} electrons/cm-3 along the length of source-channel junction compared to other devices. We

need to observe the electron and holes concentration of carriers on a particular device to comprehend the dual electrode architecture. The Figure-3(b) shows the electron and hole concentration of DE-DMGDLTFET in thermal equilibrium state (Vgs =0V &Vds= 1V) and in ON state (Vgs =1V &Vds= 1V). It is noted that at ON-state, there is a constant value of approximately 1019 cm-3 holes concentration at source side and electron concentration at the drain side. This constant value is generated due to similar electrode structure at top and bottom (i.e.) the desired doping concentration can be achieved on both sides. But in the case of Si-DLTFET and InGaN-DLTFET, it is noted that there is no metal electrode at the bottom side so the carrier concentration created by the top metal electrode work function will be decreasing with an increase in distance. The higher BTBT rate achieved by the DE-DMGDLTFET indicates that it can increase the flow of drain current. Moreover, the impact of double metal gate with improved tunneling architecture on both sides in DE-DMGDLTFET induces an n+ pocket doped virtually at the source channel interface which also leads to achieve an increase in drain current. Hence DE-DMGDLTFET has obtained a high value of ON- drive current of 5.26×10^{-7} A/µm which is comparatively higher than 4.03×10^{-18} A/µm of Si-DLTFET at V_{gs} =0.5V &V_{ds}= 0.5V as shown in Figure-4(a).
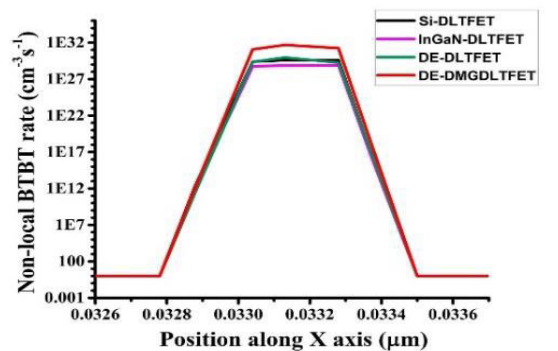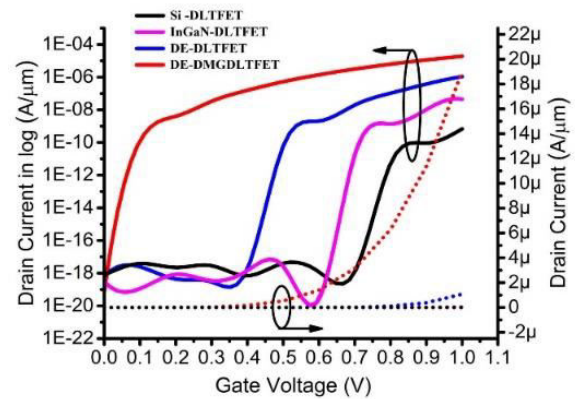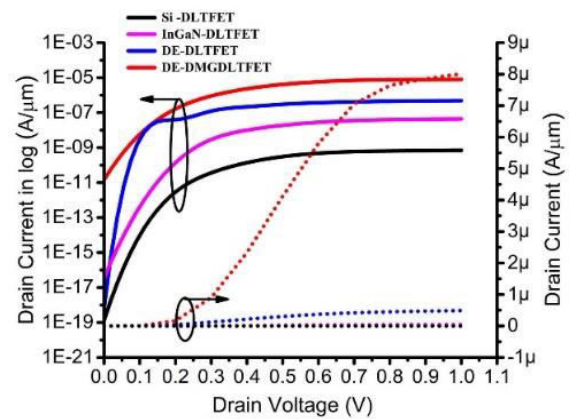

(a)
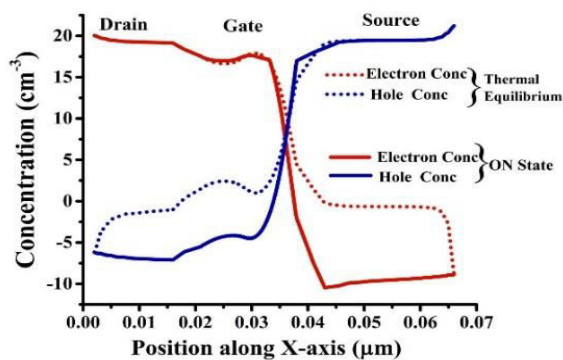
(b)

Figure-3. (a) BTBT rate of DLTFET devices (b) Electron and holes concentration of proposed DE-DMGDLTFET device

(a)

(b)

Figure-4. (a) Transfer characteristics I_d Vs V_{gs} (b) Output characteristics I_d Vs V_{ds}.

The ambipolar nature of current behavior is one, in which the device conducts the drain current even when the gate voltage is increased in positive as well as in negative direction. It can produce more OFF state leakage current, mainly in the drain channel junction.As shown in Figure-5, it is observed that we have obtained a reduced ambipolar current conduction at negative gate bias voltage from 0 V to -0.5 V. This is due to the proposed device size and space gap on drain channel and source channel interface. The size of the drain electrode (14 nm x 7 nm) is very small compared to the source electrode (28 nm x 7 nm) as shown in Figure 1. Besides, the space gap between source and gate electrode L_{sg} is kept a minimum of 2 nm whereas the space gap between drain and gate L_{dg} is kept at 6 nm. The combined effect of small size and more space gap L_{dg} on the drain-channel interface creates uplift of energy bands at the same interface. This will limit the tunneling of electrons from VB of channel to CB of drain under negative bias condition.
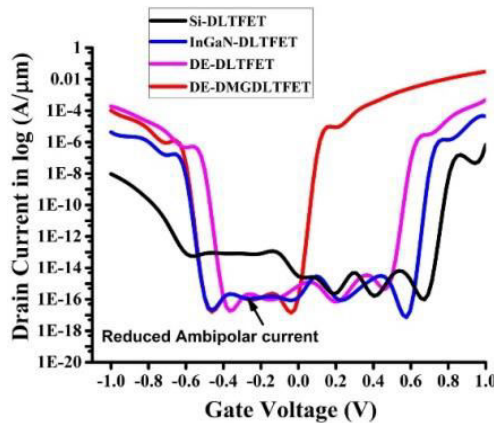
Figure-5. Characteristics of DLTFET devices with reduced ambipolar current at V_{gs} = 0 to -0.5V.

The calculated OFF current value of proposed DE-DMGDLTFET is very low as 6.92×10^{-20} A/µm. The calculated SS values of Si-DLTFET, In GaN-DLTFET, DE-DLTFET and DE-DMGDLTFET are 122.4, 92.96, 78.45 and 30.27 mV/decrespectively. The average SS of all the simulated devices are calculated by using equation (4)

$$SS = \frac{V_t - V_{OFF}}{Log\ I_{vt} - Log\ I_{OFF}} \qquad (4)$$

**Analog/RF performance analysis**

Analyzing the analog/RF response of DLTFET device is very essential when it is utilized at a circuit level. Transconductance (g_m) plays a vital role for the design of analog circuits such as operational transconductance amplifier (OTA) and operational amplifiers (OP-Amp). Transconductance (g_m) parameter signifies the amplification provided by the device. It is directly proportional to the gain of the circuit. The Transconductanc e (g_m) is calculated by equation (5).

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \qquad (5)$$

The value of g_m with the variation of V_{gs}, atV_{ds} = 1V for all the simulated devices is shown in Figure-6(a) (dotted line). As per equation (5), the value of g_m is directly dependent on the exponential increase in the value of drain current (I_d). The proposed DE-DMGDLTFET device has a good exponential increase in I_d with the variation of V_{gs} characteristics and it achieves a higher g_m value of 7.65×10^{-5} (S/µm) at V_{gs} =1V. Si-DLTFET has comparatively a lower g_m value of 6.6×10^{-7} (S/µm) due to its very low exponential characteristics of I_d. Hence, the higher value of g_m achieved by DE-DMGDLTFET is a suitable choice for analog amplification circuits. In the same Figure-6(a), the variation of Transconductance to current ratio (gm/Id) with an increase in Vgs is also shown. It represents the efficiency of the device to convert the bias current in to transconductance. This parameter is strongly related to analog performance (i.e.) higher gm/Id value ensures better amplification per unit drain current.

Moreover, the use of dual electrode and significantly an extra tunnel gate reduces the gate to source capacitances Cgs due to an increase in the electron concentration at the source channel interface. The combined effect of dual architecture and an extra tunnel gate makes the Cgs value to be quite low. Referring to the Figure-6(b), DE-DMGDLTFET has achieved a very low value of Cgd (in the range of 10-16 F/µm).

Other key parameters for high-frequency performances are evaluated by unity gain cut-off frequency (f_T) and gain band width product GBP. The f_T and GBP are computed by using the formulae shown in equation (6) and (7)
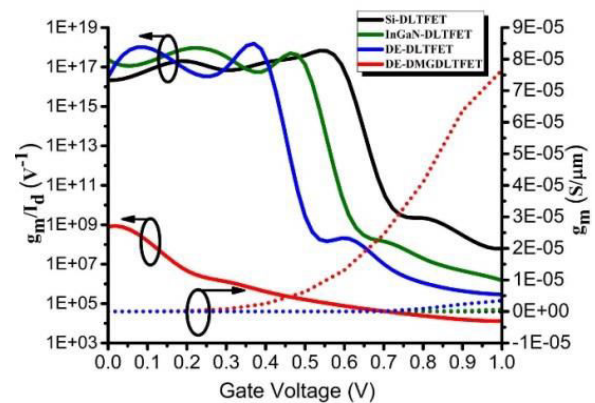
(a)
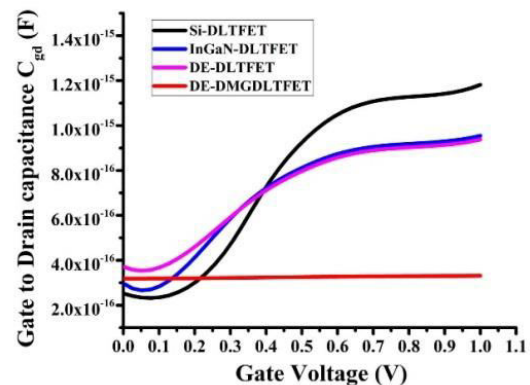
(b)

Figure-6. (a) Variation of transconductance (g_m) and transconductance to current ratio (g_m/I_d) with V_{gs} (b) Gate to drain capacitance of all simulated devices variation with gate voltage at V_{ds} = 1V.
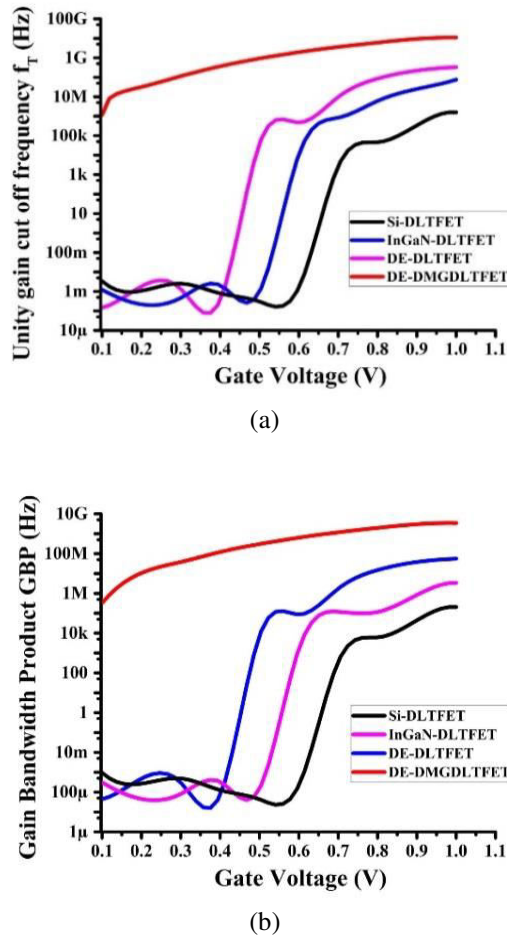
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(a)

(b)

Figure-7. (a) Cut-off frequency f_T and (b) Gain band width product GBP variation with gate to source voltage at $V_{ds} = 1V$.

$$f_T = \frac{g_m}{2\pi\,(C_{gd} + C_{gs})} \tag{6}$$

$$GBP = \frac{g_m}{2\pi\,(C_{gd})} \tag{7}$$

Where f_T is the transient frequency at which the current gain of the device becomes unity and GBP is the measure of the device performance in high-frequency ranges calculated at DC gain of 10. DE-DMGDLTFET has very good f_T response and achieves a peak value at lower V_{gs} as shown in Figure7(a). This is due to the combined effect of higher value of g_m and a decreased value of $C_{gs} + C_{gd}$. In comparison to other structures, the reduced C_{gs} owing to gate engineering enhances the f_T response of the device. It is also noticed from Figure 7(b) that GBP for DE-DMGDLTFET significantly ranges from MHz to GHz among all the other devices due to the effect of lower C_{gd}. Thus the proposed dual electrode and double metal gate engineering modification of DLTFET gets more beneficial for high-frequency circuit and ultra-low power applications.

CONCLUSIONS

In this paper, an extensive simulation and analysis of various DLTFETs were performed with the help of Silvaco 2D ATLAS simulator. The proposed DE-DMGDLTFET has shown a superior in performance compared to the other DLTFETs. It improves the ON-state current significantly, promotes high I_{on}/I_{off} ratio of 10^{15}, produces very less SS (30.27 mV/dec) and suppresses the ambipolar behavior drastically (10^{10} orders) at low voltages when compared to conventional Si-DLTFET. Better device controllability is achieved in the proposed device due to very low value of Gate to drain capacitance (C_{gd}) and Gate to source capacitance (C_{gs}). In addition to these advantages, the high-frequency parameters f_T and GBP has attained the maximum values at relatively low V_{gs} of 0.5V. Hence based upon this simulation study, DE-DMGDLTFET could be a future potential device for the designs of ultra-low-power analog/RF circuit applications. Our future research direction is to develop a Lookup table based verilog-A modelling of DE-DMGDLTFET to implement in the low power RF voltage multiplier circuit design for efficient harvesting.

ACKNOWLEDGEMENTS

REFERENCES

[1] U. E. Avci, D. H. Morris, and I. A. Young. 2015. Tunnel Field-Effect Transistors: Prospects and Challenges. IEEE Journal of the Electron Devices Society. 3(3): 88-95.

[2] S. Datta, H. Liu, and V. Narayanan. 2014. Tunnel FET technology: A reliability perspective. Microelectronics Reliability. 54(5): 861-874.

[3] S. Anand and R. K. Sarin. 2017. Dual material gate doping-less tunnel FET with hetero gate dielectric for enhancement of analog/RF performance. Journal of Semiconductors. 38(2): 024001.

[4] V. Vijayvargiya, B. S. Reniwal, P. Singh, and S. K. Vishvakarma. 2017. Impact of device engineering on analog/RF performances of tunnel field effect transistors. Semiconductor Science and Technology. 32(6): 065005.

[5] M. S. Ram and D. B. Abdi. 2015. Dopingless PNPN tunnel FET with improved performance: Design and analysis. Superlattices and Microstructures. 82: 430-437.

www.arpnjournals.com

[6] S. Takagi and M. Takenaka. 2017. Ultra-low power MOSFET and tunneling FET technologies using III-V and Ge. in Compound Semiconductor Integrated Circuit Symposium (CSICS), 2017 IEEE. pp. 1-4.

[7] J. Madan and R. Chaujar. 2016. Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability. IEEE Transactions on Device and Materials Reliability. 16(2): 227-234.

[8] P. Pandey, R. Vishnoi and M. J. Kumar. 2015. A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling. Journal of Computational Electronics. 14(1): 280-287.

[9] J. Z. Huang, Y. Wang, P. Long, Y. Tan, M. Povolotskyi and G. Klimeck. 2016. High-Performance Complementary III-V Tunnel FETs with Strain Engineering. arXiv preprint arXiv: 1605.00955.

[10] E. Lind, E. Memišević, A. W. Dey and L.-E. Wernersson. 2015. III-V heterostructure nanowire tunnel FETs. IEEE Journal of the Electron Devices Society. 3(3): 96-102.

[11] S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar and S. Jit. 2016. A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors With a SiO2/High- k Stacked Gate-Oxide Structure. IEEE Transactions on Electron Devices. 63(8): 3291-3299.

[12] K. Cecil and J. Singh. 2017. Influence of Germanium source on dopingless tunnel-FET for improved analog/RF performance. Superlattices and Microstructures. 101: 244-252.

[13] K. Nigam, P. Kondekar, and D. Sharma. 2016. High frequency performance of dual metal gate vertical tunnel field effect transistor based on work function engineering. Micro & Nano Letters. 11(6): 319-322.

[14] M. J. Kumar and S. Janardhanan. 2013. Doping-less tunnel field effect transistor: Design and investigation. IEEE transactions on Electron Devices. 60(10): 3285-3290.

[15] S. Tirkey, D. Sharma, B. R. Raad and D. S. Yadav. 2018. A Novel Approach to Improve the Performance of Charge Plasma Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices. 65(1): 282-289.

[16] R. J. Hueting, B. Rajasekharan, C. Salm and J. Schmitz. 2008. The charge plasma PN diode. IEEE electron device letters. 29(12): 1367-1369.

[17] C. Sahu and J. Singh. 2014. Charge-plasma based process variation immune junctionless transistor. IEEE Electron Device Letters. 35(3): 411-413.

[18] S. Singh, A. P. Singh and P. N. Kondekar. 2017. A novel self-aligned charge plasma Schottky barrier tunnel FET using work function engineering. Microelectronic Engineering. 168: 67-75.

[19] S. Anand and R. K. Sarin. 2017. Gate misalignment effects on analog/RF performance of charge plasma-based doping-less tunnel FET. Applied Physics A. 123(6): 413.

[20] D. S. Yadav, B. R. Raad and D. Sharma. 2016. A novel gate and drain engineered charge plasma tunnel field-effect transistor for low sub-threshold swing and ambipolar nature. Superlattices and Microstructures. 100: 266-273.

[21] D. S. Yadav, A. Verma, D. Sharma, S. Tirkey and B. R. Raad. 2017. Comparative investigation of novel hetero gate dielectric and drain engineered charge plasma TFET for improved DC and RF performance. Superlattices and Microstructures. 111: 123-133.

[22] A. U. Manual. 2010. Device simulation software, Silvaco Int. Santa Clara, CA, Version.