VOL. 14, NO. 4, FEBRUARY 2019 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

DESIGN AND IMPLEMENTATION OF COGNITIVE RADIO BASED ON XILINX FPGA

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ABSTRACT

Day by day the frequency spectrum became crowded and unable to provide new services to user easily. Cognitive radio (CR) is a convincing solution for solving spectral congestion issue that has the ability to sense the surroundings bands, adjust and learn to acquire best communication. In this paper, the energy detection (ED) is used to improve spectrum sensing by sensing the spectrum and decide whether there is a signal or noise. BPSK and QPSK are used as the received noisy signals to test the performance of the CR under AWGN. The simulation is done by MATLAB Simulink and Xilinx system generator then downloaded on FPGA SPARTAN 3A. The obtained results show good results as compared with the other works.

Keywords: CR, ED, spectrum sensing, BPSK, QPSK.

1. INTRODUCTION

CR is a modern promised technology that aims into relieves the spectrum paucity issue from wireless communication through allowing access for unlicensed secondary users into frequency bands that are allocated in to licensed primary users, in method that doesn't impact goodness for service for the licensed network [1-3]. ED is an optimum method into reveal primary signal when priori information to the primary signal is unknown to secondary users. It measures the energy of the received waveform over a specified observation time [4, 5].

The CR includes number of steps to complete its job. These steps such as: spectrum sensing, spectrum management, spectrum sharing and spectrum mobility. In this paper, the System generator (SG) that is a digital signals processing designs tool of Xilinx is used in the design. The design is based on Simulink environment i.e. Xilinx specific block set in system generator tools. We can access this Xilinx specific block set by configuring Xilinx system generator (XSG) with appropriate MATLAB and downloaded on FPGA.

2. A GENERAL CYCLE OF THE COGNITIVE RADIO

CR is continuously scanning the spectrum to determine the primary user and secondary user. Sense for vacating the band if primary user arrives cognitive radio must not harm primary user then sense for finding unused spectrum. Figure-1 shows the cognitive radio cycle [5].

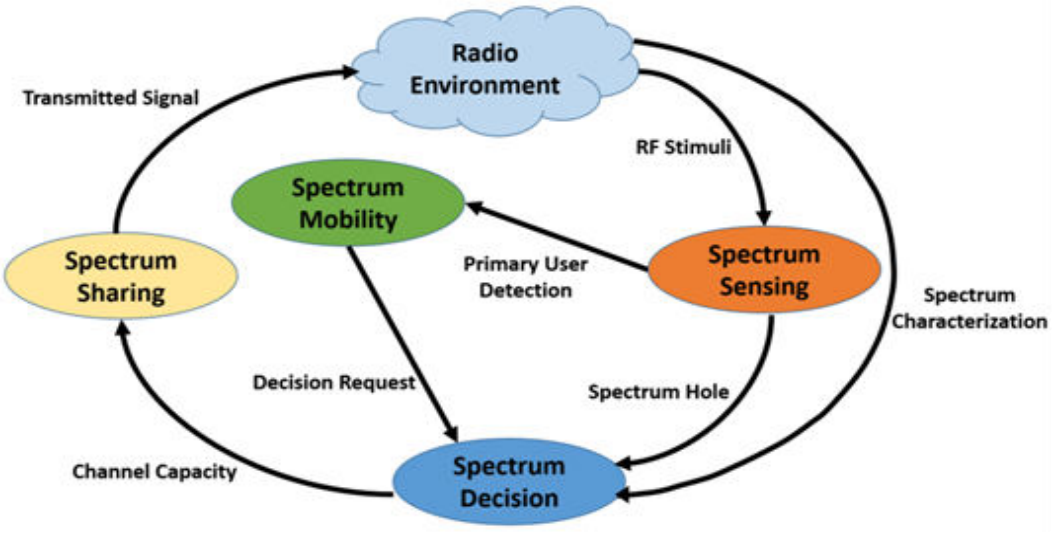

Figure-1. Cognitive radio cycle [5].

3. ED IN THE SPECTRUM SENSING

ED is the most popular way for the spectrum sensing because of its low computational & implementation complexities. It is a most generic way as the receivers do not need any knowing related to the primary user's (PU) signal. The signal is detect mean of compare the output of the energy detector for a threshold which depends on the noise floor. The important challenge

for the energy detector based sensing is the selection of the threshold for detecting primary users. The other challenges include inability to differentiate interference from primary users and noise & low performance under low signal-to-noise ratio (SNR) values [6].

4. PROPOSED SYSTEM

The first part of the proposed system is the BPSK system as shown Figure-2 that represent the BPSK transmitter in system generation that implemented as ROMs. Xilinx ROM is a signal port read only memory that stores two words corresponding to '0' and '1'.the basic of ROMs (mapper) depth 2,initial value vector[1,-1].

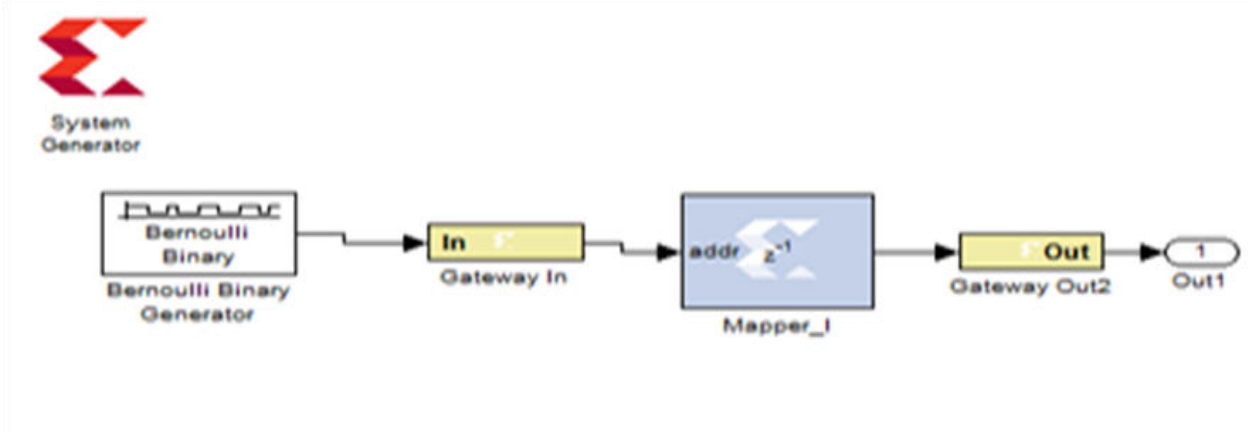

Figure-2. Xilinx BPSK transmitter in system generator.

The second part is the QPSK as shown in Figure-3 that shows the QPSK transmitter using the system generator. The input data is randomly binary sequences (1's and 0's) generated by Bernoulli Binary Generator (BBG), gate way in, serial to parallel number of bit in serial to parallel (s/p), unsigned data represented in fixed point of one bit with zero binary point, and it creates a single output of two consequential input bits, in other words it combines every two bits to be mapped in the ROM to the corresponding QPSK symbol.

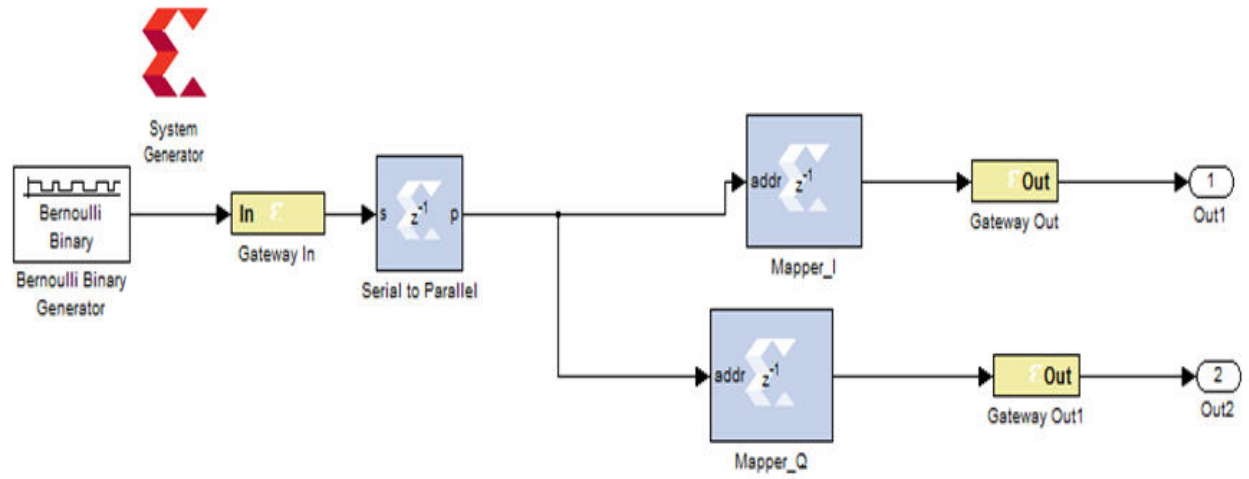

Figure-3. Xilinx QPSK transmitter in system generator.

Xilinx ROM block is a single port read-only memory that stores four words corresponding to "00","01","10","11".The QPSK symbol consist of Quadrature and In-phase value, two ROMs are used for both Q&I channels.

The combinational between the BPSK and QPSK is shown in the Figure-4 as shown below for Energy Detection(ED) of cognitive radio based multi user using MATLAB R2011a in Xilinx System Generator.

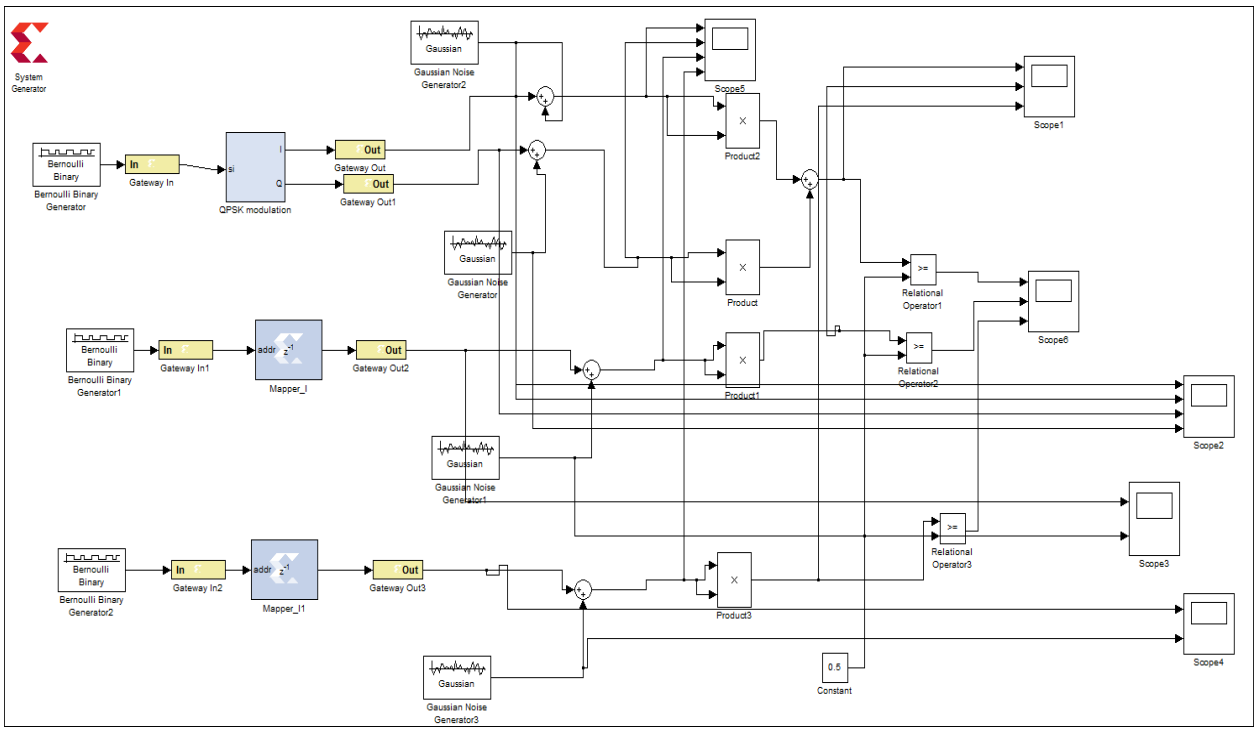

Figure-4. Xilinx (BPSK, QPSK) transceiver based multi user for ED in system generator.

The output waveform from this model compared with comparator at threshold 0.5 is shown in Figure-5.

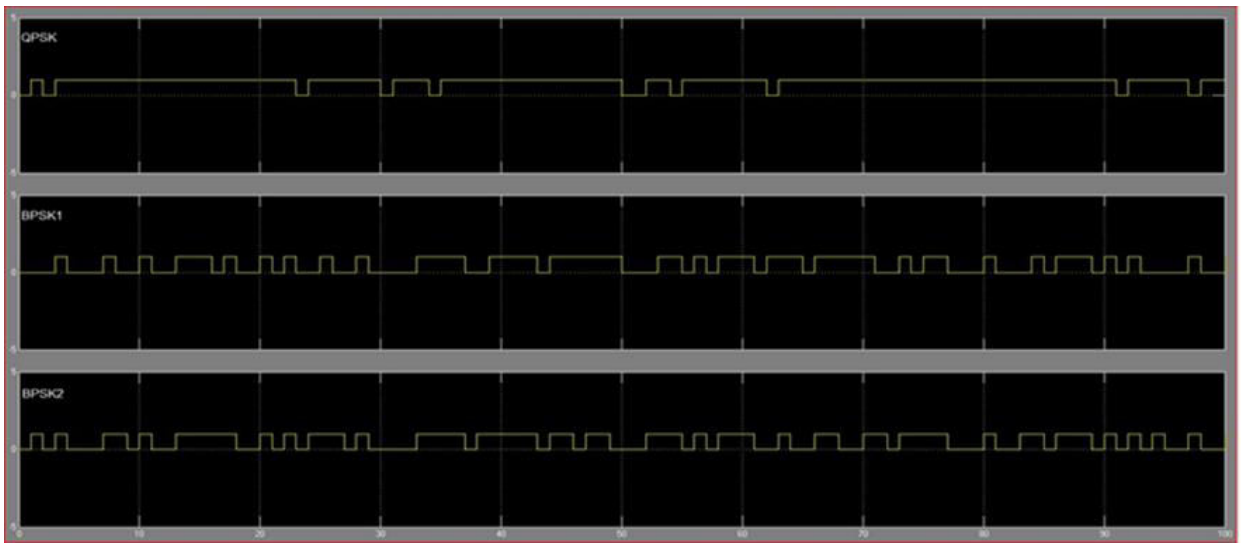

Figure-5. XSG waveform simulation transceiver for ED.

5. HARDWARE CO-SIMULATION

System Generator (SG) provide hardware co-simulation, making it likely to incorporate a design running on FPGA directly via Simulink.co-simulation compilation target automatically make bit stream & associate it into block as shown below in Figure-6.

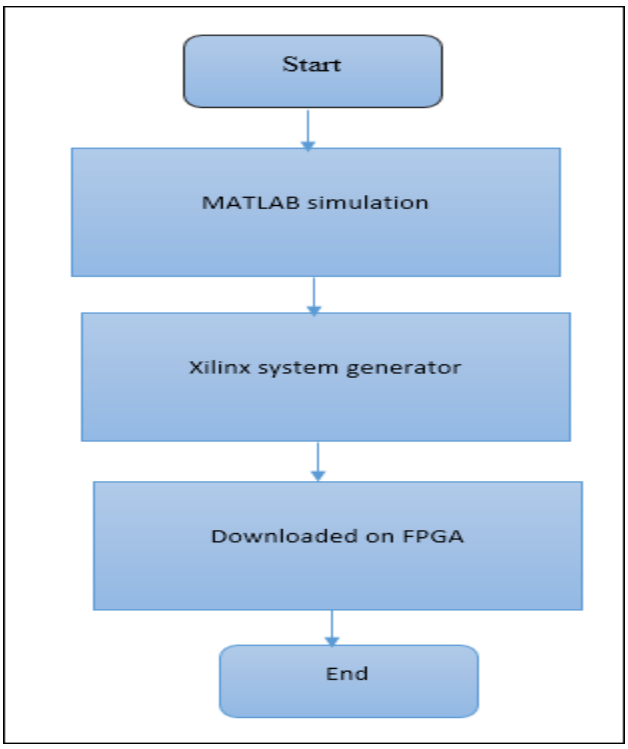

Figure-6. Block diagram of FPGA based hardware co-simulation.

Hardware co-simulation block is created in a new Simulink library by System Generator [7]. The hardware co-simulation block has the same number and names of ports for original Xilinx design. For the (BPSK, QPSK) transceiver model, a new Simulink model is created JTAG hardware co-simulation the Figure-7 as shown present for this model.

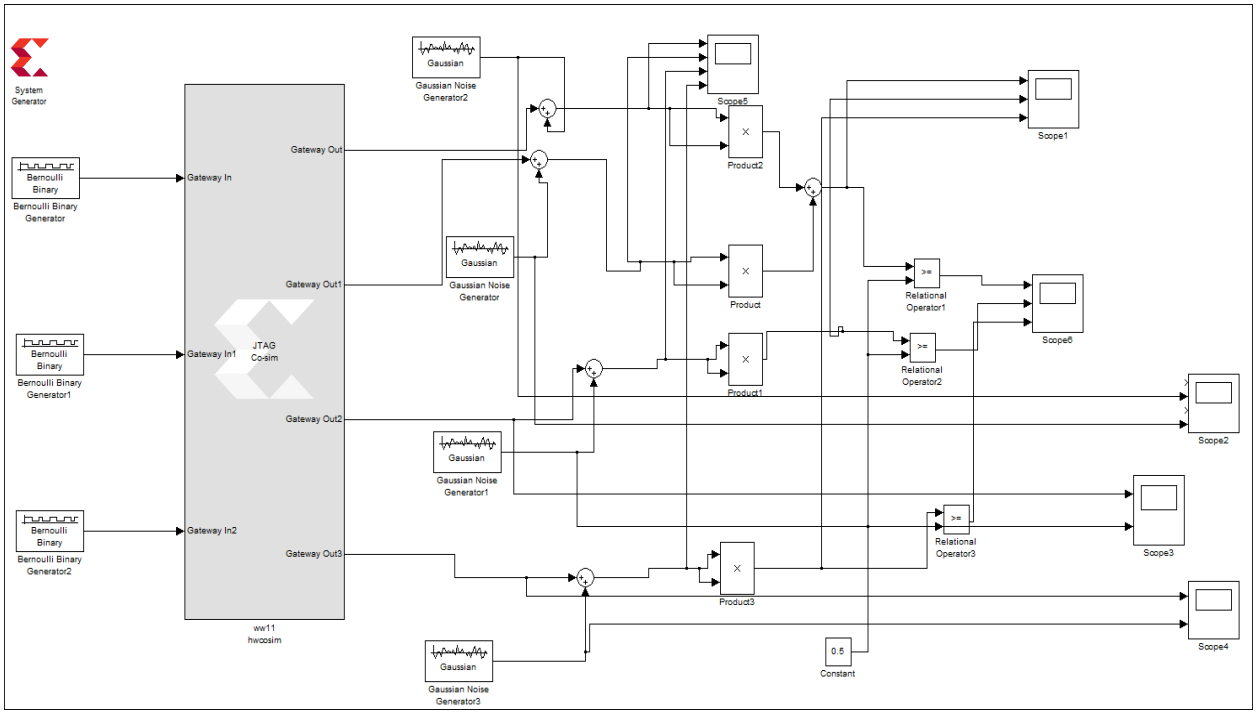

Figure-7. (BPSK, QPSK) transceiver based multi user model for hardware co-simulation.

In Figure-8 as shown is present waveform for last block (comparator) at threshold 0.5 for hardware co-simulation.

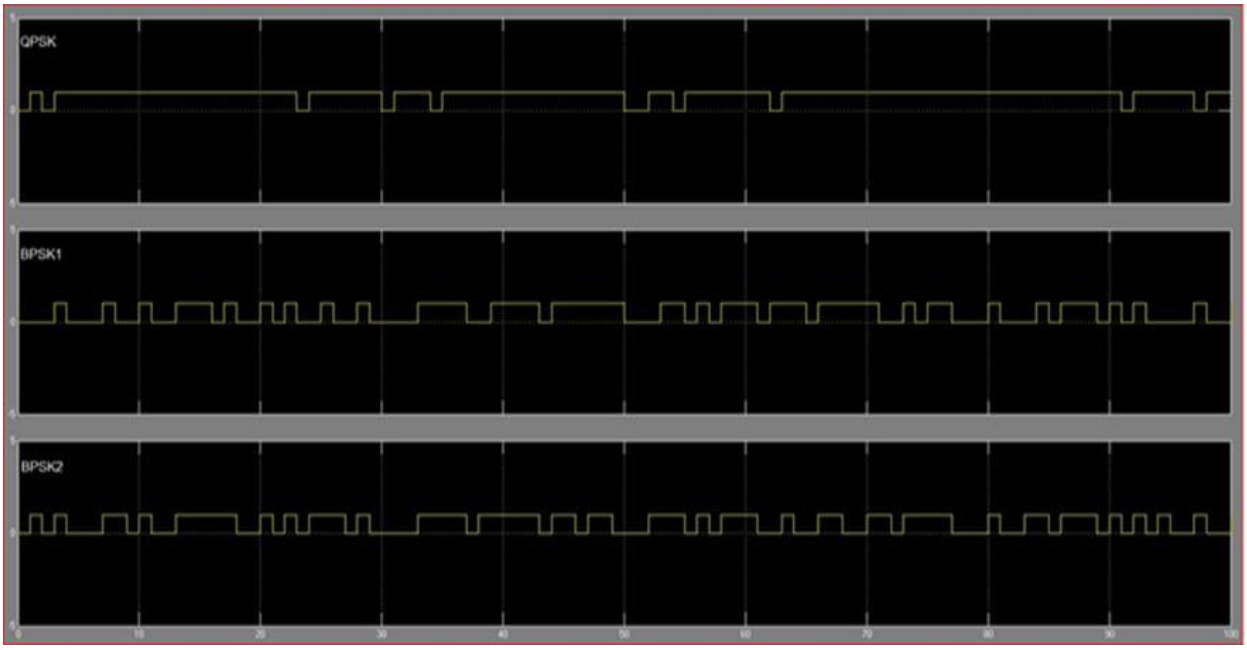

Figure-8. Hardware co-simulation waveform for transceiver model.

The output waveform in hardware co-simulation is the same waveform in XSG, hence each ones represented signal (primary user) and each zero represented noise signal (secondary user) because comparator is digital.

6. RESOURCE UTILIZATION

Table-1 represent details device utilization summary.

Table-1. Model transceiver device utilization summary.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	11	5888	0%
Number of Slice Flip Flops	17	11776	0%
Number of 4 input LUTs	1	11776	0%
Number of bonded IOBs	10	372	2%
Number of GCLKs	1	24	4%

Figure-9 shows overall model system ((BPSK, QPSK) transceiver model for hardware co-simulation) apply on FPGA SPARTAN 3A.

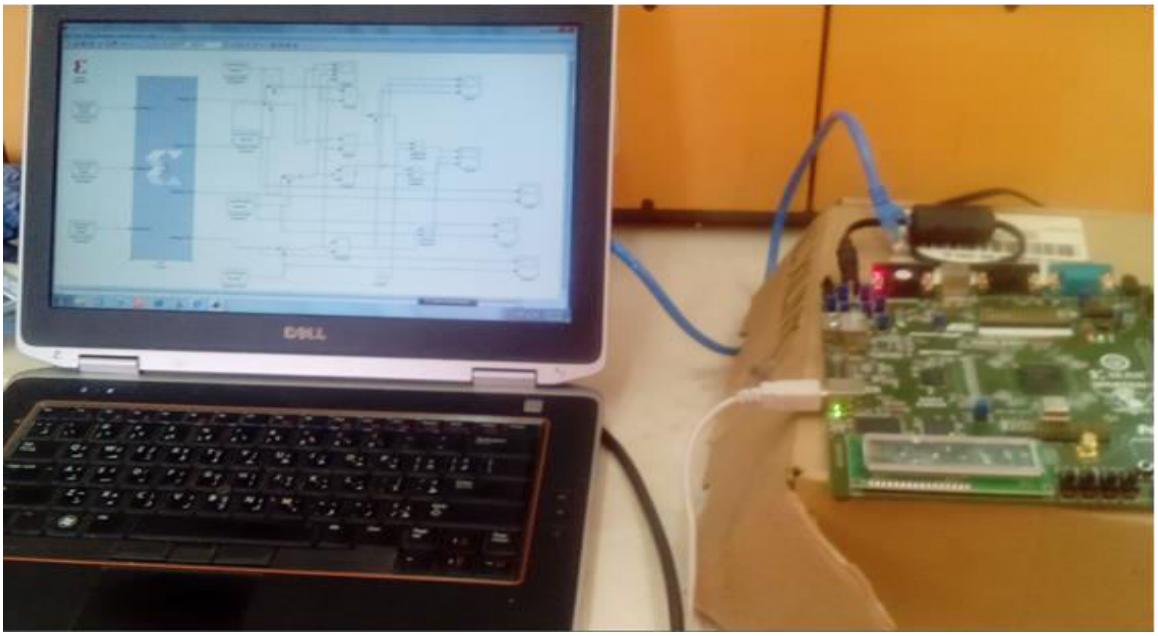

Figure-9. FPGA implementation of proposed system.

7. CONCLUSIONS

This paper represented a methodology for implementation of energy detection of CR on FPGA. ED is carried out for 3 users. The presence or absence for the primary user (PU) is decided based on the threshold .the proposed of ED for CR system by Simulink in an environment of MATLAB in system generator and downloaded on FPGA SPARTAN 3 A.

REFERENCES

[1] T. A. W. Ysocki, A. B. J. Amalipour, and U. N. O. F. S. Ydney. 2011. a Ccepted From O Pen C All S Pectrum M Anagement in C Ognitive R Adio: a Pplications of P Ortfolio T Heory in W Ireless C Ommunications.Ieee Wirel. Commun., no. August. pp. 52-60.

[2] S. Stotas and A. Nallanathan. 2012. On the Throughput and Spectrum Sensing Enhancement of Opportunistic Spectrum Access Cognitive Radio Networks.Wirel. Commun. IEEE Trans. 11(1): 97-107.

[3] Ahmed A. Thabit. 2017. Design and Simulation of Adaptive Cognitive Radio based on SDR Using Higher Order Moments and Cumulants. Book, Shaping the Future of ICT: Trends in IT, Communication Systems and Management.

[4] A. Ranjan, Anurag and B. Singh. 2016. Design and analysis of spectrum sensing in cognitive radio based on energy detection.2016 Int. Conf. Signal Inf. Process.pp. 1-5.

[5] S. Barve, A. Akotkar, A. Chavan, A. Kumar and M. Dhaigude. 2014. Open Source Software Defined Radio Using GNU Radio and USRP," international journal of scientific and technology research. 3(5): 305-308.

[6] I. F. Akyildiz, W.-Y. Lee, M. C. Vuran and S. Mohanty. 2006. NeXt generation/dynamic spectrum access/cognitive radio wireless networks: A survey. Comput. Networks. 50(13): 2127-2159.

[7] J. Ou. 2005. MATLAB/Simulink Based Hardware/Software Co-simulation for designing using FPGA Configured Soft Processors. In 19th IEEE International parallel and distributed processing symposium (IPDPS'05).