



STAIRWAY CONTROL OF BUCK POWER SUPPLIES IN PARALLEL CONFIGURATION

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ABSTRACT

Power supplies are configured in parallel to provide higher current demand to the load, while achieving modularity by using low-power power converter modules. However, in some cases, redundancy of power converters is installed to provide safety in case of overload and breakdown of a module. In such case, the wear and tear of all modules vary depending on what the load side present. We present in this work a basic control for ensuring that power module utilization is approximately equal for all modules in the parallel configuration. Our proposed control methodology turns ON/OFF a module based on the current load scenario. By switching the utilization of these modules, our control can display a stairway waveform while regulating the output voltage and supplying the necessary current. We demonstrate our control structure through simulations of various static and dynamic loading conditions, while considering error in current sharing of working power modules.

Keywords: stairway control, parallel configuration, buck converter, current sharing error.

1. INTRODUCTION

Nowadays, most systems are developed while considering modularity. The modularity in any systems allows quick replacement of broken parts and has also the advantage of quickly adding modules if the load requirement is suddenly increased. System reliability is also increased because of redundancy, while thermal stress is reduced because more power modules are sharing the load. Finally, parallel configuration offers flexibility especially for those applications requiring power increase [1]. Parallel configurations are widely utilized, and a typical example is the urban distributed power system [2], as illustrated in Figure-1. In this work, we focus only on the point-of-load (POL) converters section.

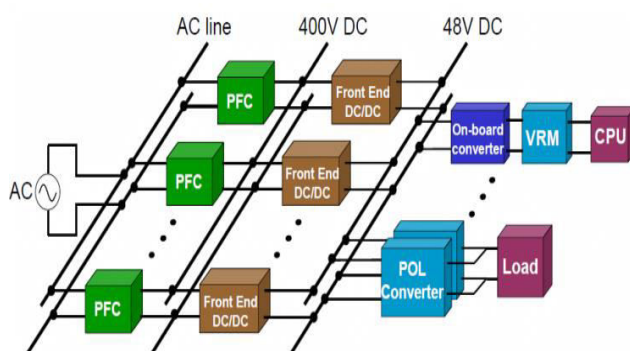


Figure-1. Distributed and parallel power system [3].

In parallel converter configuration, various current sharing methods have been developed, e.g., master-slave [4], droop method control [5], and average-current method (ACM) [6]. In this study, the ACM is employed in regulating the voltage while supplying the necessary current requirement [2].

Another key interesting aspect in today's power control is the incorporation of digital processors capable of operating high speeds. With this property, sampling and

quantizing voltage and current levels of continuous systems have become easily accessible. Digital control also offers noise immunity due and the wear and tear due to variations in the analog components. Lastly, changing of control parameters become convenient since there will be no hardware change of resistors or passive components. Every change will be done in the source code. This flexibility in digital control is easily applicable to various applications with varying specifications and can be done at a faster rate when compared to its analog counterpart [7].

In this work, we explore the idea of turning power modules ON/OFF adaptively according to the presented load current. Such method will allow the slowing down of power module damage due to wear and tear, and operational stress. We summarize our major contributions for this work below.

- The state models of the buck power converter are derived by obtaining the equations of the inductor current and capacitor voltage. Three control loops have been included to implement average-current mode sharing among all parallel converters.
- A Stairway control is proposed to allow the sequential turning ON/OFF of power converters depending on the load requirement. A current sharing error metric determines the performance of the Stairway control strategy.
- Extensive simulations to verify the system's performance under various static and dynamic loading conditions have been performed.

The outline of the research presented in this work is presented as follows: Section 2 discusses framework of the study focusing on the modeling of the step-down (buck) power converter, average-current mode control and the proposed stairway control strategy. In Section 3, we present the results derived from the exhaustive simulations we have done. Finally, the research work is concluded in Section 4.



2. PARALLEL CONVERTER SETUP AND METHODOLOGY

In this section, we discuss the modeling of the parallel converters, the control strategy, and the digital control of the power module.

2.1 Modeling of the buck converter

We utilize four step-down converter modules in our parallel configuration. The basic buck converter power section is depicted in Figure-2, while its parameters are given in Table-1. To consider the different manufacturing variation among power supply providers, we vary only the series resistance of each of the four power modules.

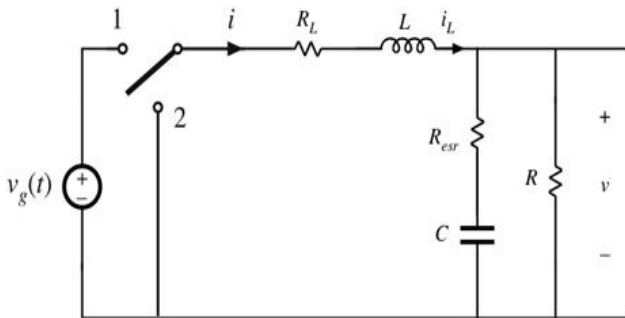


Figure-2. Buck Topology.

Table-1. Buck Converter Specifications.

Parameter	Value
Input Voltage	20 V
Output Voltage	12 V
MinOutput Current	0 A
Max Output Current	2.5 A
Switching Frequency (Current Loop)	250 kHz
Switching Frequency (Voltage Loop)	100 kHz
Series Resistance R_L	0.01 - 0.08 Ohms
Inductance L	49.08 uH
Capacitance C	153.4 uF

From Figure-2, the inductor voltage and capacitor current differential equations are obtained to arrive at the model of the buck section. These are given in Eq. (1) - (3):

$$\frac{di_L}{dt} = \frac{1}{L} (V_g * d - i_L R_L - v_o) \quad (1)$$

$$\frac{dv_C}{dt} = \frac{1}{C} (i_L - i_{out}) \quad (2)$$

$$v_o = v_C + R_{esr}(i_L - i_{out}) \quad (3)$$

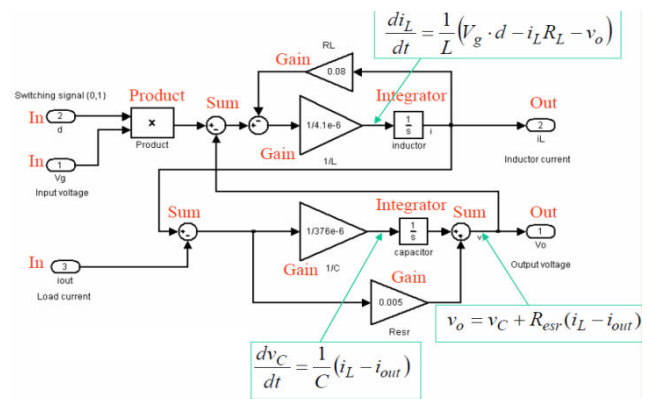


Figure-3. Power Module Modeled in Simulink.

Since we have the differential equation model, MATLAB/Simulink will be used to investigate our proposed control strategy, just like how the DC motor characteristics were studied in [8]. Figure-3 above is the equivalent working blocks of Equations (1) - (3). The corresponding differential equation representing the inductor and capacitor states are explicitly highlighted. To implement an n-module power converter, we would have to provide multiple copies of this and simply vary the gain blocks accordingly.

2.2 Average current control (ACM) strategy

When two or more power supplies are configured in parallel, the voltage of regulation of each power module tend to be different from each other, which is due to the manufacturing differences. The difference in the regulating voltage is termed as initial set point accuracy [9]. Due to this, parallel modules tend to not equally share the output current requirement. To keep the power constant, modules having a low output voltage carry much of the current requirement as oppose to those with a higher output voltage.

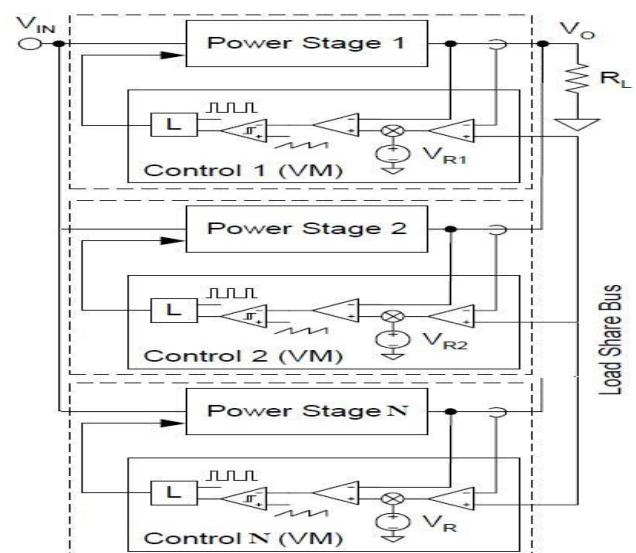


Figure-4. Average current-mode control strategy employing voltage-mode for controlling parallel buck converters [9].



Since the goal of placing converters in parallel configuration is to act as if it is equivalent to a single power module, then each paralleled module should share the load equally. To do this, we employ the average current mode control, where the inductor current is averaged and becomes the reference of all buck converters. Given the average current as the reference point, those below (above) this setting will tend to increase

(decrease) their output accordingly. Figure-4 presents a voltage-mode controlled parallel buck converter configuration.

The ACM strategy can improve noise immunity using an inner loop current compensator. Also, ACM provides the opportunity to control the inductor's average current [10]. Since digital computers are now highly available and come at a cheaper price, performing the

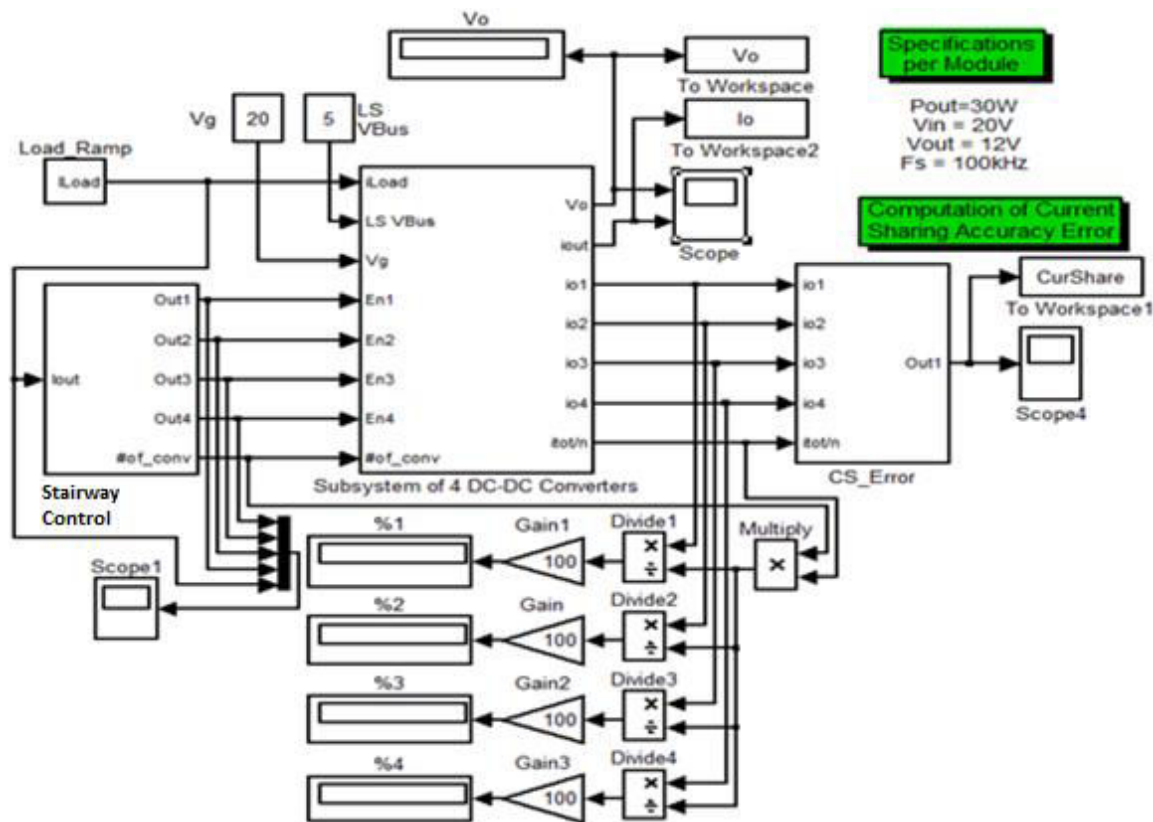


Figure-5. Complete Simulink Power Converter Model with the Proposed Stairway Control.

average of two or more states have become easy to implement. In fact, in [11], parallel DC-DC converters have already been digitally controlled to equally share the load. The disadvantage, however, was a look-up table was used as a replacement of an actual converter.

2.3 Control system

Once the plant transfer function has been modeled in Equations (1) - (3), we proceed with designing the controllers. The standard controllers used in buck converters are the PID controllers, which have many applications such as seen in [12]. The analog and its digital counterpart controllers' transfer functions are given in Table-2. There are actually three designed control loops, i.e., (1) voltage-mode control (vmc) to regulate the voltage, (2) current-mode control (cmc) for sensing/controlling of the inductor current, and (3) current share loop (CS) for the averaging of the output currents of

all modules. The CS loop has the lowest operating frequency among the three control loops, since it is the outermost feedback. Quantization of controller coefficients has been done so that choosing a microcontroller or digital signal processor will be easy. During quantization, 16-bit signed representation is used. The sampling frequencies for the voltage, current and current-share loop are 100 kHz, 250 kHz and 250 kHz, respectively.

Figure-5 illustrates the Simulink model with the proposed Stairway Control block having four parallel buck converters. Each block is discussed below. Figure-6 depicts how the four buck converters have been interconnected inside "Subsystem of 4 DC-DC Converters". The ACM scheme implements the load sharing bus at 5V.

**Table-2.** PID Controllers for each control loop.

	Analog Transfer Function	Quantized Digital Transfer Function
V _{mc}	$\frac{9 \times 10^6 (s + 2000)}{s(s + 250000)}$	$\frac{10.100z^2 + 0.200z - 9.900}{0.5z^2 - 0.4445z - 0.0556}$
C _{mc}	$\frac{37155(s + 1300)}{s(s + 105000)}$	$\frac{0.0308z^2 + 0.0001z - 0.0307}{0.5z^2 - 0.8265z + 0.3264}$
CS Loop	$\frac{0.1(s + 40)}{(s + 150000)}$	$\frac{0.0387z - 0.0382}{0.5z - 0.2693}$

To take into consideration the manufacturing differences in terms of tolerances, we introduce a metric called the current sharing error (CS_error). To determine the sharing accuracy, Equation (4) is used.

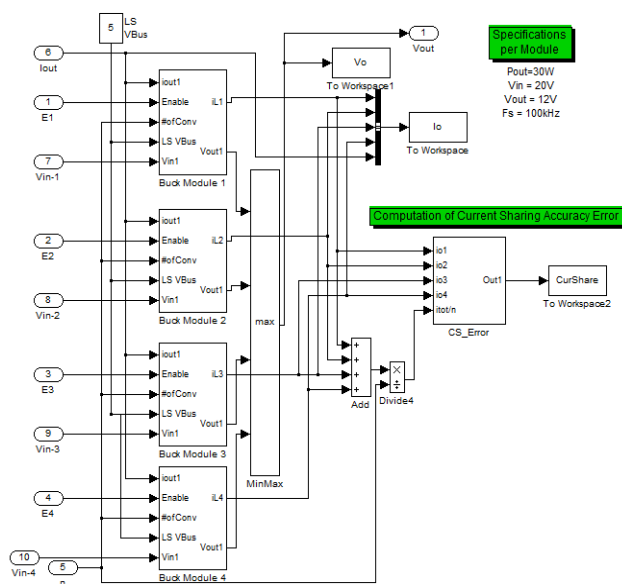
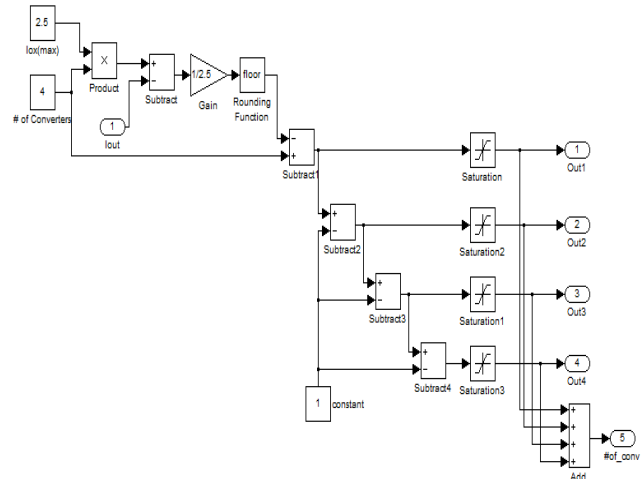
$$\%CS_{Error} = \left| \left| 1 - \frac{I_{ox}}{I_{tot} \cdot N} \right| \right| \times 100\% \quad (4)$$

To implement the basic stairway control, the output current is sampled to know the required number of operational converters. Equation (5) determines how many of the total converters in parallel must be operated. The Simulink model is shown in Figure 7.

$$n = N - \text{floor} \left\{ \frac{N I_{ox(max)} - I_{out}}{I_{ox(max)}} \right\} \quad (5)$$

where:

- I_{ox} = converter x 's output current, $x \in \{1, 2, 3, 4\}$
- $I_{ox(max)}$ = converter x 's maximum output current
- I_{tot} = total output current
- N = number of paralleled power converters
- n = number of operational converters

**Figure-6.** The block connections of four power modules under “Subsystem of 4 DC-DC Converters.”**Figure-7.** Simulink Model for the proposed Basic Stairway Control.

For a parallel configuration that has four parallel converters, the operation of the Basic Stairway Control is depicted in Table-3, given that each module has a maximum output current of 2.5A. A “1” signifies that the converter x is operational; while a “0” denotes that converter x is decoupled from the parallel configuration.

The name basic stairway control is derived from the manner how converters are sequentially turned ON or OFF. In Table-3, when one draws the output current when converters are turned ON, one would notice that a staircase is obtained. In such control scheme, however, it is obvious that all times, the first converter is always functional, while converter 4 is the least utilized, especially during light load condition, e.g., $I_{out} < 5A$. This issue is addressed by a more sophisticated controller tackled in [14].

Table-3. Stairway Control Operations Example.

I_{out}	Out1	Out2	Out3	Out4
$0.0 < I_{out} \leq 2.5$	1	0	0	0
$2.5 < I_{out} \leq 5.0$	1	1	0	0
$5.0 < I_{out} \leq 7.5$	1	1	1	0
$7.5 < I_{out} \leq 10.0$	1	1	1	1

3. RESULTS AND DISCUSSIONS

Exhaustive simulations have been performed to evaluate the performance of the proposed Basic Stairway



Control given a four-parallel buck converter system. Each buck converter has a specification of 30W with a 12V regulated output and a maximum output current of 2.5A.

We paralleled four converters to provide a total power rating of 120 Watts. Static loading of 10A was first tested to see performance of the system during full load. It is followed by an output current demand that is ramping from 0A to 10A. Lastly, the final test includes a dynamic current loading of 10-2-6-3A to verify the system's response during dynamic loading. To all these simulations trials, we will only present the current sharing error since this is only metric to verify if there is an equal sharing among the parallel modules. We guarantee that the output voltage is well-regulated. Figure-8 shows the current sharing error. Converter 1 has the largest error of about 5%, signifying that its voltage is slightly different from the three other modules. Investigating the output voltage of module 1 reveals that it has a much bigger oscillation compared to the rest of the group. However, this is just a minor ripple that has little effect on the current sharing capability of the system.

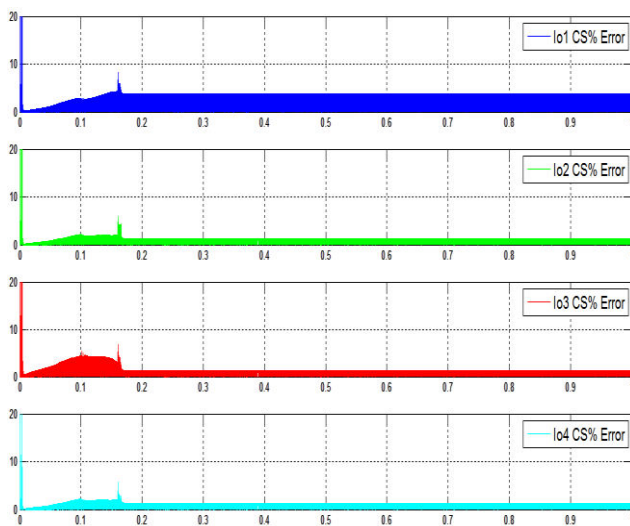


Figure-8. Current Sharing Error during Static loading condition.

In Figure-9, as the load current increases while at the same time, passing the integer multiples of $I_{ox(max)}$, the turning ON of each converter is seen, i.e., the transition from a 100% CS error to almost zero. A 100% CS error means that the converter is OFF. We can notice here that just like the static loading test, converter 1 experiences the highest current sharing error. The slight increase in the CS error of converter 1 is an indication that another converter is turned ON.

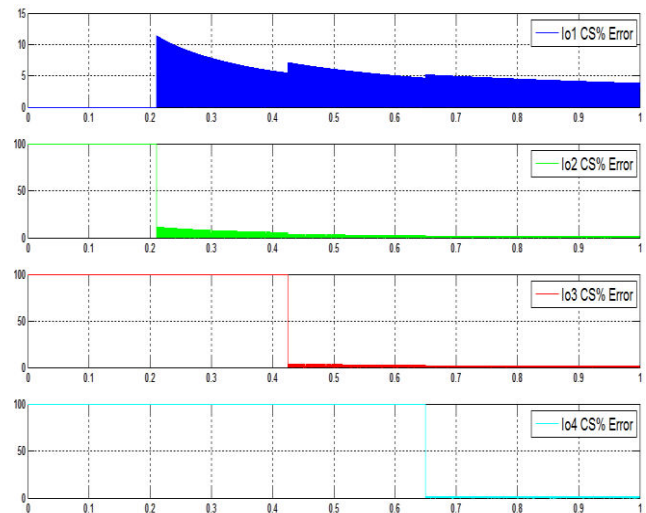


Figure-9. Current Sharing Error during a ramping output load.

From Figure-10, the current sharing error has a maximum value of 10% when more than two power converters are operating. This is one of the expected results during dynamic loading and must be investigated to make sure that results are still allowable and within range.

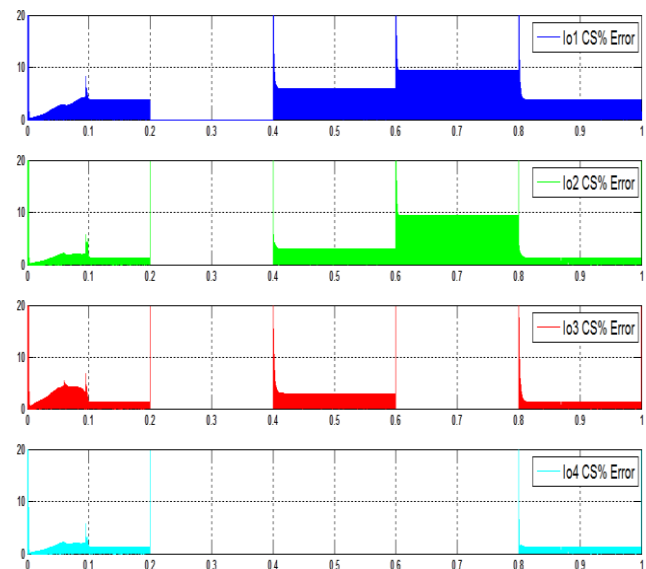


Figure-10. Current Sharing Error with an output load current of 10-2-6-3A.

Table-4. Minimum number of bits to be used in each control loop.

Voltage Mode Control Loop	Current Mode Control Loop	Current Share-loop
11	13	8

Finally, we experimented on how the number of bits affects the regulation and the sharing of the parallel system. Figures 8, 10, highlight the use of 16-bit quantization. In this investigation, we isolate each block



and maintain the other two blocks at 16 bits. For the isolated block, the number of bits is lowered until no regulation and equal current sharing are achieved. Once the minimum number of bits is determined for a control loop, we proceed with the next control loop and do the same adjustments. Table-3 summarizes these findings, while Figure-11 shows the system's performance under these bit-representations. It can still be seen that the system is well-regulated while equally sharing the load current.

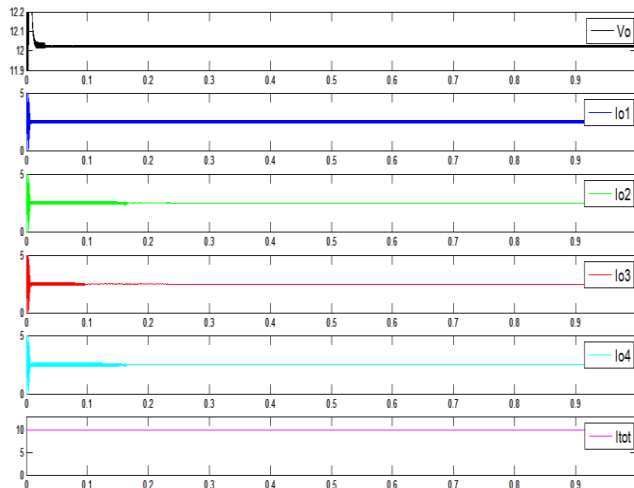


Figure-11. System Response when using the least number of bits. Static loading condition with $I_{Tot} = 10A$.

4. CONCLUSIONS

A basic stairway control of four parallel digital buck converters has been proposed and investigated using Matlab/Simulink. It has determined the corresponding number of functional converters, given the load output requirement. To verify the proposed control strategy and modeling of the digital buck converter, static and dynamic types of loading have been utilized. The basic stairway control can regulate the output voltage while at the same time keeping to a maximum of 10% current sharing error among the modules. Particularly, during high load, the current sharing error is less than 5% for each power module. This has been also achieved by utilizing a 16-bit representation for the digital controllers.

In the future, more sophisticated control techniques will be tested in order to further reduce the current sharing error. Also, scalability of the said system will be explored, while at the same time, making sure that all modules have an approximate equal utilization.

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