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CONCEPTION AND HARDWARE MINIMIZATION OF A NEW CHIEN SEARCH BLOCK FOR REED SOLOMON CODES WITH IMPLEMENTATION ON FPGA CARD

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ABSTRACT

Error Correcting Codes such as Reed Solomon (RS) and Bose, Chaudhuri, and Hocquenghem (BCH) are widely used in communication and storage systems in order to correct and control errors introduced by transmission channel. In this paper, a simplified algorithm for RS and BCH decoding is proposed with a view to reduce the number of components compared to the basic chien search block. First, we developed the design of the proposed algorithm second, we generated and simulated the hardware description language source code using Quartus software tools and finally we implemented the new algorithm of chien search block on FPGA card.

Keywords: error locator polynomial, RS decoder, BCH decoder, chien search block, even polynomial, odd polynomial, FPGA implementation.

1. INTRODUCTION

Error correcting codes are widely used in several fields, such as telecommunications, wireless channels [1] [2] [3]. We also find them in the field of storage. We add to the message to transmit additional information to be able to detect and correct the errors introduced by the transmission channel [4] [5] [6]. As these techniques make it possible to control the errors introduced by the noise of the transmission channel, they are called "channel coding" [7]. The main existing techniques are: RS (Reed-Solomon) codes used in DVB (Digital Video Broadcasting) such as (DVB-T, DVB-S and DVB-C), BCH codes (Bose, Ray-Chaudhuri and Hocquenghem) and Low-Density Parity-Check (LDPC) codes used respectively in DVB-S2 Digital Video Broadcasting - Satellite - Second Generation [8] [9]. In this context, the objective of this work is to present a conception and an optimization of the chien search block compared to the basic one used widely in DVB-S2 [10]. We also prove that it's possible to reduce both the number of components and the response time in the Chien Search Block using the hardware description language VHDL for simulation and Xilinx Spartan 3E-500 FG 320 FPGA (xc3s500e-5fg320) for hardware implementation.

2. ERROR LOCATOR POLYNOMIAL

The error locator polynomial E(x) is written to include only the terms that correspond to errors:

$$E(x) = Y_1 X^{e1} + Y_2 X^{e2} + \ldots + Y_v X^{ev} \qquad (1)$$

Where e1, … ev, identify the locations of the errors in the code word as the corresponding powers of x, while Y1,…Yv represent the error values at those locations [11].

The error locator polynomial, Λ (x), has a degree of $v \leq t$ and can be represented as:

$$\Lambda(x) = \prod_i^v (1 + X_i x) \qquad (2)$$
$$= X_1(x + X_1^{(-1)}) X_2(x + X_2^{(-1)}) \ldots$$

Where $X_1 = \alpha^{e1}$, $X_2 = \alpha^{e2}$ … then clearly the function value will be zero if $x = \alpha^{-e1}$, $x = \alpha^{-e2}$ …

3. CHIEN SEARCH ALGORITHM

This algorithm can detect the error position by calculating $\Lambda(\alpha^{-i})$ where $0 \leq i \leq n-1$, such as Λ (x) is the error locator polynomial calculated with the Euclidean algorithm [12]. For the case of RS (15, 11) we must calculate: $\Lambda(\alpha^{-14})$, $\Lambda(\alpha^{-13})$… $\Lambda(\alpha^{-1})$, $\Lambda(\alpha^{-0})$

The Table-1 as shown below presents the obtained results:

Table-1. Roots of error locator polynomial RS (15, 11).

x	x^2 term	x term	unity	Sum
α^{-14}	α^{13}	α^{12}	1	3
α^{-13}	α^{0}	α^{13}	1	13
α^{-12}	α^{2}	α^{14}	1	12
α^{-11}	α^{4}	α^{0}	1	3
α^{-10}	α^{6}	α^{1}	1	15
α^{-9}	α^{8}	α^{2}	1	**0**
α^{-8}	α^{10}	α^{3}	1	14
α^{-7}	α^{12}	α^{4}	1	13
α^{-6}	α^{14}	α^{5}	1	14
α^{-5}	α^{1}	α^{6}	1	15
α^{-4}	α^{3}	α^{7}	1	2
α^{-3}	α^{5}	α^{8}	1	2
α^{-2}	α^{7}	α^{9}	1	**0**
α^{-1}	α^{9}	α^{10}	1	12
α^{-0}	α^{11}	α^{11}	1	1

The two results $\Lambda(\alpha^{-14})$ and $\Lambda(\alpha^{-13})$ mean that: the sixth and the thirteenth symbols respectively in the code word contain the errors.

Generally, In the case of RS (n, k), we must calculate:

$\Lambda(\alpha^{-(n-1)}), \Lambda(\alpha^{-(n-2)}) \ldots \Lambda(\alpha^{-1}), \Lambda(\alpha^{-0})$

If the expression reduces to 0 $\Lambda(\alpha^{-i}) = 0$, then that value of x is a root and identifies the error position else the position does not contain an error.

3.1 Proposed Algorithm

The proposed algorithm is based on a specific and methodic factorization of the error locator polynomial such as {(P (x) = Ax^n + B, where n = 1)} should be depicted in this polynomial. This method allows us to conceive a new circuit of Chien Search Block i.e. we can minimize both the number of components compared to the basic Chien search block [13].

Beginning with theTtable-2 which describes the Number of minimized logic gates for different error locator polynomials [14].

Table-2. Number of minimized logic gates for different error locator polynomials.

Error locator polynomial	Number of logic gates for the basic circuit	Number of logic gates for the modified circuit	Number of minimized logic gates
$\Lambda(X) = AX^2+BX+C$	11	7	4
$\Lambda(X) = AX^3+BX^2+ CX+D$	15	9	6
$\Lambda(X) = AX^4+BX^3+ CX^2+DX+E$	19	11	8
. . .			
$\Lambda(X)=A_nX^n + \ldots+A_1X+A_0$	3+4n	3+2n	2n

If we take the polynomial of degree 3 we have:

$$\Lambda(X) = AX^3 + BX^2 + CX + D \qquad (3)$$
$$= X^2(Ax + B) + (Cx + D)$$

The logic circuit of equation 1 is represented in Figure-1. Also, the Number of logic gates for the basic and modified circuits is represented in Tables-3, 4, 5, 6 and Table-7.

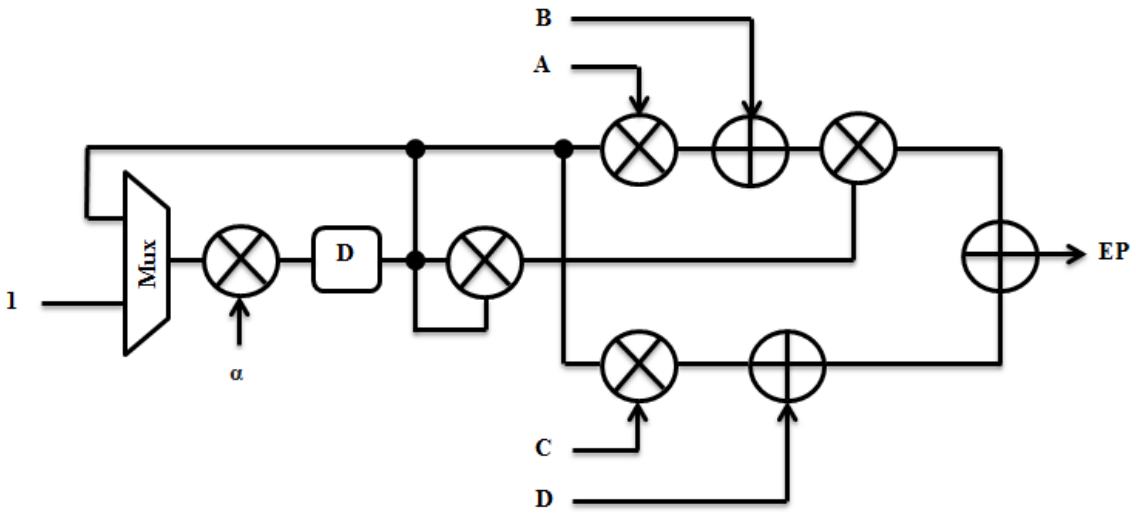

Figure-1. Modified circuit 2 of Chien Search Block for error locator polynomial as degree 3.

Table-3. Number of logic gates for the basic and modified circuits (polynomial as degree 3).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^3+BX^2+ CX+D$	15	9	10

Table-4. Number of logic gates for the basic and modified circuits (polynomial as degree 4).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^4+BX^3+CX^2+ DX+E$	19	11	13

Table-5. Number of logic gates for the basic and modified circuits (polynomial as degree 5).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^5+BX^4+CX^3+DX^2+EX+F$	23	13	15

Table-6. Number of logic gates for the basic and modified circuits (polynomial as degree 6).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^6 +BX^5+CX^4+DX^3+EX^2+FX+G$	27	15	18

Table-7. Number of logic gates for the basic and modified circuits (polynomial as degree 7).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^7+BX^6+CX^5+DX^4+EX^3+FX^2+GX+H$	31	17	20

If we take the polynomial of degree 8 we have:

$$\begin{aligned}\Lambda(X) &= AX^8 + BX^7 + CX^6 + DX^5 \\ &\quad + EX^4 + FX^3 + GX^2 + HX + I \\ &= X^7\left(Ax+B\right) + X^5\left(Cx+D\right) \\ &\quad + X^3\left(Ex+F\right) + X\left(Gx+H\right) + I \quad (4)\end{aligned}$$

The logic circuit of equation 2 is represented in Figure-2. Also, The Number of logic gates for the basic and modified circuits is represented in Table-8.

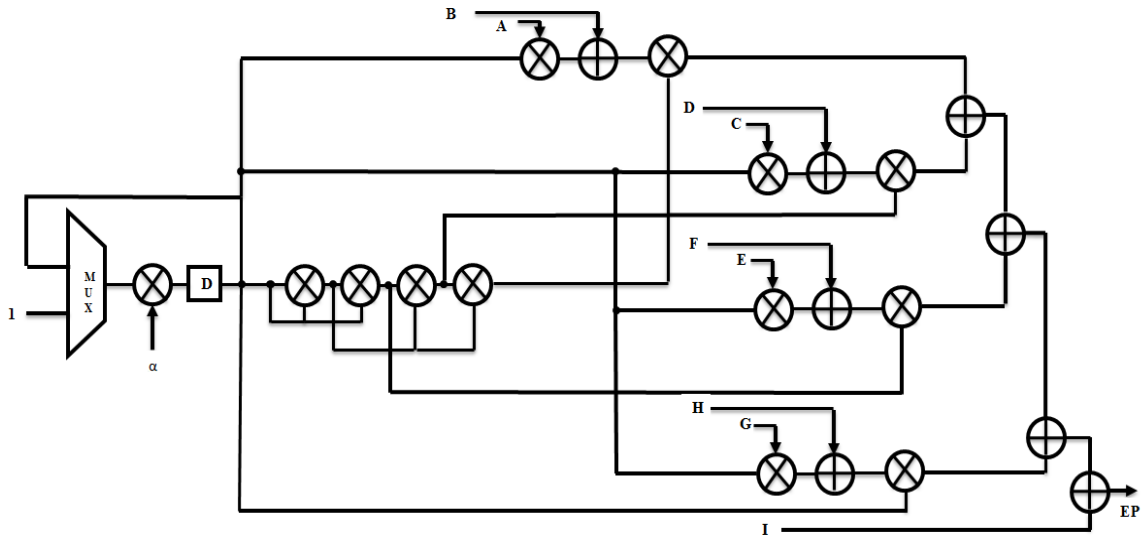

Figure-2. Modified circuit 2 of Chien Search Block for error locator polynomial as degree 8.

Table-8. Number of logic gates for the basic and modified circuits (polynomial as degree 8).

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2
$\Lambda(X) = AX^8+BX^7+CX^6+DX^5+EX^4+FX^3+GX^2+HX+I$	35	19	23

According to the tables we have adopted previously, we can resume all this in two tables, which show the number of the minimized logic gates using both the basic and the modified circuits for different even and odd error locator polynomials.

Table-9. Number of minimized logic gates for different even error locator polynomial.

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2	Number of minimized logic gates
$\Lambda(X) =AX^4+BX^3+CX^2+ DX+E$	19	11	13	6
$\Lambda(X) = AX^6+BX^5+CX^4+DX^3+EX^2+FX+G$	27	15	18	9
$\Lambda(X) = AX^8+BX^7+CX^6+DX^5+EX^4+FX^3+GX^2+HX+I$	35	19	23	12
$\Lambda(X)=A_nX^n + \ldots+A_1X+A_0$	3 + 4n	3 + 2n	3 + n/2 + 2n	3n /2

Table-10. Number of minimized logic gates for different odd error locator polynomial.

Error locator polynomial	basic circuit	modified circuit 1	modified circuit 2	Number of minimized logic gates
$\Lambda(X) =AX^3+BX^2+ CX+D$	15	9	10	5
$\Lambda(X) = AX^5+BX^4+CX^3+DX^2+EX+F$	23	13	15	8
$\Lambda(X) = AX^7+BX^6+CX^5+DX^4+EX^3+FX^2+GX+H$	31	17	20	11
$\Lambda(X)=A_nX^n + \ldots+A_1X+A_0$	3 + 4n	3 + 2n	3 + (5n-1) /2	2n – (n -1) /2

3.2 Comparison of Circuits

The simulation of the basic and modified circuits is represented respectively in Figures-3 and 4**.**

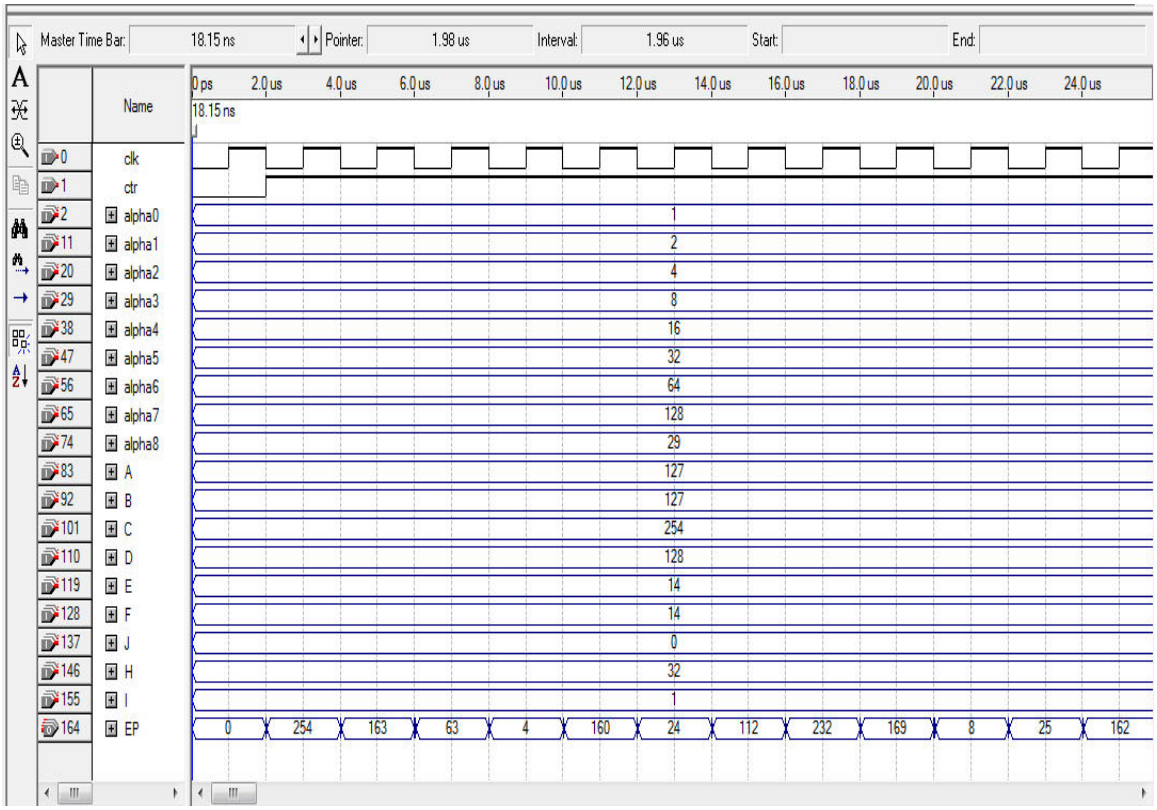

Figure-3. Simulation of the basic algorithm for error locator polynomial as degree 8

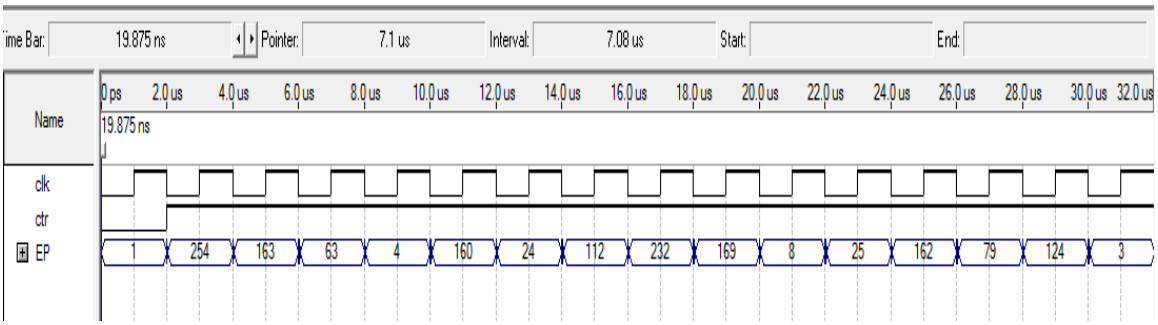

Figure-4. Simulation of the modified algorithm for error locator polynomial as degree 8.

Commensurate with the simulations and tables we have adopted previously, the results we got in the Figure-4 is the same one in comparison with the basic circuit in Figure-3 but with an important number of minimized logic gates. This minimization can reach 30% compared to the basic algorithms.

4. FPGA IMPLEMENTATION

Implementation of a new Chien Search Block for RS and BCH codes has been problematic due to very large amount of resources required we seek to implement a new Chien Search Block on FPGA based on the proposed algorithm to judge the savings in hardware resources [15] [16]. In this paper a parameterized hardware model of the Chien Search Block was developed using the Hardware Description Language (VHDL) and synthesized using Xilinx Synthesis Tool. The block diagram of the proposed algorithm as implemented is shown in Figure-5.

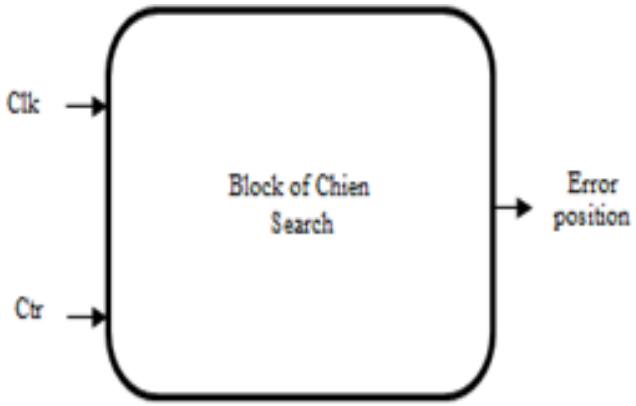

Figure-5. Block diagram of Chien Search block.

The proposed Chien Search Block consists of a global 'Clk' and the error detection process is initiated by

an 'Input', the 'Error position' can be obtained immediately after entering input.

4.1 The New Chien Search Block for RS (15, 11) Codes

This algorithm can detect the error position by calculating $\Lambda(\alpha^{-i})$ where $0 \leq i \leq n-1$, such as $\Lambda(x)$ is the error locator polynomial, calculated by the Euclidean algorithm. To try the first position in the code word, corresponding to $e_j = 14$, we need to substitute α^{-14} into the locator polynomial:

$$\Lambda(x) = 14x^2 + 14x + 1 \quad (5)$$

Where, $\Lambda(\alpha^{-14}) = 14(\alpha^{-14})^2 + 14(\alpha^{-14}) + 1 = 3$

and the non-zero result shows that the first position does not contain an error. For subsequent position, the power of α to be substituted will advance by one for the x term and by two for the x^2 term, so we can calculate the calculations as shown in Table-2. The two sum values of zero in Table-2 identify the error positions correctly as the 6th and 13th symbols, corresponding to the x^9 and x^2 terms, respectively, of the code word polynomial.

4.2 Test Procedure for RS (255, 239)

The proposed algorithm was implemented on a Xilinx Spartan 3E-500 FG 320 FPGA (xc3s500e-5fg320). A comprehensive testing environment was developed to test the implemented algorithm. The test setup is shown in Figure-6.

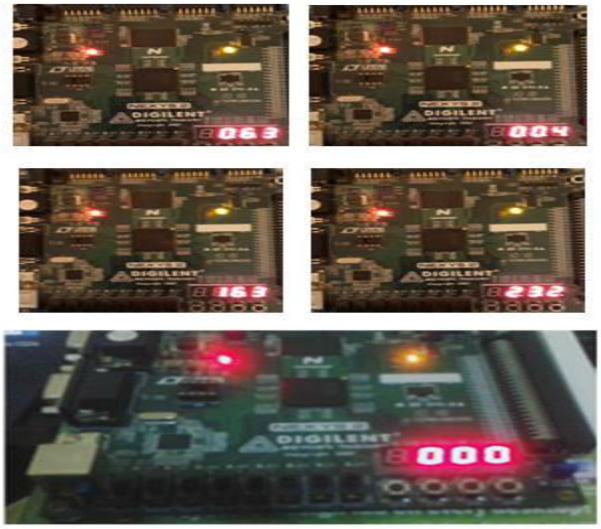

Figure-6. Values of Chien search block for RS (255, 239) codes

The non-zero result in Figure-4 (a) shows that this position does not contain an error, In Figure-9 (b) the value is equal to zero, so this position contains an error.

4.3 Comparison of Algorithms

According to the Table-11, which shows the FPGA device utilization summary for RS (255, 239) by using the two algorithms, we can conclude that: The proposed algorithm presents a low complexity and a very good performance compared to the basic algorithm.

Table-11. FPGA device utilization summary for RS (255, 239).

Recources	proposed algorithm 1	proposed algorithm 2	basic algorithm
Device	**Xilinx Spartan 3E (xc3s500e-5fg320)**		
RS (n, k)	RS (255, 239)		
Number of occupied Slices	90	261	119
Number used as Flip Flops	39	36	95
Number of 4 input LUTs	504	506	196
Number used as logic	504	481	196

5. CONCLUSIONS

A simplified algorithm of Chien Search Block for Reed-Solomon and BCH codes has been presented in this paper. This algorithm is based on a methodic factorization of the error locator polynomial in order to reduce respectively the number of minimized logic gates. The proposed algorithm has been implemented on a Xilinx Spartan 3E-500 FG 320 FPGA (xc3s500e-5fg320). The results show that the proposed algorithm requires reduced hardware resources compared to the basic algorithm.

REFERENCES

[1] M. I. Mazurkov, A. V. Sokolov. March 2019. Constructive Synthesis Methods of Binary Error Correcting Code of Length 32 for MC-CDMA Technology. 62(3).

[2] Zidong Wang, Licheng Wang, Shuai Liu, Guoliang Wei. Jan. 2018. Encoding-Decoding-Based control and filtering of networked systems: insights, developments and opportunities. IEEE/CAA Journal of Automatica Sinica. 5(1).

[3] K. Deergha Rao. March 2015. Channel Coding Techniques for Wireless Communications, Springer Publishing Company, Incorporated, ISBN: 978-81-322-2291-0.

[4] K. Manoranjan, M. Chennaiah, K. PrasadBabu, S. Ahmed Basha K. Sudhakar 2017. Implementation of BCH LFSR Encoder Decoder, I Journals: International Journal of Software & Hardware Research in Engineering. 5: 21-30.

[5] A. El habti, R. El gouri, A. lichioui, H. Laamari. 2015. FPGA implementation of a new BCH decoder used in digital video broadcasting - satellite -second generation (DVB-S2). Journal of Theoretical and Applied Information Technology. 79(1): 22-28.

[6] Zesong Fei, Jinhong Yuan, and Qin Huang. 2018. Error Control Codes for Next-Generation Communication Systems: Opportunities and Challenges, Wireless Communications and Mobile Computing. Vol. 2018.

[7] Walled Abdulwhab, Abdulkareem Kadhim Al-Nahrain. September 2018 Comparative Study of Channel Coding Schemes for 5G. Journal of Electronic Systems. 8(3): 95-102.

[8] M. Shubhangi, B. S. Vaishali. 2019. Implementation of RS-CC Encoder & Decoder using MATLAB. International Journal of Science Technology & Engineering. 5: 22-30.

[9] Y. Lee, I. Park, Omar Mouhib, Y. Hoyoung. 2018. Area-optimized Syndrome Calculation for Reed-Solomon Decoder. Journal of Semiconductor Technology and Science. 18(5): 610-615.

[10] Cesar G. Chaves, Eduardo R. de Lima and Jacqueline G. Mertes. 2015. A Synthesizable BCH Decoder for DVB-S2 Satellite Communications. Journal of Integrated Circuits and Systems. 10(3): 174-180.

[11] M. Elghayyaty, A. Hadjoudja, Omar Mouhib, A. El habti, M. Chakir. 2018. Minimized Logic Gates Number Of Components In The Chien Search Block For Reed-Solomon (RS). American Journal of Engineering Research (AJER). 7(2): 110-116.

[12] N. Kokubun, A. Yamaga, U. Hironori, D. Watanabe. 2019. Circuit-Size Reduction for Parallel Chien Search using Minimal Polynomial Degree Reduction. IEEE XPLORE.

[13] S. Roy, A. Mondal, A. El habti, S. S. Garani. 2019. A Fast and Efficient Two-Dimensional Chien Search Algorithm and Design Architecture. IEEE XPLORE. 23(1): 16-19.

[14] A. El habti, R. El gouri, A. Lichioui and H. Laamari. 2016. Performance study and synthesis of new Error Correcting Codes RS, BCH and LDPC Using the Bit Error Rate (BER) and Field-Programmable Gate Array (FPGA). IJCSNS International Journal of Computer Science and Network Security. 16(5): 21-30.

[15] Jagannath Samanta, Jaydeb Bhaumik, Soma Barman. March 2017. FPGA based area efficient RS (23, 17) codec, Microsystem Technologies. 23(3).

[16] J. Athira, B. Yamuna April 2018. FPGA Implementation of an Area Efficient Matrix Code with Encoder Reuse Method. International Conference on Communication and Signal Processing (ICCSP). pp. 0254-0257.