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DESIGN AND DEVELOPMENT OF 30 KVAR DSTATCOM FOR REACTIVE POWER COMPENSATION IN AN 800 KW RADIAL DISTRIBUTION SYSTEM

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ABSTRACT

This paper presents the design, analysis and development of 30 kVAr DSTATCOM for compensation of reactive power in an 800 kW radial distribution system, feeding power to crucial loads of an educational institution. In this paper the study of radial distribution system is analyzed in terms of electrical power system of institute, power consumption pattern and tariff related issues. We made some conclusions to improve the system performance in terms of power factor and reduction in tariff. The DSTATCOM performance depends on the calculation of the reference source currents that generates the gating pulses of the voltage source converter (VSC) based DSTATCOM. For this purpose the control strategy adopted is IRP (Instantaneous Reactive Power) and SRF (Synchronous Reference Frame) theory and ADALINE is implemented in this system using MATLAB/ SIMULINK software. Generation of the PWM pulses triggers the IGBT of the VSC based DSTATCOM. This is achieved using DSP TMS 320 F 2812, a 32 bit processor that is programmed with CCS V8.0. The performance of the selected distribution system is analyzed experimentally in a hardware prototype to evaluate the effect of DSTATCOM. It is observe that the selected radial distribution system with DSTATCOM provides voltage sag mitigation, reactive power compensation and power factor improvement.

Keywords: DSTATCOM; power quality; reactive power; power factor; point of common coupling (PCC).

1. INTRODUCTION

Reactive power supervision in a power distribution system of a power utility or industry plays a key role in i) reducing distribution loss, ii) maintaining constant distribution voltage and iii) improving power factor. The perfection of power factor enables the reduction of current demand from the Utility resulting in efficient utilization of distribution transformer and reduced electricity bills. The performance of conventional switched capacitors used for reactive power compensation would only give step control and results in over compensation or under compensation for varying loads and changeable reactive power demand. To overcome these problems, in this project, it is proposed to develop a prototype 30 kVAr DSTATCOM for reactive power compensation which would provide instantaneous correction of power factor and always maintains the set power factor. The prototype consists of a power panel with IGBT based voltage source inverter, DC filter capacitor and a DSP based controller along with necessary power supply units, protection cards and firing pulse generating units. By suitable control strategy, the STATCOM would generate leading or lagging reactive volt-amp (VAR) at the PCC (Point of Common Coupling) and avoid problems connected with lag and lead power factor. The power factor can be maintained at the desired level irrespective of system voltage.

A. Objective

The objective of this paper is

a) To Design, simulate and fabricate a +/-30 kVAr prototype DSTATCOM
b) To develop control hardware and software for reactive power compensation
c) To evolve novel testing strategies

B. Project Significance

DSTATCOM is an acronym for Distribution STATic synchronous COMpensator, and forms a member of the family, widely known as FACTS (Flexible AC Transmission System) or Custom Power devices.

Development of DSTATCOM and knowledge of Practical aspects of advanced power electronics enables the research centre in Electrical Engineering Department (EED) to be a unique one with in-house capability to design and develop a FACTS device. The idea of combining capabilities of IGBT-based voltage source converter, DSP based controller and allied power electronics as proposed in the Project ushers in an original generation of FACTS controllers. The present development would open up a path for further studies in the region of other FACTS / Custom Power devices. The know-how gained in the present development will result in tools and techniques for design of other FACTS devices such as, high power STATCOM, Static Synchronous Series Compensator (SSSC), Interline Power Flow Controller (IPFC) and Unified Power Flow Controller (UPFC), Dynamic Voltage Restorer (DVR), active power harmonic filter, active power line conditioner etc. The basic building control block diagram of DSTATCOM is shown in Figure-1. The complete Electrical Substation Layout of sultan Ul-Uloom education society as shown in Figure-2. The incoming supply is 11 kV/440V is divided

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in to two parallel feeders one is 500 kVA transformer feeder and the other feeder connected to 250 kVA transformers. The output of these two transformers feeding power to different loads in the society, in this system to control reactive power it is connected to two automatic capacitor panels one of 150 kVAr to feeder 1 and other of size 125 kVAr to feeder 2. To compensate no load reactive power of transformers a fixed capacitors of 25 kVAr directly connected to 500 kVA transformer and 15 kVAr to 250 kVA transformer at the secondary terminals of transformers.

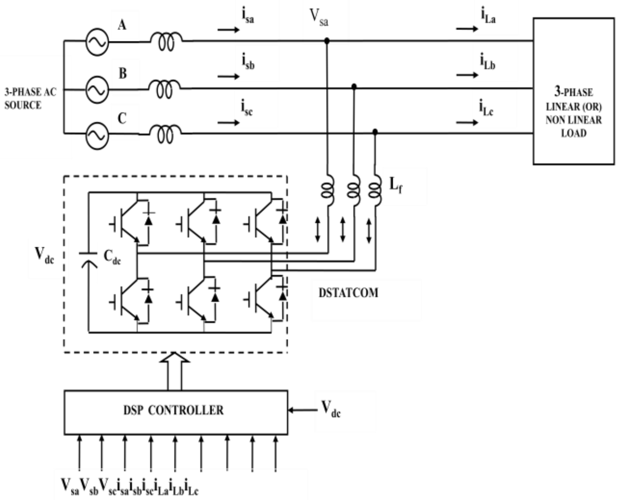

Figure-1. Basic building control block diagram of D-STATCOM.

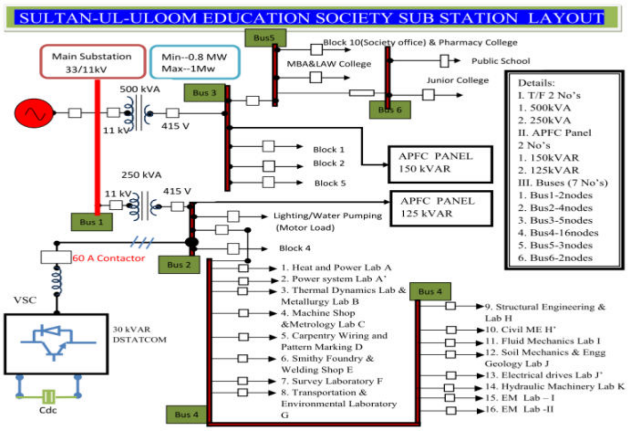

Figure-2. Power distribution of sultan Ul- Uloom educational society.

2. PROBLEM FORMULATION

A Distribution STATCOM (DSTATCOM) is a shunt compensation device used for reactive power compensation. It can be used either in the power factor correction mode or in the voltage regulation mode. The major problem associated with the design of the controller for the DSTATCOM is the selection of appropriate circuit components. The second major problem is to understand the proper working of the controller and control algorithms. It is necessary to understand the design of hardware components and the controller so that the DSTATCOM is effectively used for power quality improvement applications.

A. Design Parameters of DSTATCOM

The Design parameters are considered as design of the choke (interphase inductor), voltage rating, and selection of DC link capacitor, equalizing resistances and pre-charging circuit parameters.

a. Design of the choke: Let us consider a three-phase system with a line voltage V_{LL} of 415 V. The design procedure is explained with respect to a 30 kVAr DSTATCOM connected in shunt with the power system through a coupling inductor .For a 30 kVAr DSTATCOM, V_{LL} (RMS) = 415 V
Rated RMS line current = 42A
Peak value of the line current Ip=42*1.414= 59.39 A

Assuming the ripple current ΔI through the choke to be 20 % of the rated peak current, ΔI = Ip × 0.2 = 60 × 0.2 = 12A, Impedance Z= 5.7142 Ω.

Generally, the impedance of coupling reactor is consider either 15% or 20%. For 15% impedance = 5.7142*0.15=8.8571 Ω and for 20% impedance = 5.7142*0.2=1.1428 Ω.

Coupling inductor value for 15% Impedance = 2. 7296 mh, Coupling inductor value for 20% Impedance=3.6395 mh. Hence, a 3.6395 mH, 42 A choke can be used for this application with a tap of 2.7296 mH, it's hardware model as shown in Figure-3.

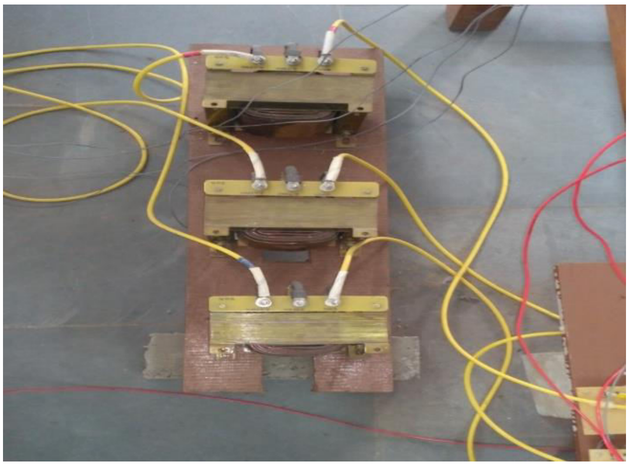

Figure-3. Inter phasing inductor.

b. Pre-charging circuit: The pre charging circuit resistor value, current value and resistor wattage calculations are given below. DC link capacitor voltage (V_{dc}) = 594.2V ~= 595V. Normally we will charge D.C. link capacitor to a full value of 90%. i.e., C_{Dc} = 0.9*595=535.5~= 536V. Each resistor wattage = 10W; each resistor current = 2.27A; each resistor value = 200Ω [10-12]. With out and with delay of pre-charging simulation wave forms are as shown in Figures 4 & 5.

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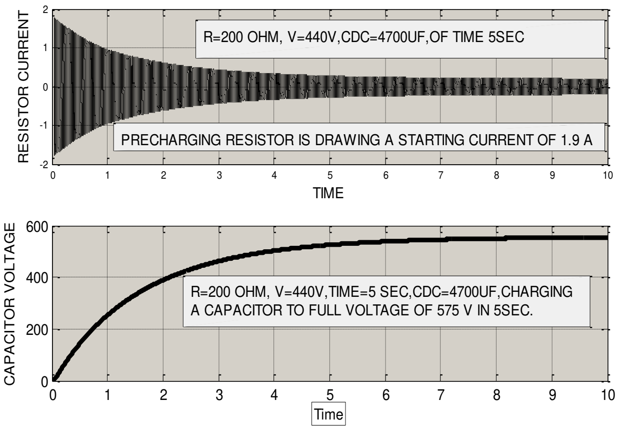

Figure-4. Charging of capacitor with out delay.

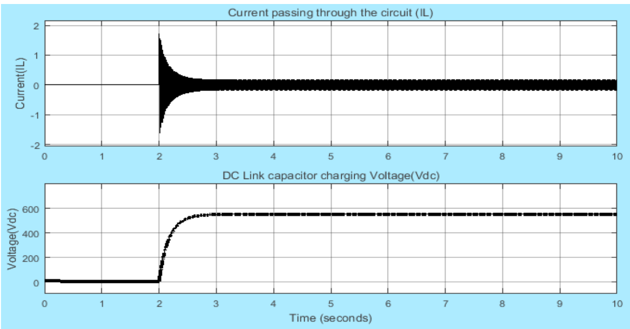

Figure-5. Charging of capacitor with a delay of 2 Sec.

The hardware model of pre-charge circuit is shown in Figure-6. It consists of 220 ohm, 10W three resistors in each phase and a pre-charge contactor of 9A capacity. When the operation starts first the main contactor (63A) is in bypass mode, pre-charge contactor of 9A is in supply. When inverter stack dc link capacitor is fully charged it bypasses the contactor form pre-charge (9A) to main contactor (63A), the main switch will be ON continuously. Only the action will be take in between pre-charge and main contactor. If any problem is occur in the control the DSP timer will give trip signal to main contactor, so the entire system will be in OFF state.

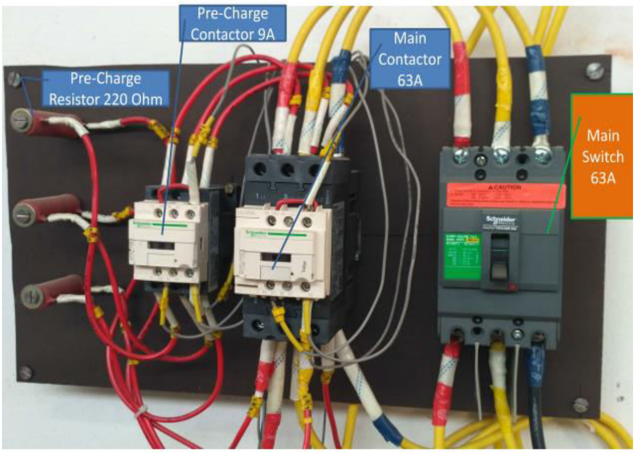

Figure-6. Hardware model of pre-charge circuit.

3. CONTROL OF DSTATCOM

The control of DSTATCOM in this paper can be divided majorly in to IRPT, SRF and ADALINE control, out of these three controller first two can be compared with DSP controller and all three can be done simulation using Matlab/Simulink software and presented the results. The Instantaneous Reactive Power Theory (IRPT) control methodology can be adopted from [5-9].

A. Control of DSTATCOM using SRF Method

In this SRF control first the line currents can be converted to d, q quantities and using LP filter and gains the equivalent direct axis real and reactive currents can be calculated , from this the reactive current requirement can be estimated. Simultaneously the DC side voltage control also can be done using dc side PI controller and ac side voltage can be controlled using the ac side PI controller from this two ac and dc side PI controller the reference supply side direct axis and quadrature axis currents can be estimated. These currents can again converted using reverse conversion of d, q to a, b, and c then after we will estimate the reference source currents. By taking actual line currents subtracting from reference we will be able to generate actual reference control signal currents this complete process as shown in Figure-7. After generating the actual reference currents using sine PWM control generate the firing pulse for the turn on and turn off of the inverter stack. With this the SRF control will be able to control the reactive power in both linear and non linear loads the corresponding conversion mathematical equations can be taken from reference [7-10].

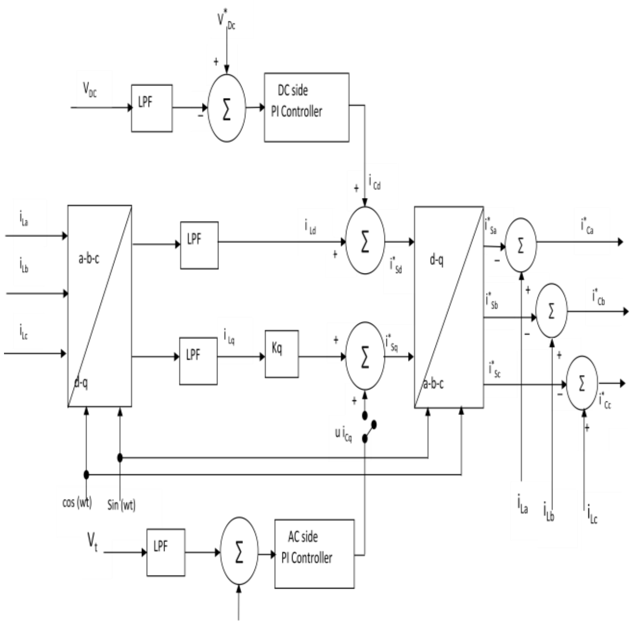

Figure-7. SRF control block diagram.

B. Control of DSTATCOM using ADALINE Adaptive Control Algorithm

Basic adaline decomposer control is based on Least Mean Square algorithm, and training through Adaline Sensed load current that is made up of real

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current (ip+), reactive current (iq+) for positive sequence, and negative sequence current (i−) can be decomposed in parts as

$$i_L = i_p^+ + i_q^+ + i^- \tag{1}$$

This control algorithm is based on the extraction of current component in phase with the unit voltage template. It tracks the unit voltage templates to maintain minimum error

$$i_L(k) - W_p(k) * u_p(k) \tag{2}$$

The estimation of weight is given as per the following iterations

$$W_{p(k+1)} = W_{p(k)} + \eta * \{i_{L(k)} - W_{p(k)} * u_{p(k)}\} * u_{p(k)} \tag{3}$$

A comparison of the sensed dc bus voltage to the reference dc bus voltage of VSC results in a voltage error, which, in the nth sampling instant, is expressed as

$$V_{dcl}(n) = V_{dc}^*(n) - V_{dc}(n) \tag{4}$$

This error signal V_{dcl} (n) is processed in a PI controller, and the output $\{I_p(n)\}$at the nth sampling instant is expressed as

$$\mathrm{I_p(n) = I_p(n-1) + K_{pdc} * \{V_{dcl}(n) - V_{dcl}(n-1)\}}$$
$$\mathrm{+ K_{idc} * V_{dcl}(n)} \tag{5}$$

Where K_{pdc} and K_{idc} are the proportional and integral gains of the PI controller. The control block diagram of ADALINE is shown in Figure-8.

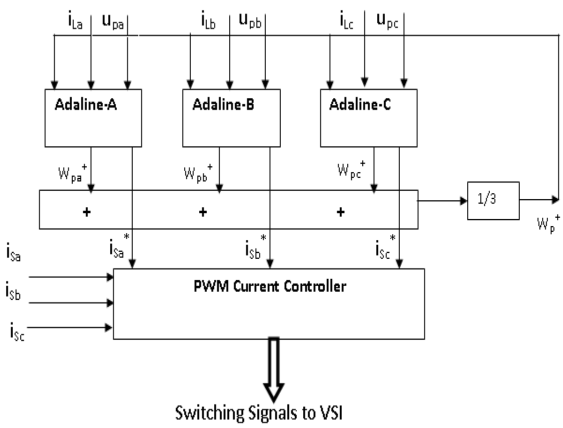

Figure-8. ADALINE control block diagram.

C. DC Link Voltage Control

To regulate the DC link voltage a PI and a fast acting PI closed loop controller are used signals from PI controller is to control the DC link voltage is expressed as

$$u_c = K_p * (v_{dcref} - v_{dc}) + K_i \int (v_{dcref} - v_{dc}) \tag{6}$$

The conventional PI controller used for maintaining the dc-link voltage as shown in Figure-9.

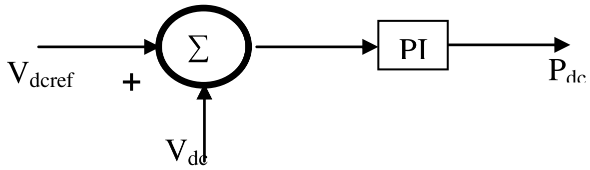

Figure-9. Conventional DC link voltage controller.

$$p_{dc} = K_p * (v_{dcref} - v_{dc}) + K_i \int (v_{dcref} - v_{dc}) dt \tag{7}$$

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is shown in Figure-10.

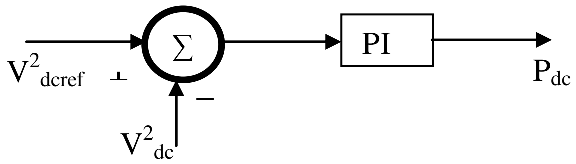

Figure-10. Fast acting DC link voltage controller.

The energy required by the dc-link capacitor to charge from actual voltage to the reference value is given as

$$w_{dc} = 0.5 * C_{dc} * (v_{dcref} - v_{dc}) \tag{8}$$

The total dc power required by the dc-link capacitor is computed as follows:

$$p_{dc} = K_{pe} * (v_{dcref}^2 - v_{dc}^2) + K_{ie} \int (v_{dcref}^2 - v_{dc}^2) dt \tag{9}$$

Figure-11. Shows the complete setup of DSTATCOM

4. EXPERIMENTAL SETUP SPECIFICATIONS

- System capacity = 800 kW
- The main line is connected to two transformers - 500 kVA and 250 kVA.
- Total reactive demand for the system is approximately 300 kVAr.
- Existing systems are provided with 150 kVAr & 125 kVAr Automatic Power Factor Correction panels.
- A 30 kVAr D-STATCOM is proposed for power factor correction. (riding over existing 275 kVAr APFC panel)
- **AC supply source:** Three-Phase, 415 V (L-L), 50 Hz.
- **Source Impedance of:** Rs = 0.04 Ohm and Ls = 2 mH. (calculated from cable ratings)
- **Loads:** Linear / Non linear Loads

- **Load Types:** 1. Different types of Motor loads, UPS, Fan and Lighting load of Educational institute.
- Rating of VSC = 30 kVA.
- Switching frequency of inverter = 5 kHz.
- **Reference dc bus voltage:** 700 V.
- DC bus Capacitance (C_{dc})=4700 µf @ 450V Series connected = 900V.
- Interfacing inductor (L_f) = 3.6395 mH (at 20% tap) with a tap at 2.7296 mH (at 15% tap)
- **Gains of DC bus voltage PI controller:** k_{id}=0.9 and k_{pd} = 3.1.
- **Gains of AC voltage PI controller:** K_{pt}=2.95 and K_{it}=4.

Figure-11. Complete test setup model of DSTATCOM.

5. MODELING AND SIMULATION RESULTS

In this section, the system is modeled in three modes i). Control of DSTATCOM in IRP, ii). Control of DSTATCOM in SRF &iii). Control of DSTATCOM in ADALINE Adaptive control. The detailed result analysis for different load conditions with and without DSTATCOM for fixed and varying loads was analyzed in this section.

A. Without DSTACOM

In this section the system is simulated without controller with a load of quarter, half, ¾Th and full load and the obtained results of different parameters are shown in Table-1.

Table-1. Load details without controller.

TYPE OF LOAD (RL)	QUARTER LOAD	HALF LOAD	¾Th LOAD	FULL LOAD
SOURCE CURRENT (A) (RMS)	299	617	982.2	1357
ACTIVE POWER (kW)	200	400	600	800
REACTIVE POWER (kVAr)	79	192	372	558
POWER FACTOR	0.93	0.9	0.85	0.82

Varying load of all above four linear loads, switching at different time period with the help of three phase circuit breakers, Base load is on through out the whole simulation time, i.e. 2 seconds, Base load: 600 kW, 372 kVAr 0.85 power factor lagging. Load 1: 800 kW, 558 kVAr, 0.82 power factor lagging, Duration 0.4 seconds to 1 seconds, Load 2: 400 kW, 192 kVAr, 0.9 PF Lag, Duration 0.7 seconds to 1.2 seconds Load 3: 200 kW, 79 kVAr, 0.93 PF Lag, Duration 1.3 seconds to 1.7 seconds These variations (varying loads) as shown in Figure-15.

B. With DSTATCOM

The control of DSTATCOM is executed by using DSP TMS 320 F 2812, it is directly connected to personal computer (PC) with JTAG Emulator, the programming is done through CCS V8.0. first using the signals of current and voltage sensors the reactive power is calculated from obtained and calculated using DSP programming, after that using the theories mentioned earlier, like SRF using gating signals the inverter stack should be fired and required amount of reactive power is pumped or injected and maintain the system power factor to unity. After compensation using DSP with SRF controller the main substation electricity energy meter shows UPF as shown in

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Figure-12. The complete hard ware DSTATCOM model as shown in Figure-13.

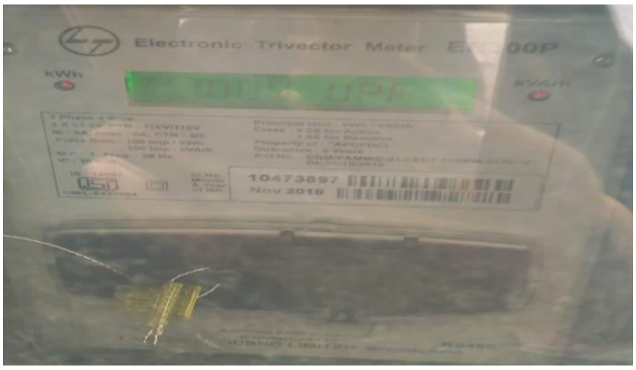

Figure-12. TSSPDCL substation energy meter showing UPF.

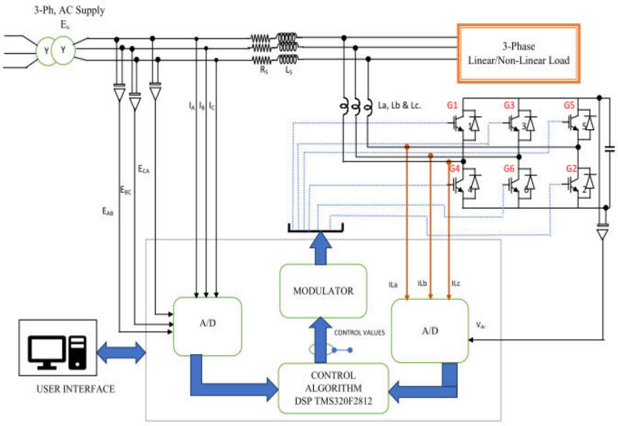

Figure-13. Complete hardware diagram of DSTATCOM.

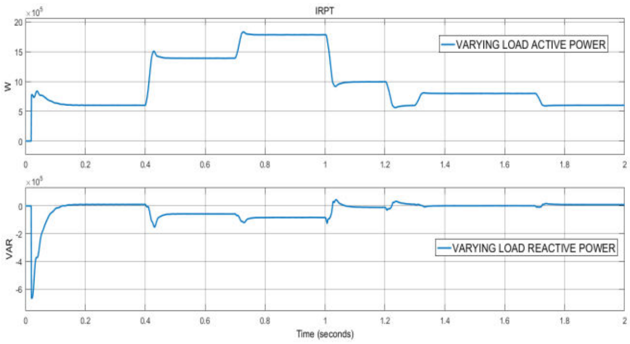

Figure-14. Varying load Active and reactive power.

Fast acting PI Controller has lesser rise time, and improved stability, lesser ripples when compared to conventional PI controller. The response time of Fast acting PI controller is better than that of Conventional PI controller. We have considered one of the loads for implementing this improved PI controller. Quarter Load has been considered for that, the Figure-15. shows us the comparison of 2 different DC link voltage applied on same load for IRPT, and the response times for conventional PI controller is 507 ms and that of fast acting PI controller is 195 msec. The reactive power injections of 3/4th load and full load as shown in Figure-16. The corresponding variable load real and reactive powers are shown in Figure-17. The variations of the angle between voltage and current of phase A with a half and quarter load with out controller as shown in Figure-18. Clearly it is showing that without controller the phase angle between voltage and current of phase A, the power factor of the different loads shown in Table-2. The correction of power factor an and the zero phase angles are shown in Figures 19, 20 & 21.

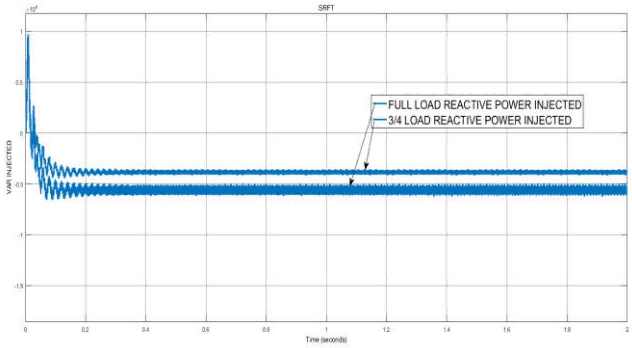

Figure-15. Conventional and fast acting PI controller.

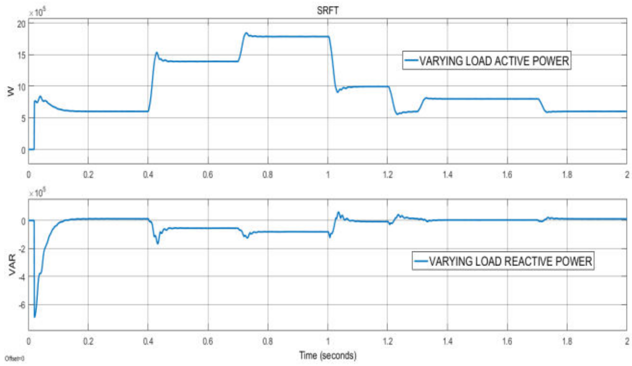

Figure-16. Reactive power injections at PCC for 3/4Th and full load conditions.

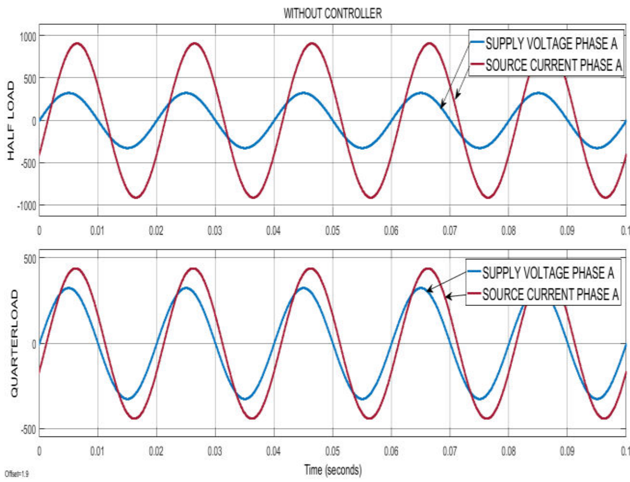

Figure-17. Varying load of real and reactive powers.

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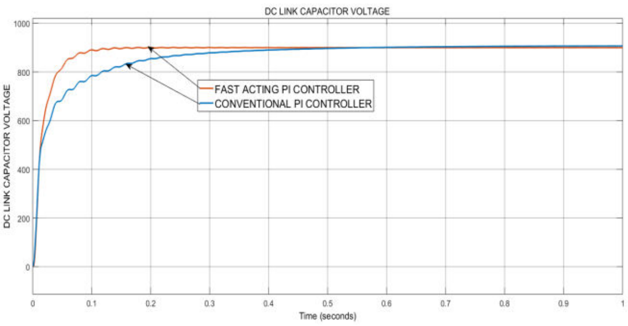

Figure-18. Voltage and current wave forms of Phase A shows power factor angle.

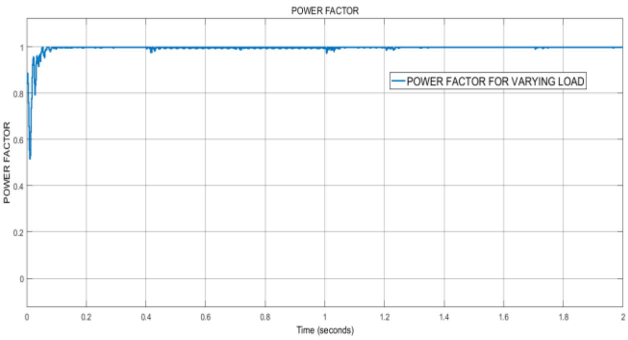

Figure-19. Power factor of varying load with controller showing UPF.

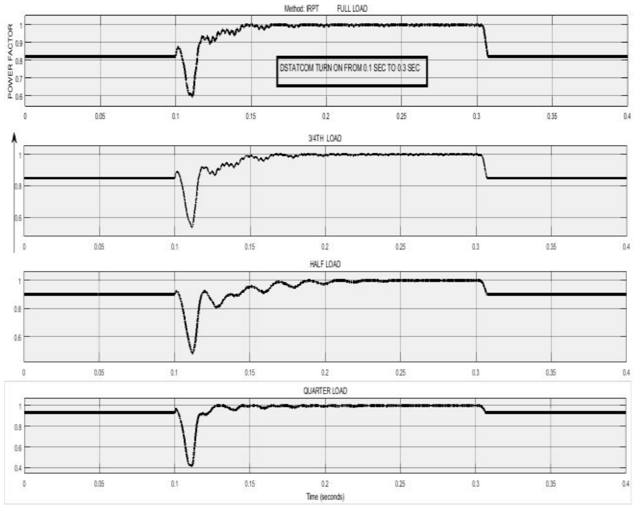

Figure-20. Power Factor of system with out and with controller.

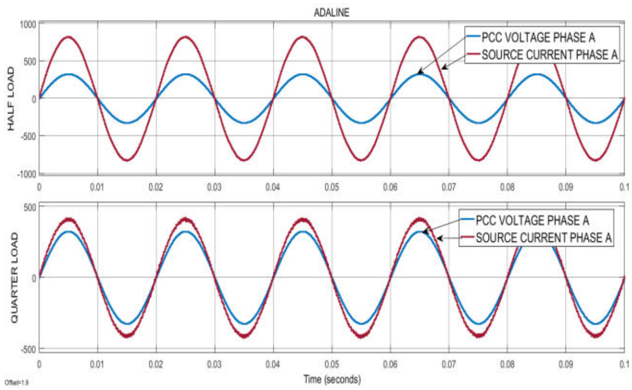

Figure-21. Wave form of the voltage and current of phase a with ADALINE controller.

The complete energy consumption details of the substation is taken from monthly energy bills.

Table-2. Power factor and correction time of different Load conditions with different controllers.

Loads	**Quarter Load (200 kW)**			
Methods	**Without Control**	**IRPT**	**ADALINE**	**SRFT**
I_S(RMS)	299	278.37	278.35	278.39
Response time(ms)	------	28	22	29
PF	0.93	0.9996	0.9996	0.9994
Loads	Half load (400 kW)			
I_S(RMS)	617	556.74	556.69	556.77
Response time(ms)	----	48	46	71
PF	0.90	0.9996	0.9996	0.9995
Loads	¾ th load (600 kW)			
I_S(RMS)	982	1193.92	1193.84	1193.93
Response time(ms)	---	47	44	50
PF	0.85	0.9998	0.9999	0.9998
Loads	Full load (800 kW)			
I_S(RMS)	1357	1113.03	1113.01	1113
Response time(ms)	----	47	44	49
PF	0.82	0.9999	0.9999	0.9999

6. CONCLUSIONS

In this paper a three phase radial distribution static synchronous compensator (DSTATCOM) is implemented using for its functions such as power factor correction and voltage mitigation for linear and nonlinear load conditions. The simulation is carried out in MATLAB/Simulink environment. For comparison the parameters considered are source current, PCC voltage, Active power, injected reactive power, response time (milliseconds) and power factor for linear and nonlinear loads. For comparison a hardware model done with PQ theory in DSP TMS 320F2812 for nonlinear load, the power factor maintained unity with the help of DSTATCOM. The gating signals are generated by a Sinusoidal PWM technique. From the simulation results it can be concluded that ADALINE control algorithm provides a better performance in both the cases when compared to SRFT control strategy. From hardware results the PQ control algorithm provides a simple and better performance in both the cases when compared to IRPT control strategy.

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