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DEVELOPMENT OF OPTIMIZED VOLTAGE LEVEL SHIFTER FOR NANOSCALE APPLICATIONS

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ABSTRACT

Multi voltage clustered systems are the basic and vital power decrease techniques, these approaches employs Level shifters to interconnect "Multiple voltage domains" to reduce power in core/module level. The Level Shifter may considered as area, power and delay overheads when its own power, delays are high. We proposed a circuit technique with broad shifting range for Nanoscale applications. In this brief, for minimization of current contention to attain both efficient and robust level shifting, we introduced new LS with series of Diode current limiters, which minimizes the dynamic power and propagation delay. Implementation of the LS in 130nm technology makes the proposed LS in accomplishing both efficient and robust level shifting from deep sub-threshold voltage 0.15V to supply voltage 1.25V. The developed LS have attained an average propagation delay of 6.20ns, Energy efficiency of 26.5fJ.
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Keywords: level shifter, power, delay, near-threshold, current limiter.

1. INTRODUCTION

The uses of portable/handheld electronic gadgets like cellular phones, multimedia cameras, and pace makers are increasing rapidly day by day, and power consumption has to be reduced at system level to attain more user satisfaction. The ultimate solution is Multi VDD systems and System-on-Chip (SoCs) [1-3]. These are becoming more popular and common in many practical applications. Such a multi VDD and SoCs are needed to be operated with different supply voltages. For such compute theory, energy and power consumptions are crucial design elements. Both the power and Delay of a digital IC depends on its supply voltage.

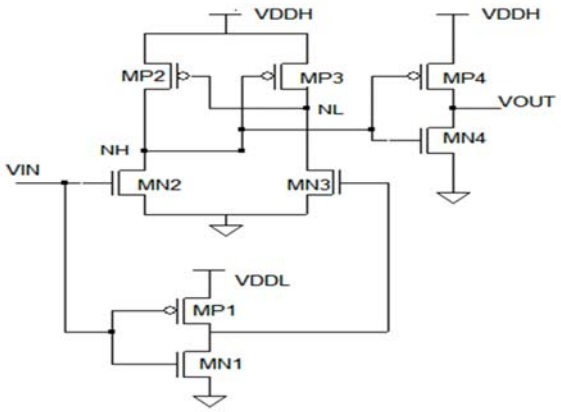

Figure-1. DCVS level shifter.

Level Shifter (LS) is necessary and widely placed among various voltage designs for multiple supply voltage domains. Considering this, to operate in a broad dynamic range the LSs are chosen, at which the near-threshold input scenarios are contained in it. Majorly, the previous LS design which is based on the "Differential Cascade Voltage Switch (DCVS)" LS design in Figure-1 is difficult for shifting from near-threshold to super- threshold, because of the prior current contention caused which is due to the limited drivability of the pull down devices operated in the near threshold region. Generally, when the input signal scales below threshold voltage, the conversion failure is caused due to the contention.

2. REVIEW ON EXISTING LEVEL SHIFTERS

By utilizing intermediate power rails in multistage LS circuit design [4] which reduces the contention in every stage. In general, generation of the multiple voltage supplies through regulators is expensive in many aspects. Thus the area and power overheads are overpowering due to boosting of pull down devices channel width, which is beneficial for good performance and efficient level conversion operation by using well desired appropriate design techniques [5].

The LSs in [6-12] useful in wide range shifting application, and having a provision for bidirectional level shifting, balancing transition time delays, and it poses DCVSL kind of circuit topology utilizes dual power supplies. Being dual power supplies routing congestion may occurs at physical design. The DCVS LS acts as a ratioed circuits and the contention among pull-up and pull-down networks turn out to be severe when input voltage are in the below sub threshold levels, which makes the transistor sizing impractical to obtain a proper level shifting [13]. To address this problem, several improvements have been proposed in [13-17]. The LSs in [13-17] are designed and optimized in 130nm technologies to meet the contention issues, can be considered as state of art circuits to convert deep sub threshold to I/O levels.

In this brief, for minimization of current contention to attain both efficient and robust level shifting, we introduced new LS with NMOS current limiter which minimizes the dynamic power and propagation delay. Implementation of the LS in 130nm technology makes the

proposed LS in accomplishing both efficient and robust level shifting from deep sub-threshold 0.15V to supply voltage 1.25V.

3. PROPOSED DYNAMIC VOLTAGE LEVEL SHIFTER

The developed LS consisting of an inverter at input side, which is responsible for providing differential small voltages and voltage shifting operation is performed by improved DCVS LS, and an output buffer is added to increase the driving strength of output, depicted in Figure-2. The key concept in the main voltage conversion stage is addition of two NMOS current limiters MN3 and MN5 in the pull up design to weaken the current contention. In the above design the ratio of NMOS to PMOS is reduced to 1 and the area optimization could obtained in comparison with conventional and state of art LSs, The device aspect ratios are very supportive and symmetrical chip fabrication can be obtained, Table-1.

Table-1. Sizing of MOSFETs of the proposed LS.

PMOS	W/L(nm)	NMOS	W/L(nm)	NMOS	W/L(nm)
MP1	150/130	MN1	150/130	MN5	150/130
MP2	160/130	MN2	150/130	MN6	150/130
MP3	160/130	MN3	150/130	MN7	150/130
MP4	150/130	MN4	150/130	MN8	150/130

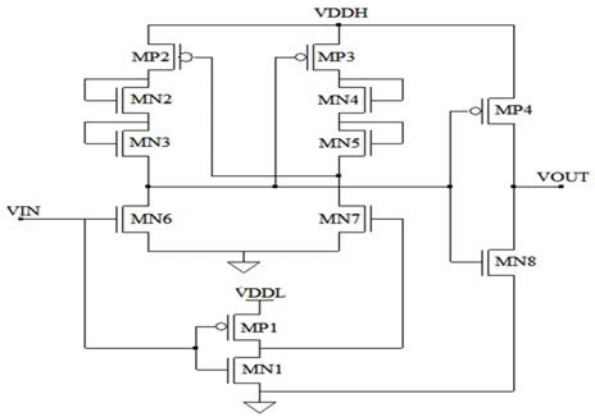

Figure-2. Schematic of optimized level shifter.

The current limiters MN2 and MN4 transistors weakened the current contention in the pull up. When the input VIN is at low to high transition, MN6 makes pull-down, despite of weak strength of pull down transistor. This will not supportive to produce full swing, this will invert to the output node by MN4-MP4 inverter with full swing (VOUT) [1]. When the input VIN is at high to low transition a short circuit current in output inverter may increase, to avoid another pair of current limiters have introduced.

When the input VIN is logic '1', i.e.0.15V, then MN6 turns ON and the VDDL inverter produces strong logic '0', which makes MN7 OFF. As MN6 is ON the load inverter produces the strong logic '1', i.e. 1.25V (VDDH) through pull-up MP4 ON. As the swing is low in the main conversion stage and current is limited by the current limiters the better delay power consumption could able to achieve. Here the complementary LS design helps for forming the feedback and it guarantees the correct functionality of the LS. The output inverter produces strong '1' and double diode current limiters ensure the contention mitigation for better Power and delay, wide voltage conversion range from 0.25V to 1.25V could able to achieve with contention mitigated LSs.

4. RESULTS AND DISCUSSIONS

4.1 Functional Simulation

The functional simulation of the optimized voltage level shifter for nanoscale applications is depicted in the Figure-3. The quality of the output in terms of level shifting from 0.25V to 1.25V and the power consumed by the circuit is only while transitions. As a level shifting, the VIN is at as low as 0.175V to VDDH with capacitive load of 50 fF, average dynamic power and propagation delay is low at frequency 1MHZ input signal.

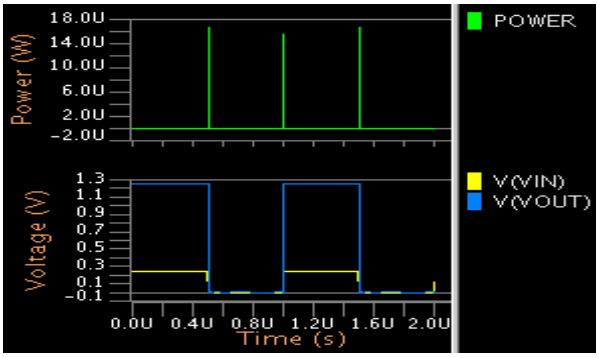

Figure-3. Functional simulation of Proposed LS.

4.2 Characterization of the LS

The Dynamic power consumption and Delay of the proposed LS for Nanoscale application is depicted Figures 4 and 5. The simulation results at 1 MHz frequency prove that the power consumption and delays are almost same for all VDDHs. The power and delay exponentially decreases as VDDL increases. The Dynamic power consumption and Delay of the proposed LS results at 2MHz and 3MHz frequencies are depicted in figures 6 -

7 and 8 - 9 respectively. The simulation results prove that the power consumption and delays are almost same for all VDDHs and decreases exponentially as VDDL increases.

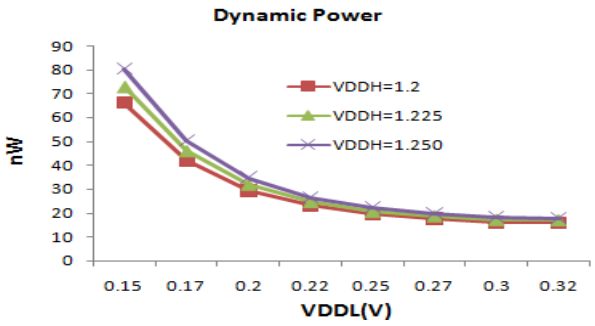

Figure-4. VDDL vs. Power @ 1MHZ.

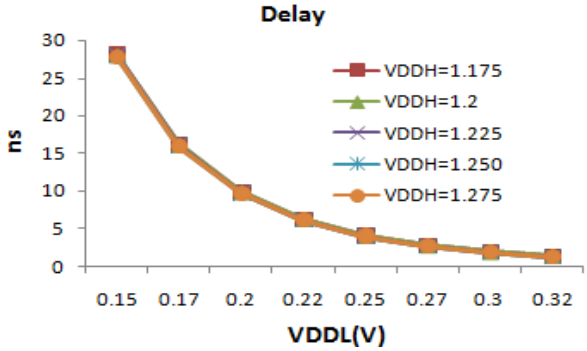

Figure-5. VDDL vs. Delay @ 1MHZ.

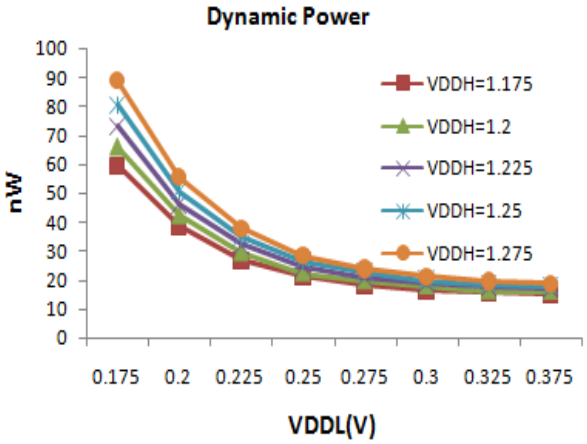

Figure-6. VDDL vs. Power @ 2MHZ.

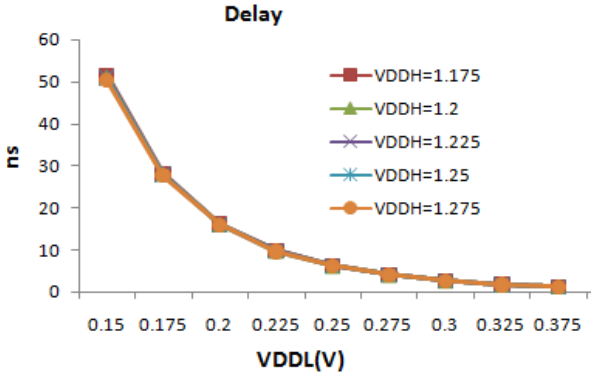

Figure-7. VDDL vs. Delay@2MHZ.

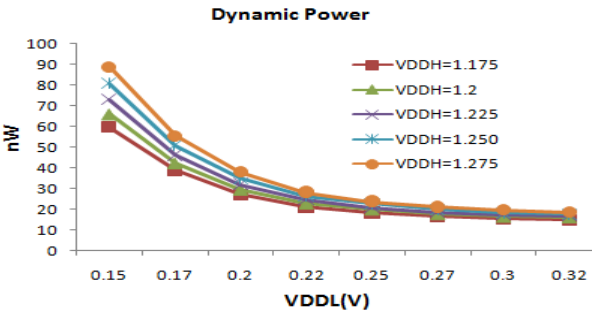

Figure-8. VDDL vs. Power @ 3MHZ.

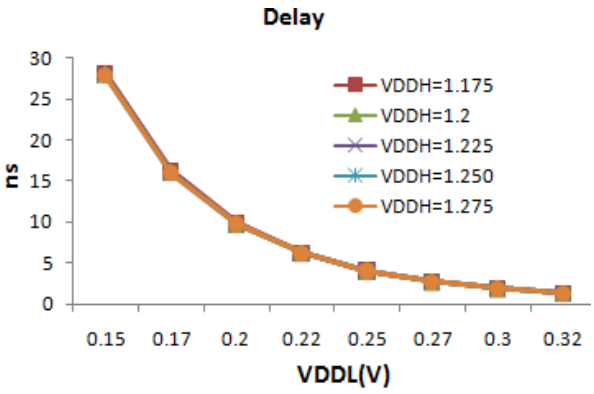

Figure-9. VDDL vs. Delay @ 3MHZ.

The Static power consumption of the proposed LS is depicted Figure-10. The static power consumption is stable for all VDDLs at different VDDHs. Even at higher VDDH the static power consumption is just 6.6nW.

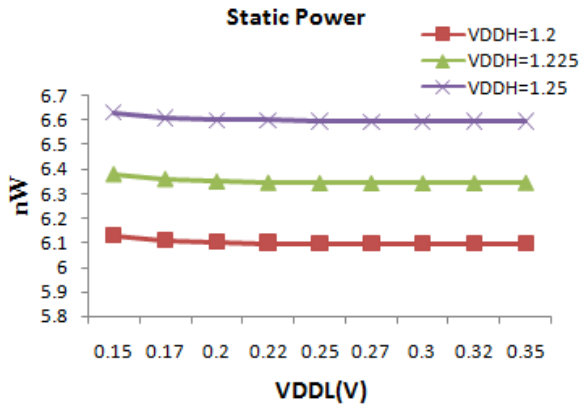

Figure-10. VDDL vs. Static power.

4.3 Comparative Analysis

The quality metrics of the developed level shifter is depicted in the Table-2 and comparable with various LSs. The proposed design is the takeover LS, it has delay of 6.02ns and dynamic power 26.54nW at the frequency of 1MHz. The developed LS outperforms in comparison with existing LSs

5. CONCLUSIONS

Level shifter circuits are essential components in the ultra-low power computing designs. The designed level shifter have two current limiters makes the design so efficient towards power, delay and area. As the power consumption, delay and power delay products are low, suits for all nanoscale applications. Basically the above circuit converts the input signal as small as 0.150V to supply of 1.25V. The developed level shifter achieves an average propagation delay of 6.2ns and 26.5nW dynamic power at shifting from 0.250V input to 1.250V. It is concluded that the level shifter circuit is favorable for Ultra Low power applications with wide voltage conversion range.

Table-2. Performance metrics of LS Designs.

Design/Ref.	Technology	Min. VDDL (V)	VDDH (V)	Delay (ns)	Dynamic power
This work	130 nm	0.15	1.25	6.02@0.25V	26.54nW@0.25V,1MHZ
[13]	130 nm	0.30	2.50	125.0@0.30V	13.6µW@0.30V,8MHZ
[14]	130 nm	0.30	2.50	41.5@0.30V	1145pW@0.30V,5KHZ
[15]	130 nm	0.30	2.50	58.8@0.30V	985pW@0.30V,5KHZ
[16]	130 nm	0.20	1.20	300@0.30V	10pW@0.30V,10KHZ
[17]	130 nm	0.23	3.00	10^4@0.40V	580pW@0.40V,10KHZ

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