VOL. 16, NO. 5, MARCH 2021 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

VOLTAGE REFERENCES FOR LED DRIVER INTEGRATED CIRCUIT

Arjuna Marzuki
School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Penang, Malaysia
School of Science and Technology, Wawasan Open University, Penang, Malaysia
E-Mail: arjunam@wou.edu.my

ABSTRACT

LED driver is an electrical device that provides the required voltage and regulates the constant amount of power to the LED's needs or string of LEDs. This article presents the design and development of voltage references for an LED driver IC. Integrated circuit design in multiple device technologies such as an LED driver requires a built-in voltage reference circuit to convert a high voltage into an appropriate voltages level for internal usage. The design of voltage reference is started with the behavioral modeling of LED driver IC. The obtained parameters from the behavioral modeling were used as the specification for the design of voltage reference in a commercial X-Fab XDM10 1.0 µm 350 V process technology. The circuit consists of a series regulator, bandgap, and opamp-based regulator. It produces 1.2 V for VREF or VH, 0.4 V for VREF_EA, and 0.2 V for VL. The circuit was also used to generate 5 V internal supply voltage, VDD. These voltages vary only by 10 % across PVT.

Keywords: integrated circuit, regulator, CMOS, DMOS.

1. INTRODUCTION

An efficient, affordable, and long-lasting alternative is required to enhance the performance of artificial lighting. Solid-State Lighting (SSL) shows a great promise that meets these features [1]. SSL devices, such as light-emitting diodes (LEDs) and organic LEDs (OLEDs), have improved rapidly. The most important advantages of inorganic LEDs are their very high lifetimes, the controllability (color control and dimming), saturated colors, robustness, small size, and high efficacy [2].

Compared with fluorescent lamps, an attractive feature of LEDs is longevity, which is typically 100,000 hours [3], [4]. The lifetime expectancy is much longer than that of fluorescent lamps, typically 10,000 - 20,000 hours. A Fluorescent lamp, although much more efficient than an incandescent light bulb, is not really very environmentally friendly. Fluorescent bulbs are made with mercury and pose a danger to our environmental health. There is currently no efficient recycling program for these toxic fluorescent bulbs. The mercury then seeps into our water tables and becomes a part of our environmental food chain that indeed not a very green choice. LED light bulbs are the most environmentally friendly light source. As the LED technology evolves, the possibilities for new and more intelligent products enlarge the demand for more specific features from the controller-based LED drivers. The applications involving LEDs are innumerable, and its varieties impose a clear demand on the design of controllable LED drivers.

LED driver is an electrical device that regulates the power to an LED or LED in series. It responds to the ever-changing needs of the LED by supplying a constant amount of power to the LED as its electrical properties change with temperature compares with conventional power supplies [5], [6], and [7]. Two approaches are currently commonly used to generate adequate forward bias for LED; a step-up converter or a step-down converter. For the step-up converter, the capacitor-charge pump [8] and inductor-based boost circuits are popular. For the step-down converter, an inductor-based buck circuit topology is more practical.

One of the standards AC supply is 220 V AC - 240 V AC at 50-60 cycles. These AC voltages will be rectified to DC voltages. A buck converter is a DC-DC converter that steps down DC input voltage to a required DC output voltage [9]. This type of converter is better when considering transformer losses. Along with the fact that higher commutation frequency can significantly reduce the transformer's size, it decreases prices and increases efficiency.

The LED driver design requires high voltage as the input voltage, and the LEDs required low voltage from the output voltage. The application of a single white LED as a portable lighting device requires a high driving forward voltage and a high driving current. A white LED is a current-driven device whose brightness is proportional to the conduction current. The conduction current is typically regulated to avoid exceeding the rated maximum current and to obtain a constant luminous intensity [10]. In order to decrease the size and weight of these devices, miniaturization of the LED driver modules is essential. As a result, the trend is to focus on CMOS implementation of converters with low power consumption [11].

The focus of this work is to implement the voltage references circuit for a LED driver IC. The work is an attempt to reduce the external components of the LED driver IC. A behavioral modeling approach was used in the determination of the voltage reference specifications. This approach is believed to be able to reduce the design time of the LED driver IC.

This paper is organized as follows. Section 2 discusses the background aspect. It covers LED driver specification, behavior model, the concept of LED driver IC and the proposed voltage references circuit. The implementation of the CMOS implementation is discussed in section 3. Section 4 discusses the results. This paper is finally concluded in the conclusion section.

2. BACKGROUND

There are two parts of the voltage reference circuit design. The behavioral modeling technique is used to verify the top-level requirement of the voltage reference circuit. Based on the system level's verified parameters, it was then used as the specification in the transistor-level design.

2.1 LED Driver IC Specifications

Pulse width modulation (PWM) is a popular approach in controlling the LED brightness. A PWM signal's frequency must be above 100 Hz to ensure that the PWM pulsing is not visible to the human eye. The PWM signal is generated by using a ramp signal with high limit voltage, VH, and lower limit voltage, VL. Table-1 lists the top-level LED driver specifications.

Table-1. Specifications of LED driver IC.

Parameters	Specification
Input voltage, VIN	310 VDC
Output current, I_{LED}	350 mA
Output voltage, V_{LED}	50 - 60 V
Current ripple	≤5%

2.2 Behavioral Model of an LED Driver IC

The IC system's behavioral model represents the functionality of an IC with top-level models rather than the actual implementation of the circuit. This technique has great potential for faster and better system verification.

Verilog-A is a hardware design language (HDL) for analog circuit and systems design. This language provides a new dimension of design and simulation capability as an analogous high-level language for analog and mixed-signal circuits and systems. Verilog-A offers a good introduction and exploration of the new level of simulation technology by behavioral modeling technique.

Behavioral models are used to establish system-level behavior. These models' verifications can minimize the potential problems downstream, validating the mixed-signal architecture early in the design process. All modeled functional blocks are translated into transistor level designs. The simulations become faster when the system regressions can be performed by using transistor-level implementation for some blocks while retaining other blocks at higher system levels. Developed behavioral models are recalibrated against the transistor level implementations using post-layout data. Therefore, behavioral models make simulations much faster, but there is a trade-off between performance and actual circuit design accuracy. Highly accurate models usually require significant development effort, and complex models take longer to simulate compared to simple ones. Behavioral models used to improve system verification speed should correlate well to the circuit implementation. The verification of the original circuit implementation requires comparisons against the behavioral model [12].

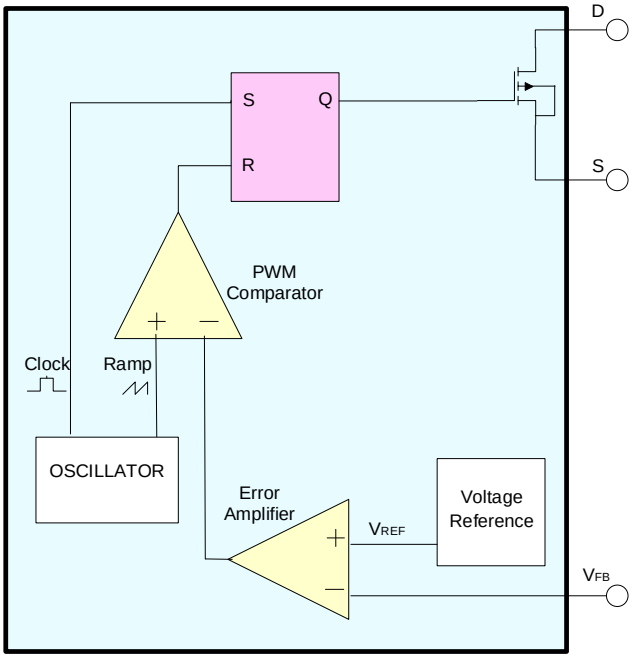


Figure-1. The concept of the control circuit for an LED driver IC with a voltage reference and power transistor.

Figure-1 shows the concept of the control circuit for an LED driver. The close loop control circuit consists of an error amplifier, PWM comparator, an oscillator (ramp and clock signals), and SR latch blocks. The focus on this behavioral modeling for voltage reference is to determine VH, VL, which will be used for ramp oscillator, and VREF for error amplifier (VREF_EA).

2.2.1 LED driver IC modeling

The behavioral modeling for a complete LED driver IC concept is shown in Figure-2.

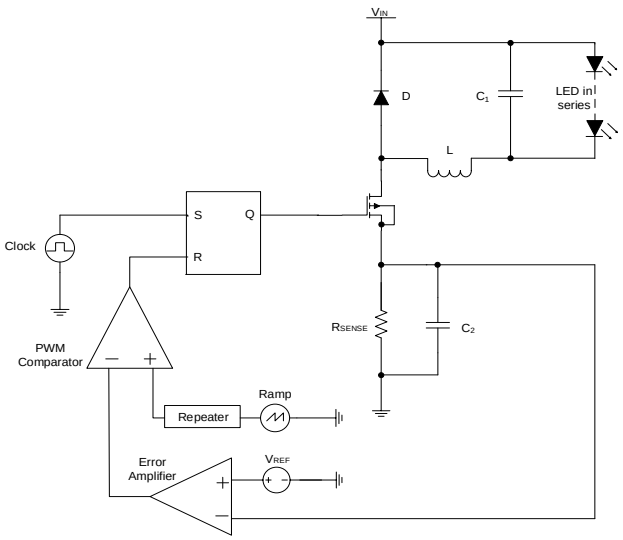


Figure-2. LED driver IC simulation schematic.

In the simulation, the power MOSFET is a DMOS device. Thus a Cadence spectre model is used for the DMOS, while Verilog-A models the rest of the blocks.

The behavioral models for the control circuit of the LED driver are including error amplifier, repeater for the ramp, PWM comparator, and SR latch. The error amplifier modeling is to identify the required gain of the output that crossing the ramp signal between the high limit voltage, VH, and low limit voltage, VL. The oscillator signals for ramp and pulse are generated from voltage sources, including reference voltage, VREF. The repeater is needed for the continuous ramp signal. The DMOS for this topology drives the diode, *D*, inductor, *L*, capacitor, C_1, and LED on the high side and allows current to flow through the sense resistor, R_{SENSE}, at the low side. C_2 is needed to regulate the switching voltage.

The parameters in Figure-2 are depicted in Table-2, and the methodology is similar to [13]. The given top-level specifications are in Table-1.

Table-2. Parameters for behavioral modeling of LED driver IC.

Component	Value
Inductor, *L*	2.6 m*H*
R_{SENSE}	1.1 Ω
Capacitor, C_1	220 n*F*
Capacitor, C_2	1 µ*F*

In the LED driver design, both capacitor values are used to establish output ripple behavior within specification given as in Table-1.

2.2.1.1 Behavioral modeling results

In Figure-3, LED current and voltage do not comply with the specification (as in Table-1) when The VL is fixed at 0.2 V, while the VH is varied from 1.2 V to 5.2 V. The error amplifier (EA) gain is at 10.

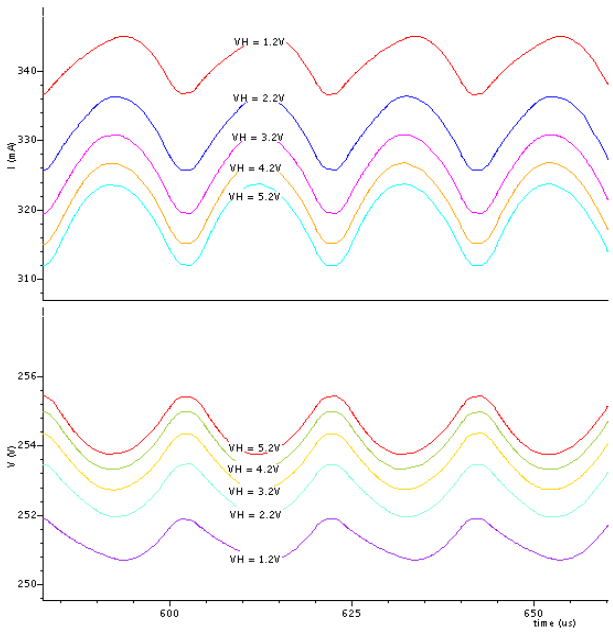


Figure-3. Black and white images must have a resolution.

Figure-4 shows that the LED driver's maximum achieved LED current and LED voltage is 348 m*A* and 59 *V*, respectively. The EA gain is 100.

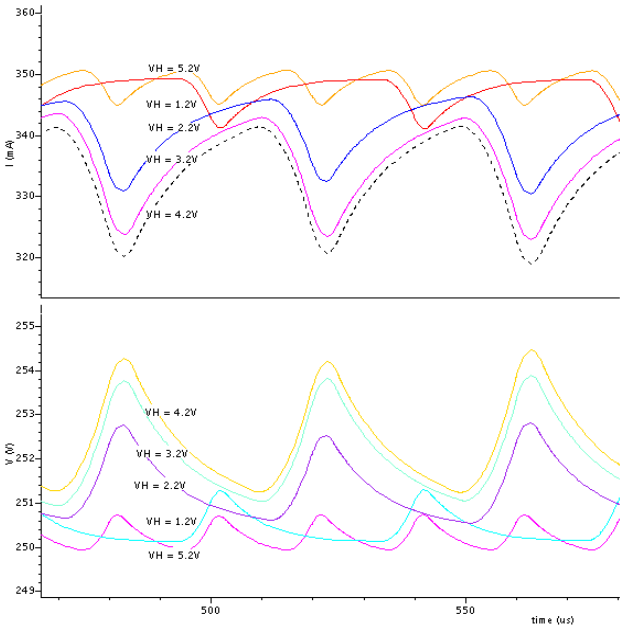


Figure-4. ILED and VLED for the LED driver for different VH with VL = 0.2V, gain = 100.

As shown in the simulation results, the modeled driver's ripple output is less than 5%. This ripple is affected by the selected frequency, inductor, and capacitor values. Increasing the inductor and capacitor values reduces the ripple but increases the costs.

Table-3 lists the key performance model parameters for the LED driver IC. VREF_EA is slightly higher than the voltage at R_{sense}(when current is 350 mA).

Table-3. Behavioral model performance parameters.

Parameters	Value
VH	1.2V
VL	0.2V
VREF_EA	V

2.3 The LED Driver IC Concept

The control circuit for the LED driver IC will be integrated using the XDM10 process for the intention to reduce the size and weight while maintains the projected lifetime of LEDs and enable high-frequency switching.

For power device selection, turn-on resistance (R_{on}) should be considered to get better efficiency. Thus, the first thing to carry out is to reduce R_{on}. Besides, in the light load scenario, the power consumption caused by dynamic switching and the static current also plays a role. The dynamic power consumption of CMOS logic is proportional to the number of transitions of load, voltage swing, and frequency of switches. Therefore, reducing

operation frequency by the control circuit will provide better efficiency in the light load scenario.

Assume the power loss of those discrete components besides transistors is negligible. Referring to equation (1), if the efficiency is expected to be greater than 90%, Ron must be at least one-tenth of the load resistance (R_{load}) [14].

$$\text{Efficiency} = \frac{R_{load}}{R_{load}+R_{on}} \quad (1)$$

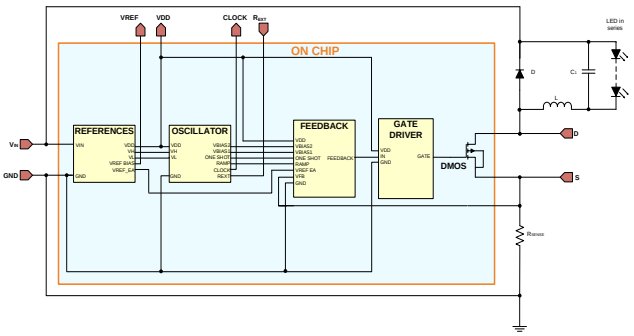


Figure-5. Block top-level diagram design of LED driver IC.

In the block diagram design, as shown in Figure-5, the driver consists of 4 top-level blocks: reference, oscillator, feedback, gate driver, and one switching transistor (DMOS). This paper only discusses the reference block.

2.3.1 Proposed voltage references concept

The basic functional block diagram of the reference is shown in Figure-6. It consists of a series regulator, a VREF_bias, a VREF_start-up, a VREF_amp, and VREF_bandgap, whose output voltage is standard 1.2 V voltage reference (VREF), and a voltage regulator. The other output voltages are VDD (5V), the upper limit voltage, VH, lower limit voltage, VL, and VREF_EA.

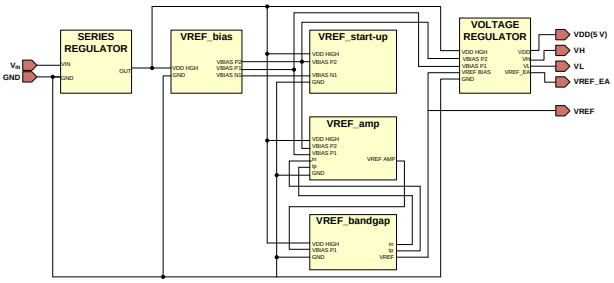


Figure-6. Block diagram of voltage references.

The series regulator is a circuit used to provide high VDD for the rest of the block in the voltage references circuit. The input voltage, V_{IN}, is a rectified AC voltage. VREF_bias is used to provide voltages for gates in VREF_amp and voltage regulator. VREF_start-up is a start-up circuit for the VREF_bias. The start-up circuit should be used only to direct the cells to its correct operational point. The VREF_amp is used together with the VREF_bandgap to produce a bandgap voltage, VREF. The reference voltage should be stable in variations of the process, supply input voltage and junction temperature [14].

3. PROPOSED VOLTAGE REFERENCES

3.1 Design Specification and Technology

The proposed design takes unregulated 310 VDC input and provides the regulated output voltages to the LED driver IC's internal circuitries. The desired regulated voltages are VH, VREF_EA, and VL. This is depicted in Table-4. This table is generated from Table-3 with an additional parameter, VDD.

Table-4. Desired values of the regulated voltage.

Reference Voltage	Value
VDD	5
VH	1.2V
VL	0.2V
VREF_EA	0.4 V

The proposed design has been implemented using X-Fab XDM10 technology [15]. There are several different types of devices used in the design. The DMOS device, which is *nd32a*, is a 350V high voltage device. The NMOS and PMOS are called *nme* and *pme*, which are 20 V medium voltages devices. Only one type of bipolar transistor was used in the design that is *qna*. This 80 V vertical NPN transistor is used in the bandgap circuit. The passive devices are a poly-poly capacitor called *cpp*, poly resistors called *rpd* and *rp2ltc*, and the special diode is called *dnda*.

3.2 Series Regulator

The series regulator is one type of linear regulator that relies upon an active electronic device's variable conductivity to drop voltage from an unregulated DC input voltage to a regulated output voltage. The series voltage regulator used nd32a transistor (350V HV-DMOS) and a Zener diode D0, dnda type, is shown in Figure-7.

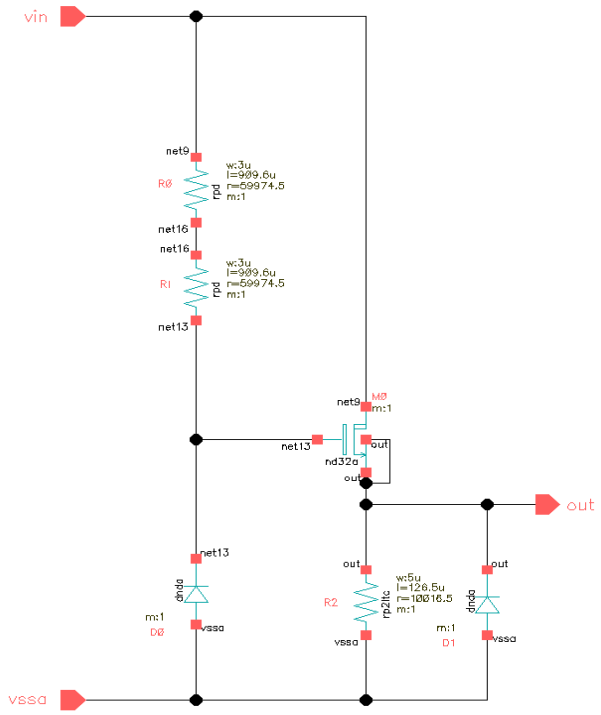


Figure-7. Series regulator circuit.

This circuit is also called a source follower voltage regulator because DMOS is connected in source follower configuration. Here, the DMOS is termed a series-pass transistor. The current in the Zener diode is small because of the current amplifying property of the DMOS. Hence there is a little voltage drop across the diode resistance, and the Zener approximates an ideal constant voltage source. *R*, total resistance between the diode and DC input voltage, V_{IN}, is

$$R = R0 + R1 \quad (2)$$

where *R0* and *R1* are *rpd* type resistors. The current through resistor *R* is the sum of Zener current, I_Z, and the transistor gate current, I_G ($=I_D/\beta \equiv I_{OUT}/\beta$), where β is the current gain of the transistor.

$$I_R = I_z + I_G \quad (3)$$

The DC input voltage, V_{IN}, is fed to the input terminals, and regulated output voltage V_{out} is obtained across the load resistor, *R*2. The diode, *DO* provides the reference voltage, V_Z, and the DMOS acts as a variable resistor, whose resistance varies with the gate current, I_G. The operation of the regulator is based on the change in input voltage appears across the transistor. Therefore, the output voltage tends to remain constant. The polarity of the different voltage is,

$$V_{out} = V_z - V_{GS} \quad (4)$$

The gate-source voltage, V_{GS} of the transistor remains almost constant, equal to that across the Zener diode, V_Z.

For the series regulator's operation, the increased V_{GS} causes the *nd32a* to conduct more current if the V_{OUT} decreases, thereby raising the output voltage and maintaining the output constant. If the V_{OUT} increases, the decrease of V_{GS} causes the *nd32a* to conduct less, thereby reducing the output voltage and maintaining the output constant. The resistor *R2* is calculated using an equation,

$$R2 = \frac{V_{OUT}}{I_{OUT}} \quad (5)$$

The second *dnda* diode, *D*1 at the output stage, is to clamp the overshoot voltage of more than 20 V. The behavior of *dnda*diode at the typical process, when it clamps the voltage, is 16.5 V. When V_{GS} is higher than 0.93 V. The current through *R2* is 1.4 mA. Table-5 shows the resistor values in the series regulator circuit. V_{out} is high VDD and called VDDA for the rest of the circuit.

Table-5. Components.

Component	Value
R0, R1	60 kΩ
R2	10 kΩ

3.3 Biasing Circuit

The independent supply bias is particularly vital in realizing any voltage references in CMOS technology.

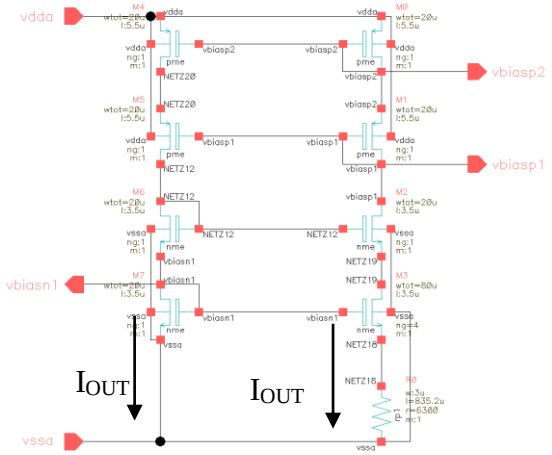


Figure-8. VREF_bias.

A beta multiplier reference (BMR) circuit, as in Figure-8, is an independent supply bias technique that forces the same current through M7 and M3. It consists of two deliberately mismatched transistors M7 and M3. M7 is K times as wide as M3. M2 and M6 are identical. A resistor *R0* is connected series with M3. The resistor determines the bias current I_{OUT} and the transconductance, g_m, its value should be accurate and stable. PMOS devices are used in the Beta multiplier to bias the current mirrors to increase the capacitance on *vbiasp* and further stabilize the circuit [16].

For this circuit, there are three outputs, which are *vbiasp2*, *vbiasp1*, and *vbiasn1*. These nodes are connected to the *vbiasp2*, *vbiasn1*, of the start-up circuit. The three outputs are finally used to bias the operational amplifier circuit (VREF_amp) and voltage regulator. The larger value of β in M3 is to satisfy equation 6 for $V_{GS7}>V_{GS3}$.

$$V_{GS7} = V_{GS3} + I \cdot R0 \quad (6)$$

M7's β is multiplied up in M3 so that the less gate-source voltage is needed to conduct the current, I_{OUT}. This is done using a larger width in M3. Knowing,

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_{THN} \quad (7)$$

$$(\beta = KP_n \cdot \frac{W}{L}) \text{ and}$$
$$\beta_3 = K\,\beta_7 \quad (8)$$

Which is satisfied $W_3 = K \cdot W_7$. The circuit operates as follows:

$$I_{M7}=\frac{KP_n}{2}\left(\frac{W}{L}\right)_7(V_{GS} - V_T)^2 \quad (9)$$

And

$$I_{M3}=\frac{KP_n}{2}\left(\frac{W}{L}\right)_3(V_{GS} - V_T)^2 \quad (10)$$

since that,

$$I_{M7} = I_{M3} = I_{OUT} \quad (11)$$

M7 and M3 are related as in equation 10. Therefore,

$$I_{OUT} = \frac{2}{R0^2 KP_n \cdot \frac{W_7}{L_7}}\left[1 - \frac{1}{\sqrt{K}}\right]^2 \quad (12)$$

$$V_{DS\,sat} = V_{GS} - V_{THN} = \frac{2}{R0^2 KP_n \cdot \frac{W_7}{L_7}}\left[1 - \frac{1}{\sqrt{K}}\right] \quad (13)$$

where $KP_n = \mu_n C'_{ox}$. The MOSFETs' finite output resistance is neglected for I_{OUT} and $V_{DS,sat}$ that is independent of VDDA. When K=4, the circuit is sometimes called a constant g_m circuit.

$$g_m = \sqrt{2KP_n \frac{W}{L} \cdot I_{OUT}} = \frac{1}{R0} \quad (14)$$

The aspect ratios and values for the bias circuit are shown in Table-6.

Table-6. Aspect ratios and values of bias circuit.

Component	Value (in µm or kΩ)
M0, M1, M4, M5	20/5.5
M2, M6, M7	20/3.5
M3	80/3.5
R0	6.3

3.4 Start-up

The start-up circuit is shown in Figure-9. In the stable state, the start-up circuit should not affect the Beta-multiplier's reference circuit operation. Based on Figure-8, if the gates of M7 or M3 are at ground and when the gates M4 or M0 are at VDDA, the undesired state occurs.

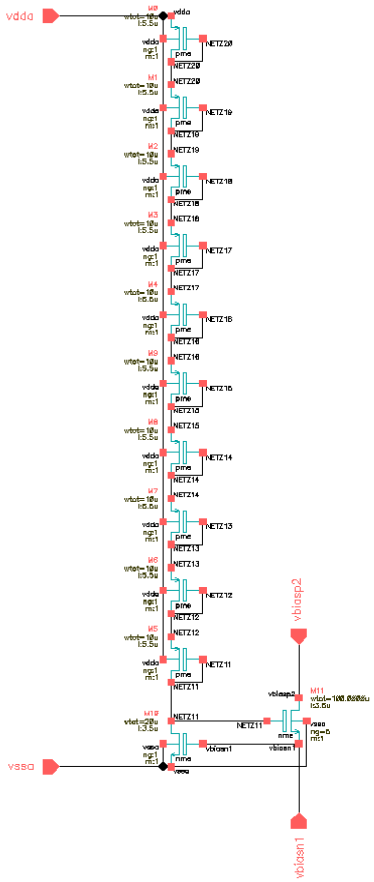


Figure-9. VREF_start-up circuit.

The M0 to M9 MOSFETs are connected in series with the same widths. The changes in the threshold voltage should not affect the biasing circuit because each device is identical.

In the start-up circuit, when the bias circuit is in zero current state, the gate of M10 is at the ground, so it is off. M11 behaves like an NMOS switch, turns ON, and leaks current into the gates of the self-biased circuit (VREF_bias). This causes the current to snap to the desired state and M11 to turn off. The *vbiasp2* and *vbiasn1* are used to set the current drawn by the circuit. The

current through M11 should be zero or very small in normal operation.

The aspect ratios of the start-up circuit are given in Table-7.

Table-7. Aspect ratios and values of the start-up circuit.

Component	Value (in µm)
M0, M1, M2, M3, M4,	10/5.5
M5, M6, M7, M8, M9	20/3.5
M10	100/3.5
M11	10/5.5

3.5 Amplifier

Figure-10 shows a schematic of a basic two-stage operational amplifier. The primary function of the operational amplifier (opamp) is to drive the VREF_bandgap circuit. Theoretically, the opamp forces the voltage at the input of VREF_bandgap to be equal.

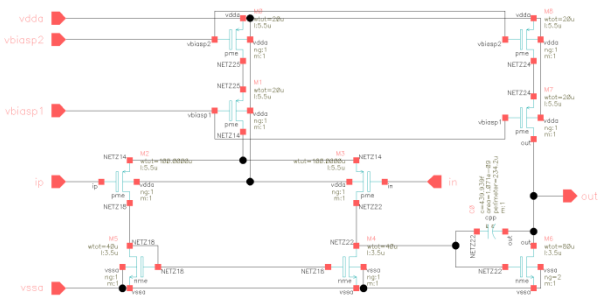


Figure-10. VREF_amp.

There are four inputs for this circuit: *vbiasp2*, *vbiasp1*, *in*, and *ip*. The output of this circuit will then connect into the input of the *vbiasp1* of the VREF_bandgap circuit. The *vbiasp2*, *vbiasp1* are derived from VREF_bias.

M0, M1, and M7, M8 are cascode current source circuits. Cascode current sources have high output impedance and moderate overdrive voltage. The value of *vbiasp2* is chosen so that M0 and M8 provide the required value of the current. While the value of *vbiasp1* is chosen to keep all the cascode current source transistors in saturation at all times.

The first stage consists of a differential pair between M2 and M3 with active load with n-channel current mirror load of M4 and M5 and cascode current source M0 and M1. The second stage consists of M6, a common source amplifier actively loaded with the cascode current source transistor M7 and M8. The capacitor *C*0 is included in the negative feedback path on the second stage. The current relationship of each transistor is

$$I_{D2} = I_{D3} = I_{D4} = I_{D5} = \frac{I_{D1}}{2} \quad (15)$$

And

$$I_{D6} = I_{D7} \quad (16)$$

When designing two-stage operational amplifiers, transistors' sizes have to be carefully set to avoid inherent or systematic input offset voltage. When input differential voltage is 0, V_{GS6} should be required to make I_{D6} equal to I_{D7}.

$$V_{GS6} = V_{DS5} = V_{GS4} \quad (17)$$

With perfect matching and zero input voltages,

$$\frac{(W/L)_4}{(W/L)_6} = \frac{(W/L)_5}{(W/L)_6} = \frac{1}{2}\frac{(W/L)_1}{(W/L)_7} \quad (18)$$

Since the second stage's input resistance is essentially high, the voltage gain of the amplifier can be found by considering two stages separately. The first stage is,

$$A_{v1} = - g_{m2}(r_{ds3} \| r_{ds4}) \quad (19)$$

$$g_{m2} = \sqrt{2KP_p\left(\frac{W}{L}\right)_2 I_{D2}} \quad (20)$$

Similarly, the second-stage voltage gain is

$$A_{v2} = -g_{m6}(r_{ds6} \| r_{ds7}) \quad (21)$$

$$g_{m6} = \sqrt{2KP_n\left(\frac{W}{L}\right)_6 I_{D6}} \quad (22)$$

As a result, the overall gain of the amplifier is

$$A_v = A_{v1}A_{v2} = -g_{m2}(r_{ds3} \| r_{ds4})g_{m6}(r_{ds6} \| r_{ds7}) \quad (23)$$

From this equation it shows that overall voltage gain is related to the quantity $(g_m r_{ds})^2$.

$$g_m r_{ds} = \frac{2V_A}{V_{ov}} = \frac{2/\lambda}{V_{GS}-V_t} \quad (24)$$

Where λ is the channel length modulation parameter that is reciprocal of the early voltage, V_A. Typical values of λ are in the range 0.05 V^{-1} to 0.005 V^{-1}.

The voltage gain decreases at high frequencies the capacitances associated with devices in the opamp. C_0 controls the fall-off, called compensation capacitance, to ensure that the circuit does not oscillate when connected in a feedback loop. For general-purpose amplifiers, the unity-gain bandwidth ω_{ta} is the bandwidth at which the magnitude of the open-loop voltage gain is equal to unity.

A simple equation can be used to find C_0 from the approximate unity-gain bandwidth is

$$C_0 = \frac{g_{m2}}{\omega_{ta}} = \frac{g_{m2}}{2\pi f} \quad (25)$$

Another important aspect of opamp design is to produce a current which is insensitive to variation of

supply voltage; V_{DDA}. This is accomplished by driving the amplifier with its output current. This is done by mirroring M1 and M7. This makes the output current of the operational amplifier almost constant to the voltage. The aspect ratios and values of the amplifier circuit are shown in Table-8.

Table-8. Aspect ratios and values of the amplifier circuit.

Component	Value (in µm or *fF*)
M0, M1, M8, M7	20/5.5
M2, M3	100/5.5
M4, M5	40/3.5
M6	80/3.5
C0	439.939

3.6 Bandgap

The implementation of bandgap reference circuit is shown in Figure-11. Input *in* and input *ip* are inputs to the operational amplifier VREF_amp. *vbiasp 1* is connected to the operational amplifier's output, and the output voltage for this bandgap reference is an input to the voltage regulator.

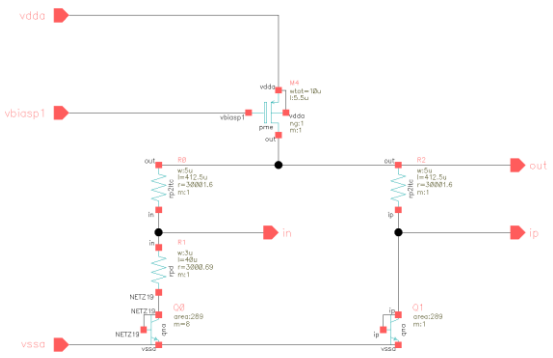


Figure-11. VREF_bandgap.

The operational amplifier, VREF_amp, as in section 3.2.4, is assumed to be ideal and a stable operating point exists for this circuit. *vbiasp1* is not derived from VREF_bias. Instead, it is connected to the output of the VREF_amp. Three resistors have been used in this circuit, which are *R*0, *R*1, and *R*2. All of these resistors are n-well resistances. Then, the op-amp's differential input voltage must be zero, and voltage drops across *R*0 and *R*2 are equals. Thus, the ratio *R*0 to *R*2 determines the ratio of *I*2 to *I*0. The collector currents of two diode-connected transistors, *Q*0 and *Q*1, refer to the ratio of *I*2 to *I*0 currents. From the circuit, the voltage across the *R*2 is,

$$V_{R2} = I_2 \times R_2 \tag{26}$$

where,

$$I_2 = \frac{V_{BE1} - V_{BE0}}{R_1} \tag{27}$$

From Equation 26 and Equation 27, the equation of V_{R2} is

$$V_{R2} = \frac{V_{BE1} - V_{BE0}}{R_1} \times R_2 \tag{28}$$

Then it becomes,

$$V_{R2} = V_T \ln(n) \times \frac{R_2}{R_1} \tag{29}$$

where n is the number of parallel BJT's. V_T is a constant called the thermal voltage, whose expression is given as

$$V_T = \frac{kT}{q} \tag{30}$$

where k is Boltzmann's constant (1.380658×10^{-23} J/K) and q is the magnitude of the electronic charge (1.6022×10^{-19} C). So, V_T is directly proportional to absolute temperature (T). V_{R2} is a positive TC voltage. Finally, the output of this circuit is

$$V_{\text{out}} = V_{R2} + V_{BE1} \tag{31}$$

Thus, the output voltage is a summation of a positive TC and a negative TC voltage. By choosing the proper value of resistors, the output reference voltage is made constant to temperatures (zero TC). The aspect ratios and values are given in Table-9.

Table-9. Aspect ratios and values of Bandgap core Circuit.

Component	Value (in µm or *kΩ*)
M0	10/5.5
R0, R2	30
R1	3
Q1	17×17
Q0	8(17×17)

3.7 Voltage Regulator

Figure-12 shows the schematic of the n-channel MOSFET voltage regulator. The regulator is similar as in [17].

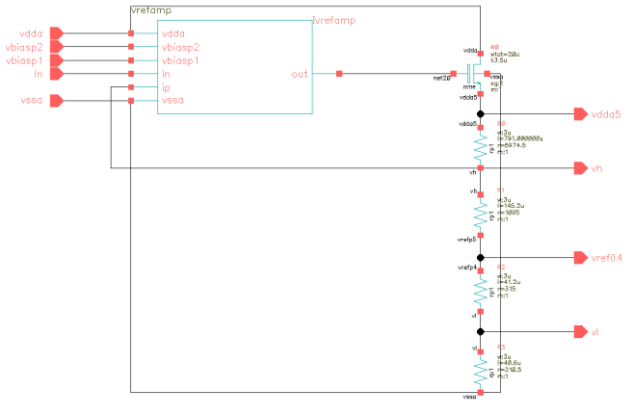


Figure-12. Voltage regulator.

The schematic consists of n-channel FET, M0, and an operational amplifier similar to VREF_ amp. One input of the amplifier monitors the fraction of the output determined by the resistor ratio of *R*0 and series resistor *R*1, *R*2, *R*3. The second input to the amplifier is from a stable voltage reference of VREF_bandgap output. If the output voltage rises too high relative to the reference voltage, the drive to the M0 changes to maintain a constant output voltage. The resistors form a voltage divider to provide the voltage references.

$$\text{VDD} = \left(1 + \frac{R0}{R1+R2+R3}\right)\text{VREF} \qquad (32)$$

The outputs of the voltage regulator are VDD, VH, VREF_EA, and VL. VDD is a 5 V supply voltage for other circuits, including an oscillator, feedback, and gate driver. Table-10 shows the aspect ratios and values of the voltage regulator.

Table-10. Aspect ratios and values of voltage regulator.

Component	Value
M0	20/3.5
R0	3/791 (5.975 kΩ)
R1	3/145.2 (1.095 kΩ)
R2	3/41.2 (315 Ω)
R3	3/40.6 (310.5 Ω))

4. RESULTS

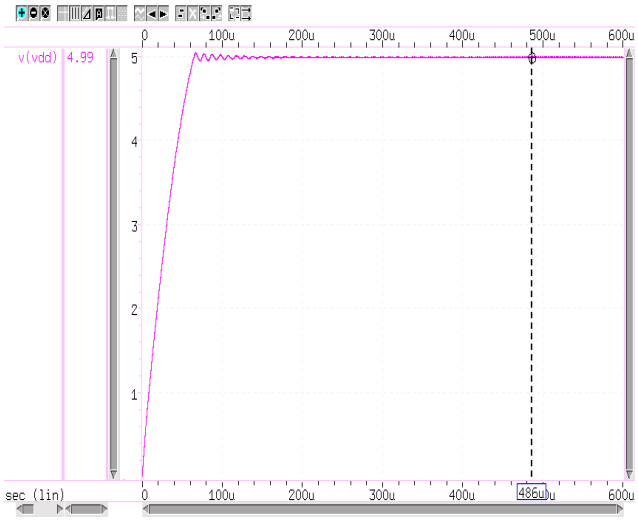
4.1 Introduction

Simulation results of the reference circuit using XDM10 technology are presented in this section. Pre layout simulation results are the results of basic transistor implementation, while post-layout results are the simulation results with the extracted parasitic capacitances and resistances of the layout.

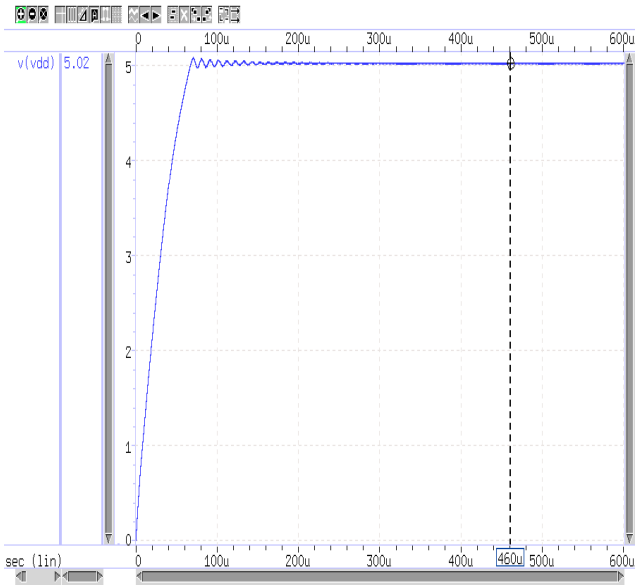
4.2 Regulated Output Voltages

The proposed design takes unregulated 310 V DC input and provides the regulated output voltages to the LED driver IC's internal circuitry. The desired regulated voltages are VDD, VH, VREF_EA, and VL, as depicted in Table-4. The results are compared between pre-layout and post layout. The parasitic capacitances, extracted according to the design layout, are affecting the actual performance of the design.

Figure-13a shows the pre-layout simulation result of VDD, and Figure-13b shows the post layout result. It can be seen, both results are closest to the desired value of 5V regulated voltage. The value is higher for the post layout result affected by parasitic components but acceptable since it increases by 0.4%.



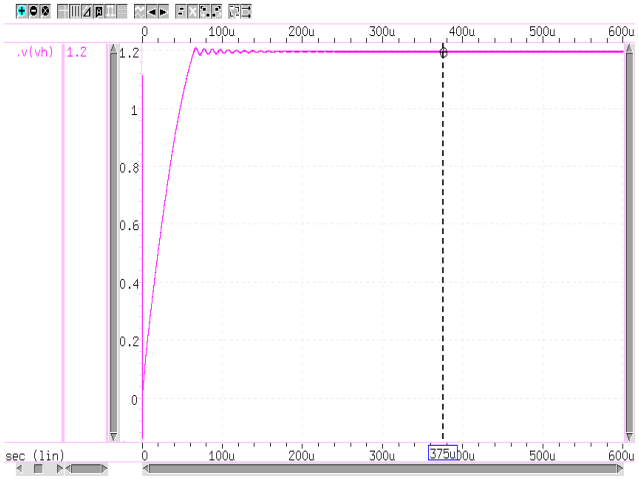
(a)



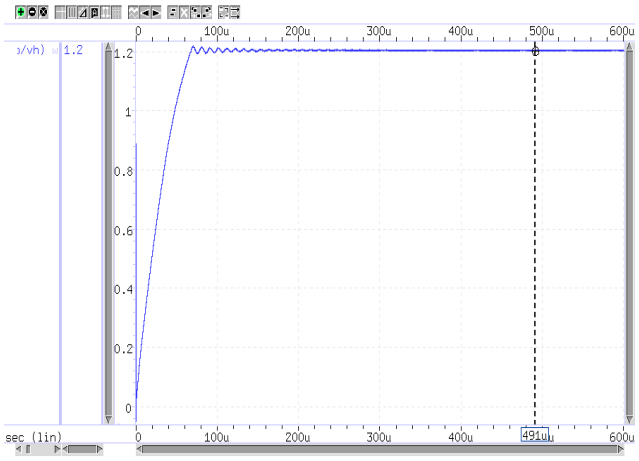
b.

Figure-13. a. Pre layout simulation result of VDD, b. Post layout simulation result of VDD.

The reference voltages for the ramp limit are shown in Figures 14 and 15. The high limit voltage, VH for both simulations is perfectly meet 1.2 V desired output. This value is the output voltage of the VREF_bandgap circuit. VL in the post-simulation result is less 0.1 mV from the pre-layout result. However, these values are close to the targeted 0.2V value.

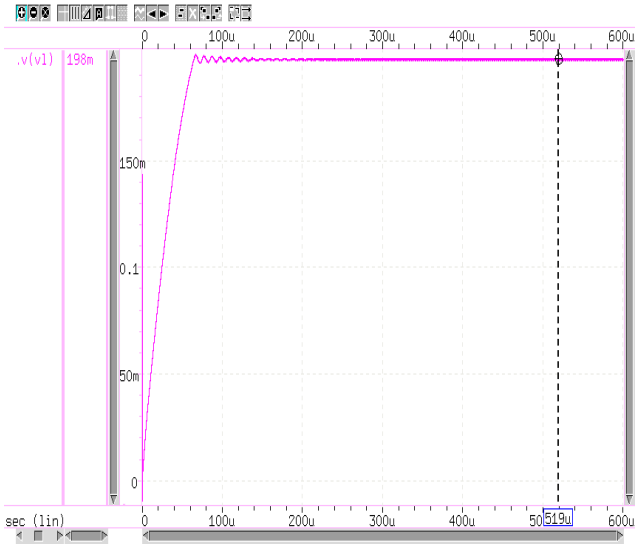


(a)

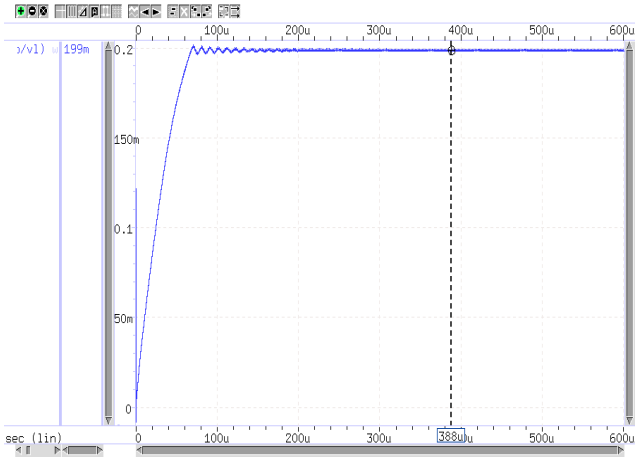


(b)

Figure-14. a. Pre layout simulation result of VH, b. Post layout simulation result of VH.



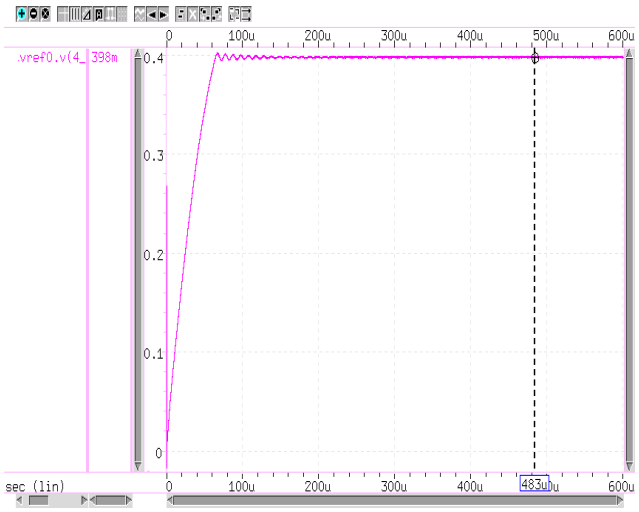
(a)



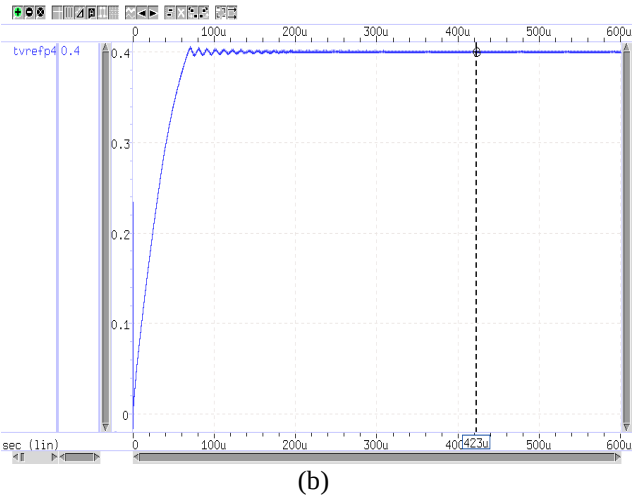
(b)

Figure-15. a. Pre layout simulation result of VL, b. Post layout simulation result of VL.

As in Figure-16, the fourth regulated voltage that controls the feedback circuit is VREF_EA. The pre-layout output is 0.398 V, while the post layout output is 0.4V. This value is important in the LED current optimization as discussed in section 2.2.1.1.



(a)



(b)

Figure-16. a. Pre layout simulation result of VREF_EA, b. Post layout simulation result of VREF_EA.

The voltage reference simulation results across process, voltage, and temperature are depicted in Table-11. The generated VDD is also shown in the table. Input voltage, V_{IN} is varied from 20 V to 310 V, temperature is varied from 0°C to 100°C**,** and 3 process corners which are Worst Power (WP), Typical Mean (TM) and Worst Slow (WS). The design performs very well across V_{IN} and temperature; there are very small changes in the voltage references and VDD. The maximum changes are only across corners. Nevertheless, this is expected and considered acceptable for the real application.

Table-11. Post layout simulation results of voltage regulator across process, voltage and temperature.

Corner: WP (Worst power)															
V_{IN}	**0°C**					**25°C**					**100°C**				
	VDD (V)	**VREF (V)**	**VH (V)**	**VREF_EA (V)**	**VL (V)**	**VDD (V)**	**VREF (V)**	**VH (V)**	**VREF_EA(V)**	**VL (V)**	**VDD (V)**	**VREF (V)**	**VH (V)**	**VREF_EA (V)**	**VL (V)**
20	5.396	1.292	1.291	0.429	0.213	5.384	1.289	1.288	0.428	0.212	5.277	1.264	1.262	0.419	0.208
100	5.401	1.294	1.292	0.429	0.213	5.391	1.291	1.290	0.428	0.213	5.294	1.268	1.266	0.420	0.209
200	5.401	1.294	1.292	0.429	0.213	5.392	1.291	1.290	0.428	0.213	5.294	1.268	1.266	0.402	0.209
310	5.402	1.294	1.293	0.429	0.213	5.392	1.291	1.290	0.429	0.213	5.294	1.268	1.266	0.420	0.209

Corner: TM (Typical Mean)															
V_{IN}	**0°C**					**25°C**					**100°C**				
	VDD (V)	**VREF (V)**	**VH (V)**	**VREF_EA (V)**	**VL (V)**	**VDD (V)**	**VREF (V)**	**VH (V)**	**VREF_EA(V)**	**VL (V)**	**VDD (V)**	**VREF (V)**	**VH (V)**	**VREF_EA (V)**	**VL (V)**
20	5.020	1.205	1.204	0.401	0.199	4.987	1.197	1.196	0.398	0.198	4.829	1.158	1.158	0.385	0.191
100	5.023	1.206	1.205	0.401	0.199	4.991	1.198	1.197	0.398	0.198	4.836	1.160	1.159	0.385	0.191
200	5.023	1.206	1.205	0.401	0.199	4.991	1.198	1.197	0.398	0.198	4.837	1.160	1.159	0.385	0.191
310	5.024	1.206	1.205	0.401	0.199	4.991	1.198	1.197	0.398	0.198	4.837	1.160	1.159	0.385	0.191

Corner: WS (Worst slow)															
V_{IN}	0°C					25°C					100°C				
	VDD (V)	VREF(V)	VH (V)	VREF_EA (V)	VL (V)	VDD (V)	VREF (V)	VH (V)	VREF_EA(V)	VL (V)	VDD (V)	VREF (V)	VH (V)	VREF_EA (V)	VL (V)
20	4.779	1.159	1.159	0.388	0.193	4.740	1.149	1.149	0.385	0.191	4.577	1.108	1.108	0.371	0.184
100	4.781	1.160	1.159	0.388	0.193	4.742	1.150	1.149	0.385	0.191	4.582	1.109	1.109	0.371	0.184
200	4.781	1.160	1.159	0.388	0.193	4.742	1.150	1.149	0.385	0.191	4.577	1.108	1.108	0.371	0.184
310	4.781	1.160	1.159	0.388	0.193	4.742	1.150	1.149	0.385	0.191	4.582	1.109	1.109	0.371	0.184

Figure-17 shows the voltage reference circuit's layout within the LED driver IC layout.

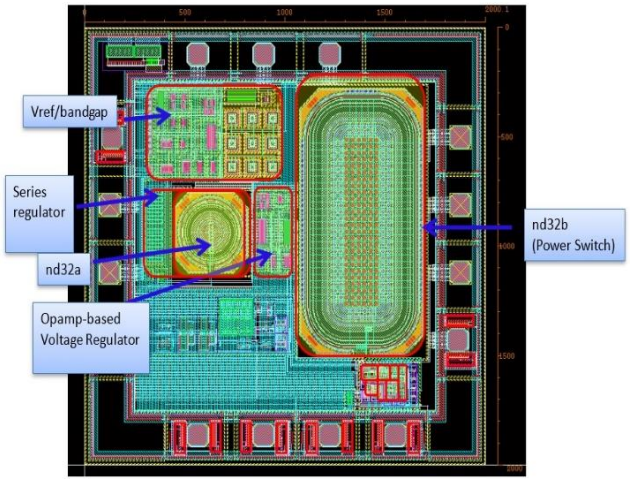


Figure-17. Layout of LED Driver with voltage reference circuits.

5. CONCLUSIONS

In summary, the development of the reference circuit was done with the help of behavioral models. Verilog-A was used in the development of models. It offers efficient ways for faster and better system verification for quick IC design implementation. The models are verified in top-level LED driver simulation. The modeled parameters such as VH, VREF_EA, and VL of the LED driver are used to design the voltage reference circuit. The design of the voltage reference circuit was implemented in X-Fab XDM10 1.0 µm 350 V process technology. The obtained results met the targeted specifications. The voltage reference provides precise voltages varied as much as ±10% across PVT, which indicates a robust and acceptable performance.

The proposed design is embedded with other circuits, such as a clock, PWM generator, to form a complete LED driver IC and will be tested together as an LED driver IC.

ACKNOWLEDGMENTS

The author would like to acknowledge Siti Rohaya Abdul Aziz as a master student involved in the development of the LED driver IC. This work is supported by Universiti Sains Malaysia, RUI1001/PELECT/8014008 and the Education Ministry of Malaysia, FRGS-203/PELECT/6071417.

CONFLICT OF INTEREST

The author declares no conflict of interest.

REFERENCES

[1] Azevedo I. L., Morgan M. G., Morgan F. 2009. The Transition to Solid State Lighting. Proceedings of the IEEE, 97(3): 481-510. https://doi.org/10.1109/JPROC.2009.2013058

[2] Jacobs J., Shen J., Hente D. 2008. A Simple Digital Current Controller for Solid-State Lighting. Power Electronics Specialists Conference, pp. 2417-2422. https://doi.org/10.1109/PESC.2008.4592303

[3] Baddela S. M., Zinger D. S. 2004. Parallel connected LEDs operated at high frequency to improve current sharing. Proc. Industry Electronics Society Annual Meeting. pp. 1677-1681. https://doi.org/10.1109/IAS.2004.1348696

[4] Calleja A. J., Ricosecades M., Cardesin J., Ribas J., Corominas E. L. 2004. Evaluation of a high efficiency boost stage to supply a permanent LED emergency lighting system. Industry Applications Conference, pp. 1390-1395. https://doi.org/10.1109/IAS.2004.1348594

[5] Zhou S., Rincon-Mora G. A. Apr 2006. A high efficiency, soft switching DC-DC converter with adaptive current-ripple control for portable. IEEE Trans. Circuits and Systems II. 53(4): 319-323. https://doi.org/10.1109/TCSII.2005.859572

[6] Bonizzoni E., Borghetti F., Malcovati P., Maloberti F., Niessen B. 2007. A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter. IEEE International Solid-State Circuits Conference,

pp. 526-619. https://doi.org/10.1109/ISSCC.2007.373526

[7] Nagaraja H. N., Kastha D., Patm A. 2005. Generalized analysis of integrated magnetic component based low voltage interleaved DC-DC buck converter for efficiency improvement. IEEE International Symposium on Circuits and Systems, 3, pp. 2485 -2489. https://doi.org/10.1109/ISCAS.2005.1465130

[8] Bao Y., Wu X., Xia X., Gao Y. 2015. High-efficiency negative charge-pump circuit for WLED backlights. Informacije MIDEM. 45(4): 277-283.http://ojs.midem-drustvo.si/index.php/InfMIDEM/article/view/176/112

[9] Isurin A., Cook A. 2006. Achieving a wide input voltage and output power load range step-down DC-DC conversion with good full range efficiency at 4 kW. IEEE APEC, pp. 67-71. Https://doi.org/10.1109/APEC.2006.1620517

[10] Wu C-H., Chen C-L. 2009. High-Efficiency Current-Regulated Charge Pump for a White LED Drive. IEEE Transactions on Circuits and Systems II. 56(10): 763-767. https://doi.org/10.1109/TCSII.2009.2027955

[11] Lee C. F., Mok P. K. T. 2002. On-chip current sensing technique for CMOS monolithic switch-mode power converter. IEEE Int. Symp. Circuits and Systems, 5, pp. 357-362.https://doi.org/10.1109/ISCAS.2002.1010691

[12] Fitz Patrick D., Miller I 1997. Analog Behavioral Modeling with the Verilog-A Language. Springer.https://doi.org/10.1007/b101821

[13] Marzuki A., Abdul Aziz S. R., Zulkifli T. Z. A. 2018. Solid State Lighting Driver IC Modeling Using Behavioral Simulation Technique. ICIAS 2018, pp. 1–6. https://doi.org/10.1109/ICIAS.2018.8540569

[14] Wang C. C., Chen C. L., Sung G. N., Wang C. L. 2011. A high efficiency DCDC buck converter for sub 2xVDD power supply. Microelectronics Journal, 1-9.https://doi.org/10.1016/j.mejo.2011.02.004

[15] XDM10 Datasheet. 2009. X-FAB Semiconductor Foundries AG. http://www.xfab.com.

[16] Baker R. J. 2010. CMOS Circuit Design, Layout, and Simulation. 3rd Edition. IEEE. https://doi.org/10.1002/9780470891179

[17] Marzuki A. 2020. CMOS Analog and Mixed-Signal Circuit Design. Boca Raton: CRC Press. https://doi.org/10.1201/9781003000648