VOL. 16, NO. 7, APRIL 2021 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

# DESIGN OF NOVEL LOW POWER (NLP) SRAM CELL FOR WIRELESS SENSOR NETWORK APPLICATIONS

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**ABSTRACT**

In the last decade, the development of embedded on-chip SRAM memories has been radically increasing. The demand of on-chip processing and computations of data in Wireless Sensor Networks (WSN) and Internet-of-Things (IoT) applications have been consistently increasing. This increased requirement influences the embedded on-chip Static Random Access (SRAM) memory to be vital and constantly improve the performance, stability and energy efficiency. The low power, high-performance and energy efficient SRAM has become a very important component in modern systems. In this research work, a Novel Low Power (NLP) FinFET based SRAM cell with 10T is proposed. The proposed cell is designed using 14 nm FinFET technology to reduce the power, read/write delay and improve the stability. The NLP cell has minimised 40% write power and 50% read power. In addition, 50% average delay has improved for write operations and 40% delay for read operations. The NLP cell is proved to be stable in worse conditions with temperature ranging from -50ºC to 140ºC and works for various $V_{DD}$ starting from 0.8V to 0.25V. Overall, the speed and stability have also improved in read operations due to three transistors. The read stability is improved 2.93x than the conventional cell because of the separate read circuit. The proposed NLP SRAM cell has also improved the read/write stability against the PVT (process, voltage, temperature) variations. It is also observed that the cell has 33.33% area overhead compared to 6T SRAM Cell.

**Keywords:** SRAM cell, FinFET, power, delay, performance, stability, WSN, IoT.

## 1. INTRODUCTION

There is a tremendous growth in Wireless Sensor Network and Internet of Things (IoT) applications with its multiple number of easily connected and battery-operated devices. The Wireless Sensor Network (WSN) performs a vital role in these applications. Basically, the WSN offers the communication and connectivity to gather data between the nodes and the base-station for further processing. The WSN environment and sensor node architecture is illustrated in Figure-1 (a) & (b).

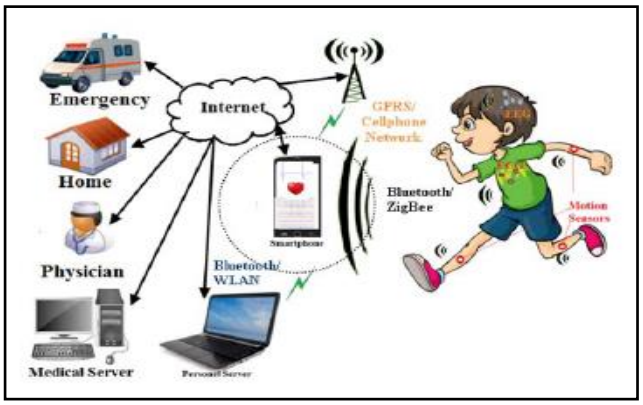



**Figure-1. (a)** Wireless Sensor Network.

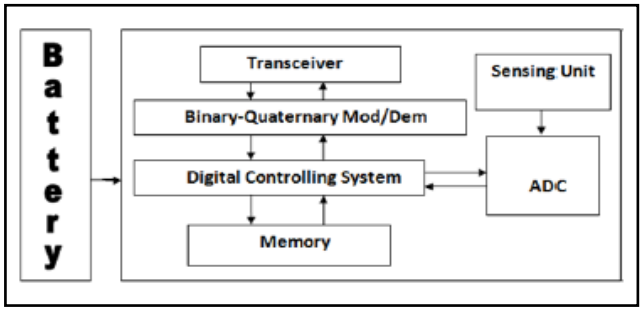



**Figure-1.** (b) Sensor node architecture.

From the WSN architecture, it can be clearly seen that the sensor node does all the processes pertaining to the data: capture, process, analyse and store. [1]. The paradigm of a group of wireless sensor nodes form the wireless sensor network of an application such as in healthcare, military, agriculture and manufacturing industries and the respective geographical area. All these applications demand persistently the battery devices' operating lifetime to be extended.

The faster, consistent, and increasing memory capacity are being constantly required to store and compute the data for the present IoT applications and modern portal gadgets. The use of mobile appliances, personal digital assistants, smart phones, and portable gadgets are becoming part of the daily life. In particular, the smart phones and mobile devices have predominantly become main part of everybody's life. The mobile gadgets are produced with continuous developments to cover many applications and taking different dimensions of features and specification. This rapid improvements in mobile devices extremely demand product success and sustainability [1]. Large

amount of data is being processed by such devices especially on media data for live streaming. There is continuous increase and high demand for fixed memory in terms of its usage for processing multimedia applications. The power consumption and limited operating lifetime of battery can be affected in these applications.

Summarising all the above, the demand for an extended battery lifetime is essential and has been increasing. Further, this can avoid the human efforts to frequently replace the batteries and at times it is too challenging to power-up these IoT devices due to their remote deployment and smallest size factor etc. Therefore, the low power consumption and higher performance have become main constraints for the up-to-date IoT based system-on-chip (SoC) in digital VLSI system designs. To meet this ever-increasing requirement of on-chip computational processing in IoT applications, the SRAM is always ideal due to its unique characteristics: high performance, rapid response, and low power consumption. It is confirmed from the literature that power consumption of SRAM is always high compared to the overall power of the system. About 40% to 50% of dynamic energy is being constantly consumed by SRAMs memory in high performance SoCs. The on-chip SRAM cache normally consumes a major portion of overall total power per operation.

SRAM is critical and one of the repetitive architectures in VLSI systems. There are so many budding cells developed by researchers with characteristics such as high speed, increased stability, low power, and overall performance. These characteristics of SRAM cells are becoming mandatory requirement to meet the continuous industry requirements on various modern VLSI development [2, 3]. The VLSI performance is generally improved by SRAM cells as they play a vital role [4-7]. The power and supply voltage are though equivalently decreased, the performance in terms of speed and stability are degrading. The many earlier proposed cells' Static Noise Margin (SNM) and overall performance [8-11] are to be improved.

The stability of SRAM is arisen to be a crucial design parameter under sub-micron feature technology. The CMOS technology has reached its limits in device shrinking, the FinFET technology becomes the substitute for Si-bulk SRAM. Due to its leakage reduction and significant performance improvement, FinFET became the mainstream IC technology than the flat-panel CMOS technology [12].

Generally, there were various write and read assist methods have been proposed and designed to overcome the power and stability issues. Some of the common ones are power gating with different supply voltage, single bit-line operation, Schmitt trigger design, staff effect and separate read circuit. The SRAM cell's read stability is normally improved by having a separate read circuit which isolates the storage nodes from the read path. There were many SRAM cells proposed earlier using CMOS and FinFET technologies and deployed with different techniques. Despite of having all these common improving factors, it is reported from the literature that the conventional SRAM cells are not highly suitable for Wireless Sensor Networks and Internet of Things (IoT) based low power applications [13].

Summarizing the above, we can conclude that the research is still in progress on SRAM cell development in terms of the leakage current, power, performance, write ability and read stability. Hence, in this work, a Novel Low Power (NLP) SRAM cell is proposed and designed in 14nm FinFET technology with the following striking features:

- To improve power performance and stability, the proposed cell is constructed with a circuit for write and separate one for read operations.
- The latch circuit is totally disconnected so then the data switches quickly on the nodes in the write operations. The power consumption is less due to the lesser discharging at the bit-lines.
- The PVT variations are applied on three different modes namely typical, minimum and maximum with varying temperature, supply voltage and threshold voltage to measure the write power.

This paper is organized as follows: Section 1 highlights the introduction. Section 2 introduces the design structure and explains the architecture and operation of the suggested Novel Low Power cell. Section 3 discusses the simulation results outcome and analysis, post-layout simulation results for various performance metrices of the NLP cell and further highlights the comparative results with the conventional cells. The last section highlights the area overhead and concludes the work.

## 2. ARCHITECTURE OF NOVEL LOW POWER (NLP) CELL

The proposed NLP cell's schematic architecture is shown in Figure-2. The proposed NLP cell is designed to decrease the power without any trade-off between the stability and access time. The NLP cell is designed with ten transistors (10T) through FinFET in 14nm submicron technology with an additional circuit for the read mode as shown in Figure-1. The novel cell comprises two inverters in the name of InvR and InvL. The FinFET based transistors M1 and M2 are connected to form the InvL and InvR has M3 and M4 transistors. The two tail transistors M7 & M8 play a vital role during the write operations. The M7 and M8 transistors are controlled by LW and RW signals.

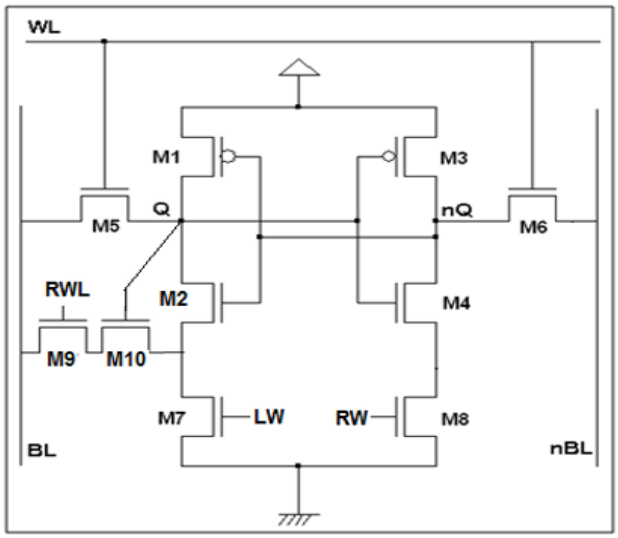



**Figure-2.** NLP SRAM Cell Schematic.

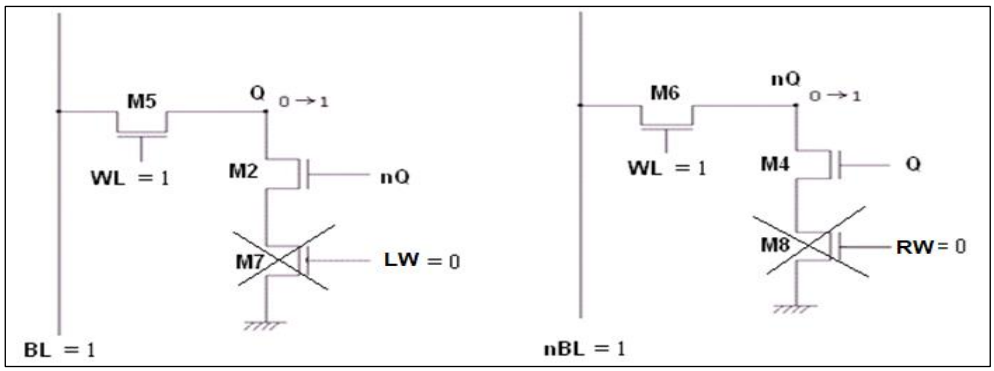
The bit-lines BL and nBL are connected with respective output nodes Q and nQ through M5 and M6 transistors. These two transistors (M5 and M6) behave as access transistors. The write mode operation is normally performed by the word-line WL and the signal LW and RW in this NLP cell. When the write mode operation is performed, the M5 and M6 transistors are ON and the LW and RW signals are alternatively ON so that the corresponding data can be transferred faster on nodes Q and nQ respectively.

The read circuit which consists of transistors M9, M10 and M7 through FinFET performs separately during the read operations.

This separate read circuit is designed to improve this novel cell's read stability. The read pass-transistor M9 through FinFET controls the read word-line (RWL). During the read mode and hold mode operations, the LW and RW signals are assigned to be high so then the latch property of cell can be stored. The output nodes are segregated from the bit-lines during read and hold mode operations through which the proposed cell's SNM is been significantly improved.

### 2.1 Write Operation

The data switching happens easily at the nodes due to the cell's dynamic nature with access transistors M5 and M6. The word-line WL is asserted to high and RWL to low after the data is assigned on bit-lines BL and nBL. The LW and RW signals play an important role instead of WL for all the write operations to enhance the write ability. The write circuit for write operations is shown in Figure-3.




(a) (b)

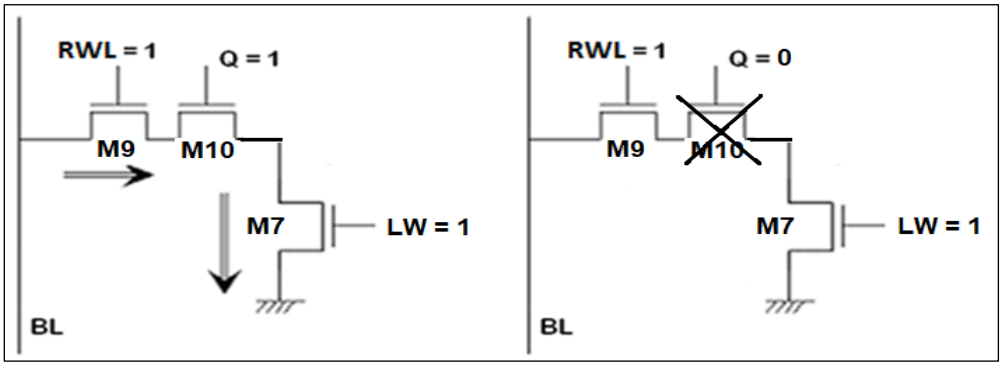
**Figure-3.** NLP SRAM Write Mode: (a) Write '1' (b) Write '0'.

During the write '1' operation, the bit-line BL is set to high and WL is asserted to high. Prior to asserting the WL, the LW is set to low and RW signal is high so that M7/M8 transistor is disconnected/connected from the ground and caused the data to be stored in Q. When nBL is assigned to '0', the transistor M7 turns off due to LW is also set to '0' which disconnects pull-down path of invL which flip node Q to high without any waiting for bit-line (nBL) to discharge completely. During the write '0' operation, the bit-line nBL is set to high and WL is asserted to high. Prior to asserting the WL, the LW is set to high and RW signal is low so that M7/M8 transistor is connected/disconnected from the ground and which causes the data to be stored in nQ. When BL is assigned to '0', the transistor M8 turns off due to RW is also set to '0' and disconnects pull-down path of invR which flip the node nQ to high without any waiting for the bit-line (BL) to discharge completely. The effect of disconnecting the pull-down path causes low power consumption and improved write access time. During the hold mode and read mode, the signals LW and RW are maintained to be high.

### 2.2 Read Operation

The read operation is performed by using the separate circuit consists of transistors M7, M9 and M10. During read operation, the RWL is set to high and WL is set to low. In the read '1' operation, the read word-line RWL is set to '1'. When the RWL is asserted, the M9, M10 and M7 transistors are ON so that the bit-line BL is discharged thru the three transistors. In read '0' mode, the stored data at Q = 0 makes M10 transistor turns off. This M10 transistor is disconnecting the read path and hence there is no discharging activity which causes less power and

better performance in the read operation. The read '1' and read '0' operations are presented in Figure-4.




(a) (b)

**Figure-4.** NLP SRAM Read Mode: (a) Read '1' (b) Read '0'.

## 3. SIMULATION RESULTS

The proposed NLP cell and other compared cells' architectures have been deployed in a standard 14nm submicron FinFET technology. The post layout simulations were also performed in similar technological environment. The power, delay, PVT variations and performance of NLP cell have been compared with 6T and Zero Aware (ZA) conventional cells. The conventional cells have the strategic similarities with NLP cell. The 6T and ZA cells have been redesigned together with NLP cell. The simulation was performed with a uniform device sizing in the similar environment for a fair comparison [14]. The simulation results of FinFET based NLP SRAM cell are analysed in terms of power (write/read), delay (write/read), variation of write power consumption and delay at various voltages are summarised here. Further, the variation of read power and delay with temperature ranging from -50°C till 140°C is also presented in this section.

### 3.1 Write Power and Write Delay

The discharging happens at two bit-lines in the conventional 6T SRAM cell due to which it consumes more power [15]. Alternatively, the power for write '0' operation in ZA SRAM cell is less due to one bit-line [4]. Whereas, in the proposed NLP cell, the tail transistor M7 or M8 disconnects the pull-down path during the write operations. This causes the write power and write delay to minimize as shown in the Table.1 and Figure.5.

**Table-1.** Write power.

| SRAM Cell | Write Power (µW) | |
|---|---|---|
| | Write '0' | Write '1' |
| 6T | 5.192 | 5.202 |
| ZA | 2.939 | 5.202 |
| NLP | 3.006 | 3.064 |

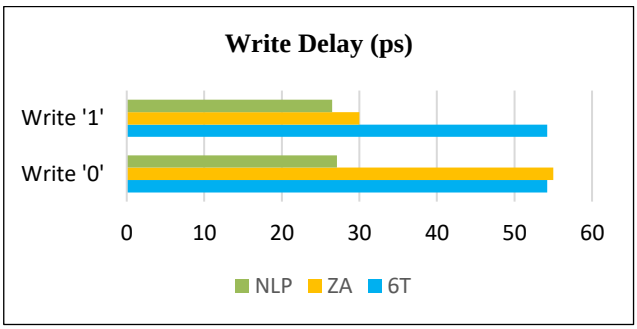



**Figure-5.** Write delay.

The average write power of the proposed NLP cell is 42% is less compared to conventional 6T SRAM cell. The average write delay has also improved about 50% for write '0' and 51% for write '1' operations compared to 6T SRAM Cell. There is an average of 25% power and 40% delay has been improved compared to ZA SRAM cell as well.

### 3.2 Analysis on Variation of Write Power Consumption and Delay

The proposed NLP cell and 6T SRAM cells are been simulated with variation of supply voltage $V_{DD}$ ranging from 0.8V till 0.25V. The average write power and write delay has been compared with the 6T SRAM cell. The proposed NLP cell confirms that it can work even at the 0.25V whereas the 6T cell can last only up to 0.33V. The write power consumption and the respective delay is presented in Figure-6 and Table-2 as shown below:

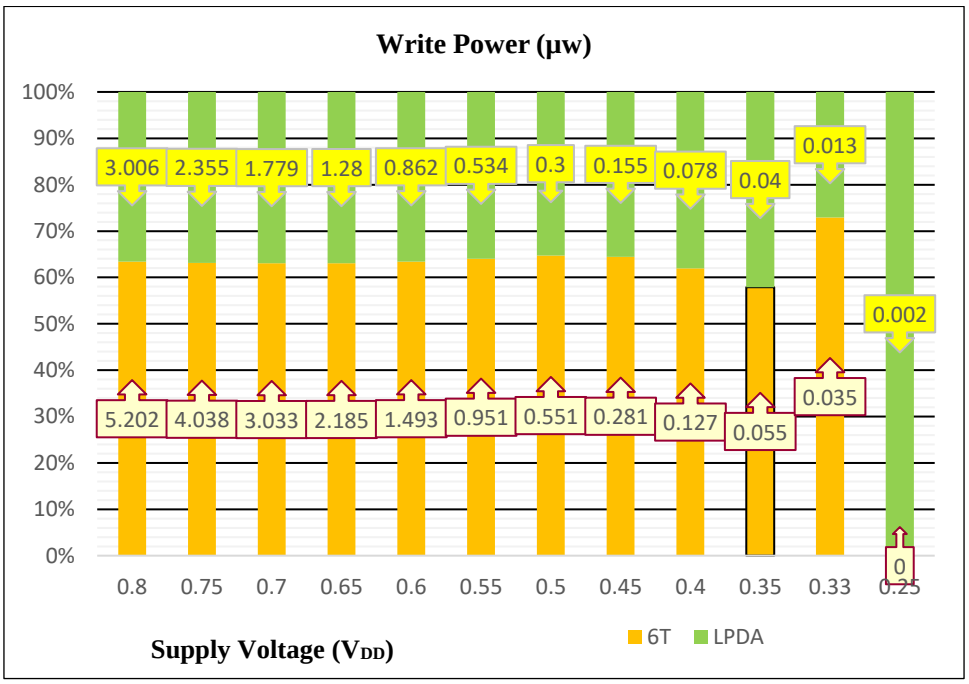



**Figure-6.** Variation of write power on various $V_{DD}$.

**Table-2.** Write delay on various $V_{DD}$.

| Supply Voltage ($V_{DD}$) | Write Delay (ps) | |
|---|---|---|
| | 6T | NLP |
| 0.8 | 54.2 | 26.5 |
| 0.75 | 63.7 | 36.7 |
| 0.7 | 74 | 47.5 |
| 0.65 | 85.2 | 58.8 |
| 0.6 | 97.6 | 70.5 |
| 0.55 | 111 | 82.4 |
| 0.5 | 126 | 94.8 |
| 0.45 | 143 | 109 |
| 0.4 | 163 | 126 |
| 0.35 | 193 | 150 |
| 0.33 | 216 | 163 |
| 0.25 | - | 240 |

### 3.3 Read Power and Read Delay

The average read power of the proposed NLP cell is 50% is minimised compared to conventional 6T and ZA SRAM cells. The average read delay of 40% has also been improved for both read '0' read '1' operations. The delay of the proposed NLP cell's read '0' operation is very less as there is no discharging happening. The read power and read delay are shown in the Table-3 and Figure-7 as below:

**Table-3.** Read delay.

| SRAM Cell | Read Delay (ps) | |
|---|---|---|
| | Read '0' | Read '1' |
| 6T | 84.6 | 85.4 |
| ZA | 85.3 | 85.6 |
| NLP | 15 | 86 |

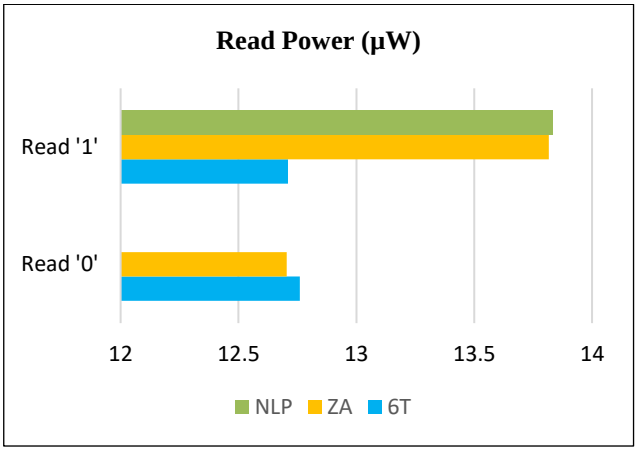



**Figure-7.** Read power.

### 3.4 Analysis on Variation of Read Power Consumption and Delay

The proposed NLP cell has been tested for the read power with temperature ranging from -50°C to 140°C against 6T and ZA SRAM cells. There is an average read power of 50% is reduced compared with the other two cells.

The proposed NLP cell has also been tested for its stability with temperature ranging from -50°C to 140°C

against 6T and ZA SRAM cells. An average of 40% has been improved when compared with the other two cells. The simulated results with various temperature on power and read delay are shown in Figure-8 and Table-4 as below. The simulated results prove that the NLP SRAM cell can be applied in any worse condition (T=140ºC) with minimum power loss.

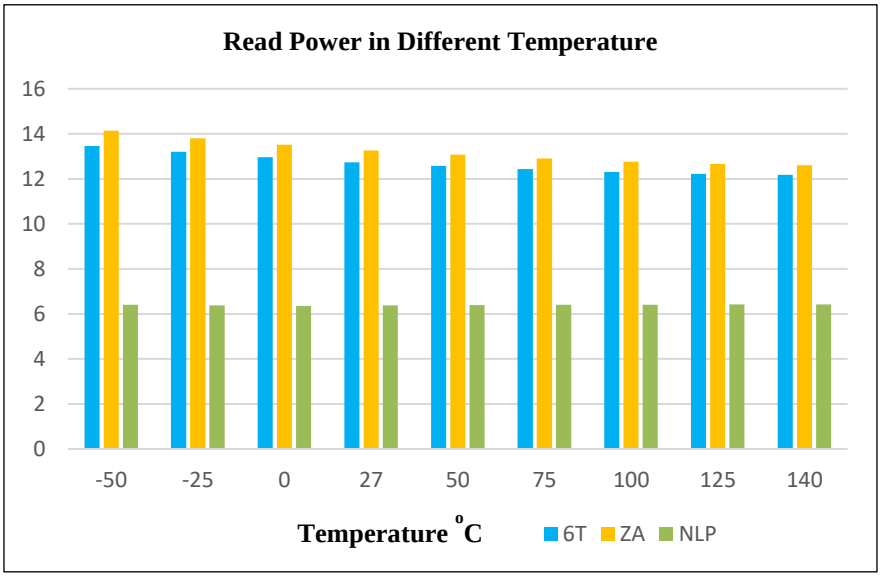



**Figure-8.** Variation of read power on various temperature.

**Table-4.** Read delay on various temperature.

| Temperature (ºC) | Read Delay (ps) | | |
|---|---|---|---|
| | 6T | ZA | NLP |
| -50 | 78.8 | 79.1 | 21.95 |
| -25 | 82.4 | 81.2 | 22.25 |
| 0 | 82.85 | 83.3 | 22.5 |
| 27 | 85 | 85.45 | 22.7 |
| 50 | 86.8 | 87.35 | 22.8 |
| 75 | 88.7 | 89.3 | 22.9 |
| 100 | 90.65 | 91.3 | 22.95 |
| 125 | 92.55 | 93.25 | 22.95 |
| 140 | 93.7 | 94.4 | 22.9 |

### 3.5 PVT Variations

The PVT (Process/Voltage/Temperature) variations are applied to test the write power of 6T SRAM cell and the proposed NLP cell. The PVT conditions have been applied and simulated with different inputs on supply voltage ($V_{DD}$), temperature (T) and threshold voltage ($V_{TH}$). There are three different modes of PVT operations performed to measure the power performance and write access time for both write '0' and write '1' operations. The PVT conditions are applied and simulate for both conventional 6T SRAM cell and the proposed NLP SRAM cell. The three modes of PVT variations are namely: typical, minimum and maximum modes. In the typical mode, 25ºC temperature, 0.8V supply voltage ($V_{DD}$) and 0.310V threshold voltage ($V_{TH}$) are applied. Whereas 50ºC temperature, 0.92V supply voltage ($V_{DD}$) and 0.270V threshold voltage ($V_{TH}$) are applied in the minimum mode and in contrast 50ºC temperature, supply voltage of 0.92V and threshold voltage of 0.270V are applied in the maximum mode.

The simulated results of write power on all the three PVT modes are shown in Figure-9 and Table-5. The power is measured in microwatts (µw). The resultant data shows that 41% power is minimised in typical mode, 43% is reduced in minimum mode and 40% power is saved in the maximum mode. In all three modes of PVT variations with variable data on supply voltage, threshold voltage and temperature, an average of 41% power consumption is reduced compared to 6T SRAM cell for both write '0' and write '1' operations. These data confirm that the proposed cell's write power is much lesser than 6T cell.

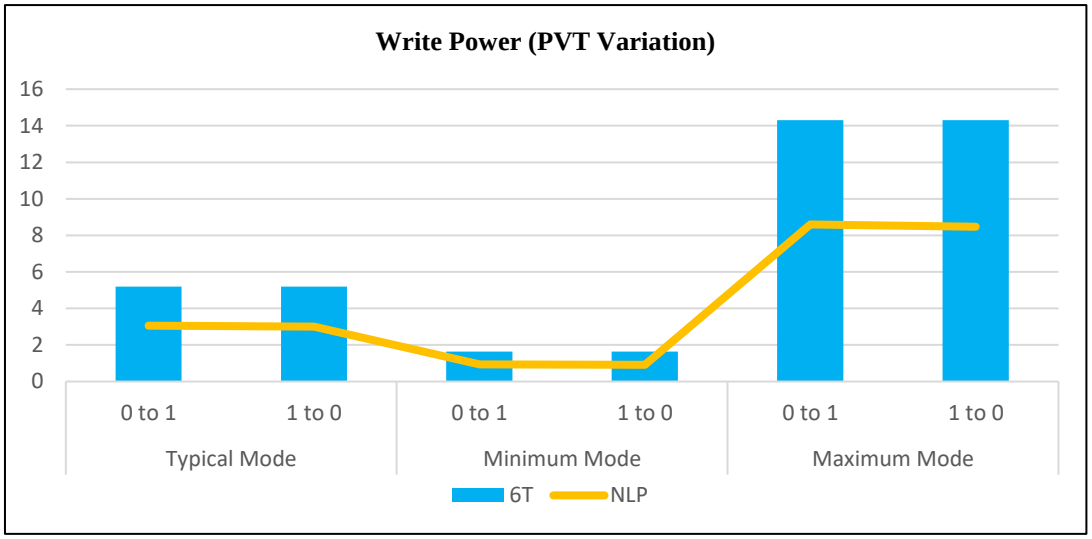



**Figure-9.** Write power of three PVT variation modes.

**Table-5.** Write power data of all 3 modes.

| Mode | Write Power (µw) | | | | | |
|---|---|---|---|---|---|---|
| | **Typical Mode (T=25°C, $V_{DD}$=0.8V & $V_{TH}$ = 0.310V)** | | **Minimum Mode (T=125°C, $V_{DD}$=0.68V & $V_{TH}$ = 0.365V)** | | **Maximum Mode (T= -50°C, $V_{DD}$=0.92V & $V_{TH}$ = 0.270V)** | |
| SRAM Cell | 0 → 1 | 1 → 0 | 0 → 1 | 1 → 0 | 0 → 1 | 1 → 0 |
| 6T | 5.202 | 5.192 | 1.637 | 1.632 | 14.306 | 14.298 |
| NLP | 3.064 | 3.006 | 0.942 | 0.915 | 8.597 | 8.476 |

The write delay is measured in picoseconds (ps). The simulated results of write delay on all the three PVT modes are shown as below in Table.6. Comparing the 6T and the proposed NLP cell, the results show that an average of 51% delay is improved in typical mode, 33% in minimum mode and there is no delay at the maximum mode. Overall, 42% power is minimized and 61% of delay has improved in the PVT conditions. The write delay data confirms that write ability of the proposed NLP cell has highly improved.

**Table-6.** Write delay of all 3 modes.

| Mode | Write Delay (ps) | | | | | |
|---|---|---|---|---|---|---|
| | **Typical Mode (T=25°C, $V_{DD}$=0.8V & $V_{TH}$ = 0.310V)** | | **Minimum Mode (T=125°C, $V_{DD}$=0.68V & $V_{TH}$ = 0.365V)** | | **Maximum Mode (T= -50°C, $V_{DD}$=0.92V & $V_{TH}$ = 0.270V)** | |
| SRAM Cell | 0 → 1 | 1 → 0 | 0 → 1 | 1 → 0 | 0 → 1 | 1 → 0 |
| 6T | 54.2 | 54.2 | 87.5 | 87.7 | 19.9 | 20.0 |
| NLP | 26.5 | 27.1 | 59.7 | 58.8 | - | - |

### 3.6 Stability/SNM and Cell Area

The stability of the SRAM cell is normally defined by the static noise margin (SNM) as the maximum value of DC noise voltages that can be tolerated by the cell without any change of output nodes [14]. The maximum possible square between normal and mirrored voltage transfer characteristics (VTC) usually derives the SNM [15]. In this proposed NLP cell, read SNM is 2.93x more than 6T SRAM cell due to a separate read circuit which is depicted in Figure-10.

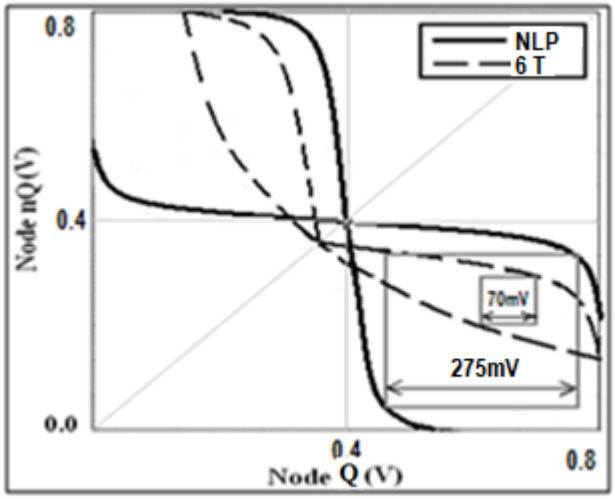



**Figure-10.** Static noise margin.

**Table-7.** Cell area.

| SRAM Cell | Number of Transistors | Area (μm$^2$) |
|---|---|---|
| 6T | 6 | 0.08 |
| NLP | 10 | 0.12 |

Table-7 above shows the number of transistors and occupying area of the chip for 6T and proposed NLP SRAM cells. It is also observed that 33% of area overhead than 6T cell.

## 4. CONCLUSIONS

Many low power techniques deployed earlier to minimize read power as write power is normally is greater than the read power. The proposed NLP SRAM cell reduces both read and write power. An average of 42% write power is saved during write '0' and 41% during write '1' operations. The write delay has also improved about 50% for write '0' and 51% for write '1' operations compared to 6T SRAM Cell. For read operations, an average of 50% read power and 40% read delay have been minimized. Overall, the speed and stability have also improved in read operations due to the separate read circuit with three transistors. Besides the power and delay, the NLP cell confirms that it can also work for various $V_{DD}$ ranging from 0.8V to 0.25V and proved to be stable even in worse conditions with temperature from -50ºC to 140ºC. The read stability (SNM) is also improved 2.93x compared to conventional cell due to separate read circuit. It is also observed that the NLP cell has 33.33% area overhead than 6T SRAM Cell. The proposed NLP cell is undoubtedly an attractive choice and it can be effectively used for WSN applications due to its low power consumption and higher stability.

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