VOL. 16, NO. 10, MAY 2021 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

VLSI IMPLEMENTATION OF COMPLEX MULTIPLIER USING VEDIC MATHEMATICS AND STUDY ITS PERFORMANCE

Ansha Noushad and A.R. Abdul Rajak
Department of Electrical and Electronics Engineering Birla Institute of Technology and Science Pilani, Dubai Campus, Dubai, United Arab Emirates
E-Mail: Noushad.ansha@gmail.com

ABSTRACT

In this paper, an attempt to implement an optimal complex multiplier using the "Urdhva Tiryakbhyam" Sutra of the ancient Indian Vedic Mathematics is presented. Signal Processing is based on mathematical analysis of complex numbers. Many DSP operations are based on complex operations like Fast Fourier Transform, z-transform, linear systems, multimedia applications, and telecommunications. The multiplier determines system performance as it is the slowest element and generally occupies a large area. Due to such conflicting constraints designing a complex multiplier has always been a challenge with significant tradeoffs. The proposed 16-bit Complex Multiplier using Vedic Multiplication is coded in VHDL, simulated and synthesized in Xilinx Vivado 2016 Software and compared to a standard Booth Complex multiplier.

Keywords: complex multiplication, Vedic multiplication, VHDL.

1. INTRODUCTION

The advancement in technology and switch from analog to digital has made Digital Signal Processing a unique need. The signals for digital processing are expressed as complex numbers; hence, operations on complex numbers are an essential part of DSP operations. Multipliers consume a large area and are usually the slowest elements in a circuit. They are also the power-consuming aspect of the device. Hence an optimal design of a multiplier is always a challenge. Complex Transformation is the heart of Digital Signal Processing. Signal Processing is based on mathematical analysis of complex numbers. Many DSP operations are based on complex operations like Fast Fourier Transform, z-transform, linear systems, multimedia applications, and telecommunications. Multiplication is the fundamental core of such complex operations. The multiplier determines system performance as it is the slowest element and generally occupies a large area. Due to such conflicting constraints designing a complex multiplier has always been a challenge with significant tradeoffs. Power consumption is also a critical factor as growing technology demands more computation capacity

Vedic Mathematics [11], [12] is a set of rules for enhancing the speed of time-consuming arithmetic operations like addition, subtraction, multiplication, squaring, cubing. Multiplication is carried out by three Sutras, namely Nikhilam Navatascaraman Dasatah, Ekadhikena Purvena, and Urdhva Tiryakbhyam. Urdhva Tiryakbhyam which means vertical and crosswise is a general formula which can be applied to all cases of multiplication.

2. VEDIC MULTIPLICATION

Consider a0a1 and b0b1 as two 2 bit numbers to be multiplied (Figure-1). First, the LSB of the two numbers is multiplied (s0). Then crosswise product a1b0 is added to the crosswise product a0b1, and the carry is carried over (s1). Then the MSB of the two numbers are multiplied, and any carryover is added to it (c2s2)

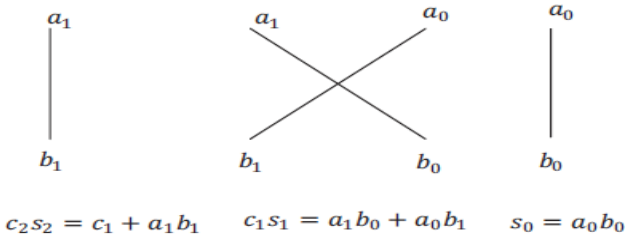

Figure-1. 2-bit Vedic multiplication.

It can be implemented using AND gates and two half adders, as shown in Figure-2. Using 2X2 multiplication block, we can build higher units like 4x4 and using 4x4 we can build 8x8 so on.

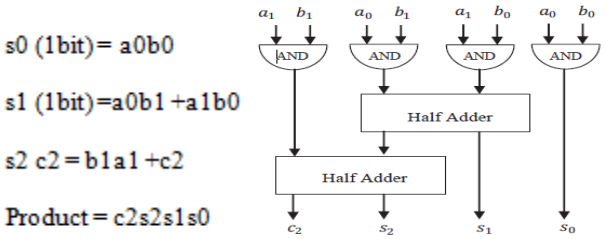

Figure-2. Gate level implementation of 2-bit Vedic multiplier.

3. IMPLEMENTATION OF COMPLEX MULTIPLIER USING VEDIC MULTIPLIER

Complex number multiplication requires four real multiplications and two additions/subtractions, which can limit the overall speed.

X + jY = (A + jB) (C + jD) = (AC – BD) + j (AD + BC)
Real part: (AC) - (BD)
Imaginary part: (AD) + (BC)

The real multiplication is achieved by using Vedic Multiplication techniques as well as Booth's

Multiplication algorithm for comparison purpose. Multiplication process involves generation of partial products, reduction of the formed partial products and final addition to generate result.

The addition and subtraction are performed using carry-save adder to reduce time, and also we can add more than two bits at a time.

3.1 The architecture of Complex Multiplier using Vedic Multiplier

We can build a complex multiplier unit (Figure-3) using four Vedic Multiplier Blocks. The results are added using an adder block and subtracted using a subtractor block to get the real and imaginary parts.

P = ab = (ar +jai). (br + jbi)
Pr = arbr - aibi
Pi = arbi + aibr

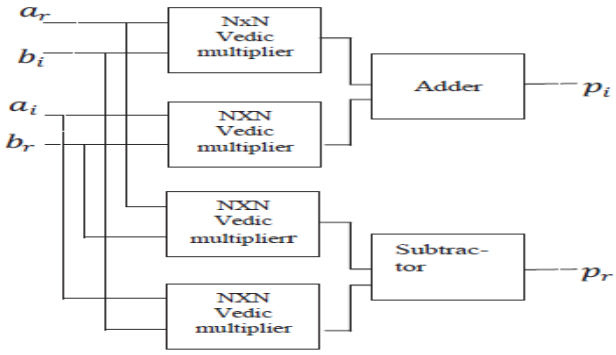

Figure-3. Architecture of complex multiplier using Vedic multiplier.

3.2 The architecture of Complex Multiplier using Booths Algorithm

The real multiplication is carried out using Booth's Algorithm (Figure-4) by encoding the multiplier bits. Here 3-bit recoding is used that is we add a zero to the LSB of the multiplier and separate the multiplier into bits of three. Once the bits are formed, the partial product generator generates partial products according to the 3 bits. The partial products are added using CSA adder.

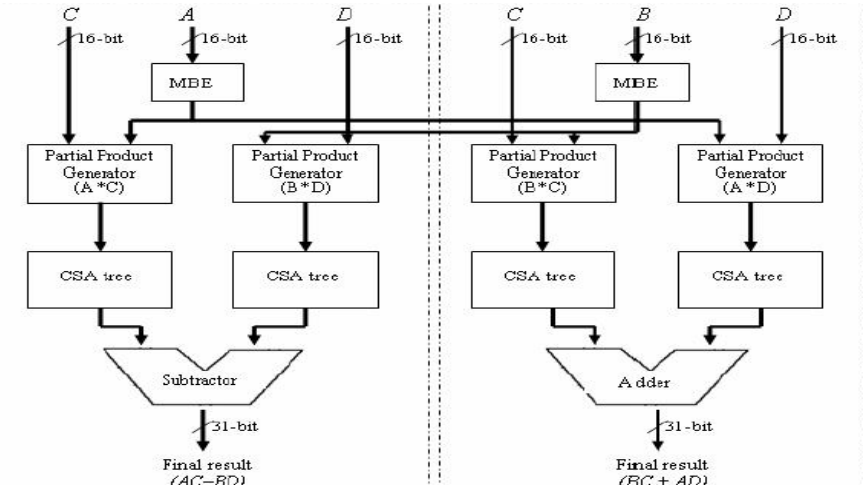

Figure-4. Architecture of booth multiplier.

4. SIMULATION AND RESULTS

The proposed 16-bit Complex Multiplier using Vedic Multiplication is coded in VHDL, simulated and synthesized in Xilinx Vivado 2016 Software. A 16-bit Complex Multiplier using Booth algorithm is also coded and synthesized for comparison purposes. The results are shown in the Table-1. Simulation waveforms for both Vedic (Figure-5) and Booth Complex multipliers (Figure-6) are also shown.

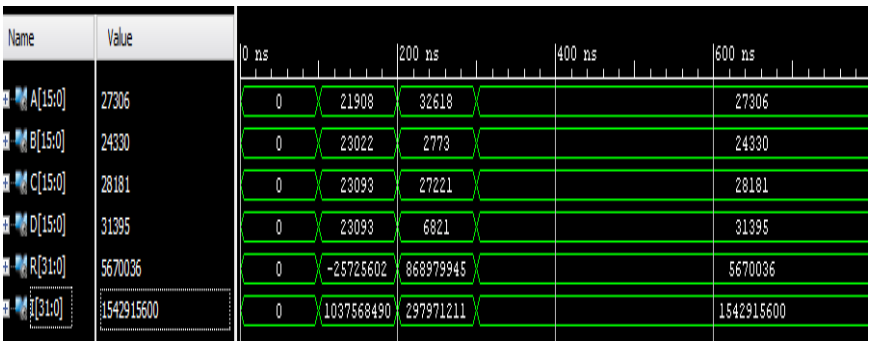

Figure-5. Simulation results of 16-bit Vedic based complex multiplier.

Table-1. Performance of 16 BIT VM and booth complex multiplier.

Parameters	Models	
	VM	Booth
Slice Units	2501	3683
Max Delay(ns)	29.347	30.685
Power(mW)	144.33	177

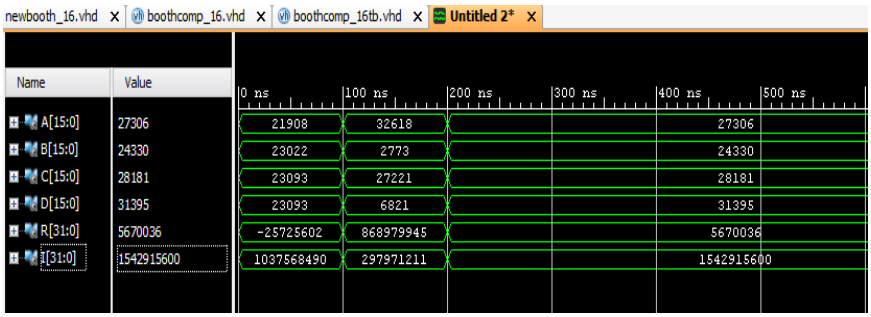

Figure-6. Simulation results of 16-bit Booth based Complex Multiplier.

5. CONCLUSIONS

Complex multiplication is an essential component for achieving high-performance DSP applications. However, it comes at the price of the increased area, power, and delay. So the challenge is to design an efficient complex multiplier that can achieve higher speed with less area requirement. In this thesis, a complex multiplier is designed using Urdhva Tiryakbhyam sutra from ancient Indian Vedic Mathematics to achieve a faster computation time with minimum area and power.

REFERENCES

[1] K. Deergha Rao, Ch. Gangadhar, Praveen K Korrai. 2016. FPGA Implementation of Complex Multiplier Using Minimum Delay Vedic Real Multiplier Architecture. 2016 IEEE Uttar Pradesh Section International Conference on Electrical, Computer and Electronics Engineering (UPCON) Indian Institute of Technology (Banaras Hindu University) Varanasi, India, Dec 9-11.

[2] Vojin G. Oklobdzija, David Villeger and Thieny Soulas. 1992. Considerations for Design of a Complex Multiplier. IEEE.

[3] Design and implementation of different multipliers using VHDL, Moumita Ghosh.

[4] Design of multiplier and its VLSI Implementation, Qi Liu, B.S., B.A., M.E., M.S

[5] L.P. Thakare Dr. A.Y. Deshmukhb. 2016. Area Efficient Complex Floating Point Multiplier for reconfigurable FFT/IFFT Processor Based on Vedic Algorithm. 7th International Conference on Communication, Computing and Virtualization.

[6] Premananda B.S., Samarth S. Pai, Shashank B, Shashank S. Bhat. 2014. Design of Area and Power Efficient Complex Number Multiplier. 5th ICCCNT - 2014July 11 - 13, Hefei, China, IEEE - 33044.

[7] Rizalafande Che Ismail and Razaidi Hussin. 2006. High Performance Complex Number Multiplier Using

Booth-Wallace Algorithm. ICSE2006 Proc. 2006, Kuala Lumpur, Malaysia.

[8] Laxman P. Thakare, A. Y. Deshmukh and Gopichand D. Khandale. 2014. VHDL Implementation of Complex Number Multiplier Using Vedic Mathematics. Proceedings of International Conference on Soft Computing Techniques and Engineering Application, Advances in Intelligent Systems and Computing 250, DOI: 10.1007/978-81-322-1695-7_46, Springer India.

[9] Manjunath K M1, Dr. K N Muralidhara2, Manasa K Chigateri3, Manjuvani K M4. 2016. An Exhaustive Research Survey on Vedic ALU Design. International Journal of Innovative Research in Computer and Communication Engineering. 4(7).

[10] Ku. Damini C. Dandade1, Prashant R. Indurka. 2017. Design of High Speed 16-Bit Vedic and Booth Multiplier. International Journal for Research in Applied Science & Engineering Technology (IJRASET). 5(VIII).

[11] Aaron D'costa1, Abdul Razak, Shazia Hasan. 2018. Analysis and comparison of fast multiplier circuits based on different parameters. International Journal of Engineering & Technology. 7(3): 1189-1192.

[12] Srinivasan S V, Dr. Abdul Razak. Physical Design of IC Chip for FFT using Vedic Mathematics. International Symposium on Fundamentals of Electrical Engineering (ISFEE 2014), University "Politehnica" of Bucharest, Romania IEEE Xplore.