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A REDUCED RATING OF ISOLATED-VSIS DSTATCOM FOR PQ ENHANCEMENT USING MRE-PWM TECHNIQUE

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ABSTRACT

Now-a-days, the voltage and current wave-shapes of distribution system is deviated due to power-electronic controlled non-linear load devices causing severe power-quality issues. Among the various custom-compensation devices, the DSTATCOM is most suitable for eradication of harmonic currents, reactive-power control, voltage balancing, power-factor correction, etc. The DSTATCOM utilizes the inverter for mitigation, but it is un-popular because of high rated switching devices, absence of current-sharing principle, high size and low efficiency, so on. A parallel-connected dual-inverter based DSTATCOM is also available; it reduces the rated capacity of DSTATCOM. But, un-popular due to complex control circuitry and dual DC capacitors, need of more switches which increases the switching losses, size, cost, complex design and low efficiency. In this paper, a novel reduced-switch isolated-VSIs DSTATCOM has been developed for PQ enhancement in distribution system using proposed MRE-PWM control scheme. The performance evaluation of proposed reduced-switch isolated-VSIs DSTATCOM is investigated in balanced, un-balanced and variable non-linear load conditions by using Matlab-Simulink computational tool, simulation results are presented.

Keywords: distributed static compensator, dual-inverters, reduced-switch inverter, isolated-vsis, mre-pwm control scheme, power-quality.

INTRODUCTION

The Electric-Power System (EPS) is an end-to-end interconnecting network includes various power-generation plants, power-transmitting systems for delivering power supply to customers via power distribution systems. In recent past, the voltage and current wave-shape of distribution system is deviated due to presence of power-electronic controlled non-linear loads causing severe Power-Quality (PQ) issues [1], [2]. These modern non-linear devices like rectifiers, switch-mode power converters, variable speed drives act as major sources for generation of harmonic current deviations. It deteriorates virtue in voltage and current wave-form quality at common feeding or coupling point (PCC) of three-phase distribution network.

The existed PQ issues are not new in distribution network, but the evolution of modern compensation device is big responsibility for power-system engineers. To mitigate these PQ issues in distribution point, a reliable mitigation strategy has been selected; it relies on nature and source of PQ issues. Over the various passive techniques [3], the Custom-Power Devices (CPD's) technology plays a prominent role in distribution system for compensating both voltage-current appraised issues [4], [5]. Among the various CPD techniques, Distributed-Static Compensator (DSTATCOM) plays a well-recommended role in distribution system for elimination of current harmonics, reactive-power regulation, voltage balancing, power-factor correction and all current appraised issues coming from non-linear loads [6].

The DSTATCOM includes shunt-connected 3-phase Voltage-Source Inverter (VSI), reference current extraction through suitable control scheme and gate-drive circuitry and current/voltage sensing devices. The VSI of DSTATCOM is functioned as in-phase mitigation principle for protecting the other loads integrated at PCC of distribution networks [7]. In this process, the VSI of DSTATCOM is de-rated due to injection of high current flow during harmonic compensation and reactive-power controlling which increases the usage of high-rated switching devices.

The ratings of DSTATCOM is minimized by many ways, a novel DSTATCOM topology is driven by non-stiff DC-link source, enables the low-rated DC-link capacitor without affecting compensation principle proposed by *S. B. Karanki et.al* in [8]. The averaged switching frequency of switches in VSI topology is decreased by reducing the voltage of DC capacitor; it minimizes the switching losses and rating of the VSI topology. The significant control algorithm is used to extract the suitable reference signal for injecting low value compensation current is explored by *C. Kumar and M. K. Mishra* in [9]. Thus, they minimize the losses in VSI and distribution network. It implies the injection of low value current harmonics and reactive power control without affecting the system specifications. A reduced-rating VSI-DSTATCOM is employed by zigzag transformer for enhancing PQ features in a 3-phase 4-wire distribution system; it reduces the need of additional split DC capacitors [10].

These methods are inefficient and alleviate by employing two low-rated VSIs and connected as parallel-form to attain current-sharing principle, reduced switch stress/losses and maximize the over-all efficiency, etc. A novel three-leg dual-VSI based DSTATCOM powered by common DC capacitor with associated control scheme is

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explored by *M.V.M. Kumar et.al* in [11]. It ensures the sharing of injected currents which regulates the THD value of source current and over-all rating of device. The dual-VSIs based shunt compensator is proposed by *Y. R. Babu and C. S. Rao* in [12], for minimizing harmonic currents in 3-phase distribution system and also reduces the rated capacity through distributed generation scheme. In this work, dual control schemes are used for controlling both PQ and DG operation in a distribution system is carried under various conditions.

The dual-VSIs based DSTATCOM have high fault tolerance and robust operation during internal faults of VSI, it improves flexible power flow, maintain continuous operation and reduces the over-all ratings of device. It establishes the sharing of injected currents between the VSIs without affecting the compensation principle using suitable control schemes [13]. The popular control schemes are Instantaneous Symmetrical Component (ISC) [14], Synchronous Reference Frame (SRF/id-iq) [15], Instantaneous Real-Power (IRP) [16] control schemes, etc. Among these, IRP-PQ is the recognized for extracting reference currents for active compensation, independent controlling of real-reactive power in a distribution system by sensing the proper measurements.

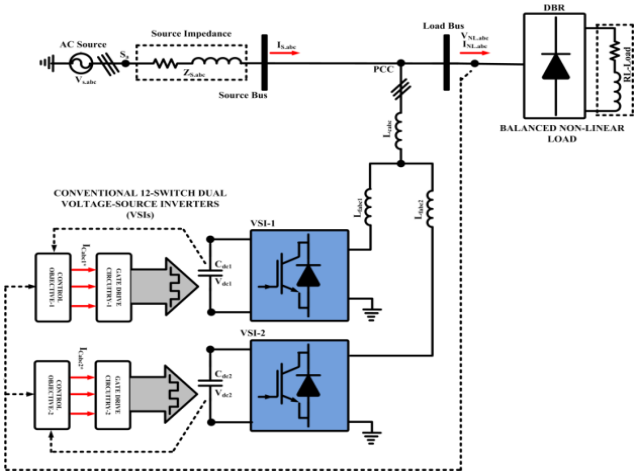

Figure-1. Schematic diagram of conventional dual-VSIs based DSTATCOM.

The schematic diagram of conventional dual-VSIs based DSTATCOM is shown in Figure-1. The conventional dual-VSIs DSTATCOM consists of two 3-phase VSIs powered by two DC-link capacitors, connected as parallel-form to distribution network for injecting the in-phase compensation currents. These dual-VSIs of DSTATCOM requires two or more VSI topologies for current sharing which increases cost, size, complex design due to need of more low-rated switches. In this paper, a novel reduced-switch isolated-VSIs DSTATCOM has been proposed for PQ enhancement in distribution system using IRP-PQ and MRE-PWM scheme. The performance evaluation of proposed isolated-VSIs DSTATCOM is verified in balanced, un-balanced and variable non-linear loads using Matlab-Simulink computational tool, simulation results are presented.

PROPOSED ISOLATED-VSIs BASED DSTATCOM

The proposed reduced-switch VSIs requires 9-switches for designing DSTATCOM for PQ compensation, load balancing in a three-phase distribution network. The proposed 9-switch isolated-VSI reduces the over-all rating of the DSTATCOM by employing new parallel-VSI structure with integration of additional inductors. The schematic diagram of proposed isolated-VSIs DSTATCOM is shown in Figure-2.

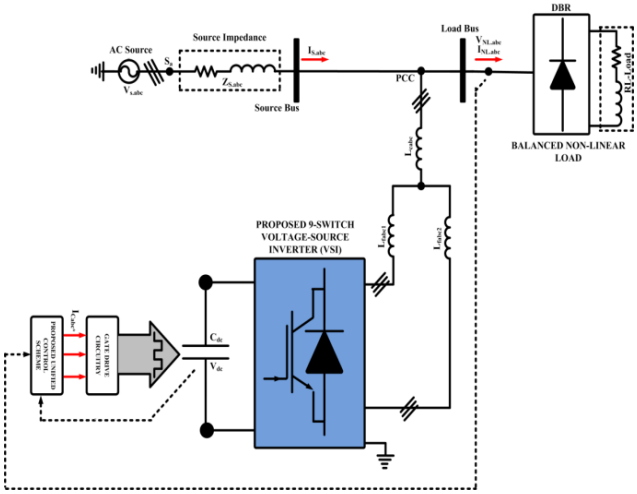

Figure-2. Schematic diagram of proposed isolated-VSIs DSTATCOM.

The proposed 9-switch isolated-VSIs are interfaced to three-phase distribution system powered by three-phase voltage source $V_{s.abc}$, source current $I_{s.abc}$ with a source impedance $Z_{s.abc}$ driving the Diode-Bridge rectifier as non-linear load with load voltage/current as $V_{NL.abc}$, $I_{NL.abc}$, respectively. It utilizes the single DC capacitor as C_{dc} to drive the isolated-VSIs which injects compensation currents as $I_{C.abc1}$ and $I_{C.abc2}$. The suitable line interfacing inductors $L_{f.abc1}$ and $L_{f.abc2}$ are connected at output of isolated-VSIs for eliminates the notching affects during compensation. The proposed 9-switch isolated-VSIs is a static device dedicated to provide compensation currents injected by isolated-VSIs, it replaces the usage of dual 6-switch (6x2) VSI structure. Therefore, the need of number of switching devices is low and thus reduces the switching stress/loss, size, cost, complex design and maximizing the over-all efficiency of DSTATCOM.

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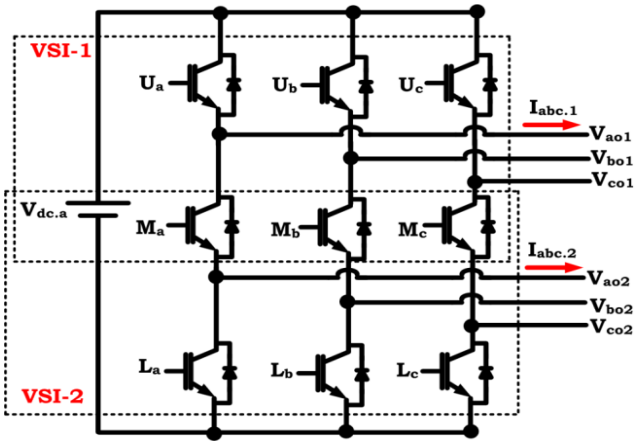

Figure-3. Schematic diagram of proposed 9-switch isolated-VSIs topology.

The proposed isolated-VSIs consists of 9 switches connected as bridge manner, it combines two-three-phase VSIs. The VSI-1 consists of six switches with combination of upper part switches are U_a, U_b, U_c and common middle part switches are M_a, M_b, M_c. The VSI-2 consists of six switches with the combination of lower part switches are L_a, L_b, L_c and common middle part switches are M_a, M_b, M_c, respectively. The schematic diagram of proposed 9-switch isolated-VSIs topology is depicted in Fig.3. It has two operating modes for getting dual outputs by switching the respective switches of isolated-VSI using suitable switching pattern produced by modulation technique. In mode-A, the switches of lower part (L_a, L_b, L_c) are conducted continuously for a period of half cycle. Also, the remaining switches of upper and middle part are considered as VSI-1 to generate required output voltage V_o at load terminals. In mode-B, the switches of upper part (U_a, U_b, U_c) are conducted continuously for a period of remaining half cycle. Also, the remaining switches of middle and lower part are considered as VSI-2 to generate required output voltage V_o at load terminals by using switching pattern is illustrated in Table-1. A Pulse-Width Modulation (PWM) technique is used to generate the switching states of proposed 9-switch isolated-VSIs topology with a reference signal extracting from unique control scheme and triangular carrier signals.

Table-1. Switching pattern of proposed 9-switch isolated VSIs topology.

	Switching States									Output Voltage (Vo)		
	U_a	U_b	U_c	M_a	M_b	M_c	L_a	L_b	L_c	V_{ab}	V_{bc}	V_{ca}
VSI-1	1	0	0	0	1	0	1	1	1	+Vo	-Vo	0
	1	0	0	0	0	1	1	1	1	+Vo	0	-Vo
	0	1	0	0	0	1	1	1	1	0	+Vo	-Vo
	0	1	0	1	0	0	1	1	1	-Vo	+Vo	0
	0	0	1	1	0	0	1	1	1	-Vo	0	+Vo
	0	0	1	0	1	0	1	1	1	0	-Vo	+Vo
VSI-2	1	1	1	1	0	0	0	1	0	+Vo	-Vo	0
	1	1	1	1	0	0	0	0	1	+Vo	0	-Vo
	1	1	1	0	1	0	0	0	1	0	+Vo	-Vo
	1	1	1	0	1	0	1	0	0	-Vo	+Vo	0
	1	1	1	0	0	1	1	0	0	-Vo	0	+Vo
	1	1	1	0	0	1	0	1	0	0	-Vo	+Vo

This work presents a new control scheme in distribution system with integration of battery to DSTATCOM for improving the power quality features. The battery system will get charge and discharge based on load requirement. The proposed control strategy again modified to control the battery current which is evaluated by simulation tool, simulation results are presented for various test cases. Figure-1 shows the conventional DSTATCOM connected in distribution system. The DSTATCOM consists of voltage source converter and capacitor. DSTATCOM supplies the reactive power and harmonics required by the load.

REFERENCE CURRENT EXTRACTION

The reference current extraction plays an important role in compensation, because it is influencing on accuracy and performance of DSTATCOM. These reference current estimation schemes are classified as frequency-domain and time-domain methods. Among, the time-domain representation is very simple technique due to less circuit analysis and low mathematical transformations, it requisites low computational time and precise control. In this work, the instantaneous real-reactive power (IRP-PQ) theory is represented in time-domain function for extraction of reference current signals to proposed DSTATCOM topology [17]. Mainly, it

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utilizes the Clarke's transformations for conversion of stationary *abc* coordinates into instantaneous $\alpha\beta$ rotating orthogonal reference frame. The non-linear load currents ($i_{Ln.abc}$) and source terminal voltage ($v_{ts.abc}$) is transformed to $\alpha\beta$ rotating frame such are stated in below Eqn. (1) and (2),

$$\begin{bmatrix} v_{ts.\alpha} \\ v_{ts.\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_{ts.a} \\ v_{ts.b} \\ v_{ts.c} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \mathrm{i}_{\mathrm{Ln}.\alpha} \\ \mathrm{i}_{\mathrm{Ln}.\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} \mathrm{i}_{\mathrm{Ln.a}} \\ \mathrm{i}_{\mathrm{Ln.b}} \\ \mathrm{i}_{\mathrm{Ln.c}} \end{bmatrix} \quad (2)$$

Where, $v_{ts.abc}$ and $i_{Ln.abc}$ are the three-phase source terminal voltage and non-linear load current in *abc* frame, $v_{ts.\alpha\beta}$ and $i_{Ln.\alpha\beta}$ are three-phase source terminal voltage and non-linear load current in $\alpha\beta$ frame, respectively. The immediate sum of both real (P) and reactive power (Q) are represented in $\alpha\beta$ frame is stated as,

$$\mathrm{S} = \mathrm{P} + \mathrm{jQ} = \mathrm{v}_{\mathrm{ts}.\alpha\beta} * \mathrm{i}_{\mathrm{Ln}.\alpha\beta} = \left(\mathrm{v}_{\mathrm{ts}.\alpha} - \mathrm{jv}_{\mathrm{ts}.\beta}\right).\left(\mathrm{i}_{\mathrm{Ln}.\alpha} - \mathrm{ji}_{\mathrm{Ln}.\beta}\right) \quad (3)$$

$$\mathrm{P} = \mathrm{v}_{\mathrm{ts}.\alpha}\mathrm{i}_{\mathrm{Ln}.\alpha} + \mathrm{v}_{\mathrm{ts}.\beta}\mathrm{i}_{\mathrm{Ln}.\beta} \quad (4)$$

$$\mathrm{Q} = -\mathrm{v}_{\mathrm{ts}.\beta}\mathrm{i}_{\mathrm{Ln}.\alpha} + \mathrm{v}_{\mathrm{ts}.\alpha}\mathrm{i}_{\mathrm{Ln}.\beta} \quad (5)$$

Thus, the instantaneous real-reactive power (P-Q) are formed as matric function can be described as below,

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_{ts.\alpha} & v_{ts.\beta} \\ -v_{ts.\beta} & v_{ts.\alpha} \end{bmatrix} \begin{bmatrix} i_{Ln.\alpha} \\ i_{Ln.\beta} \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{Ln.\alpha} \\ i_{Ln.\beta} \end{bmatrix} = \frac{1}{v_{ts.\alpha}^2 + v_{ts.\beta}^2} \begin{bmatrix} v_{ts.\alpha} & v_{ts.\beta} \\ -v_{ts.\beta} & v_{ts.\alpha} \end{bmatrix} \begin{bmatrix} P \\ Q \end{bmatrix} \quad (7)$$

The instantaneous real-reactive power (P-Q) components are decomposed into DC average and AC oscillatory parts are stated in below Eqn. (8),

$$\begin{aligned} P &= \bar{p} + \tilde{p} \\ Q &= \bar{q} + \tilde{q} \end{aligned} \quad (8)$$

The DC average component ($\bar{p}$) of instantaneous real-power (P) describes the fundamental current and voltage components to the real-power carried from source terminal to load, while the AC oscillatory part ($\tilde{p}$) is relatively power exchanging between source terminal and load. The DC averaged component ($\bar{p}$) of instantaneous real-power is the only power component should be furnished by three-phase AC terminal which is extracted through High-Pass Filter (HPF). The HPF regulates the low-range frequencies and allows the high-phase order which is considered as un-processed reference currents. Likewise, the instantaneous reactive power (Q) is described as $(\bar{q}), (\tilde{q})$, represents the fundamental and harmonic parts which are subjected for energy circulation in between the respective phases of non-linear load.

The reference current components are extracted from both oscillatory AC part ($\tilde{p}$) as real component and total reactive power (Q) with addition of VSI switching loss as ($\bar{p}_{loss}$). The switching losses of VSI are recomposed by regulating the DC voltage of isolated-VSIs by using Proportional-Integral (PI) controller. It administer the error quantities for minimizing the losses in VSI by comparing the measured ($V_{dc.m}$) and reference DC-link voltage ($V_{dc.r}^*$), the response of PI controller at ith period is stated in Eqn. (9),

$$\begin{aligned} \mathrm{V}_{\mathrm{dc.er}} &= \mathrm{V}_{\mathrm{dc.r}}^* - \mathrm{V}_{\mathrm{dc.m}} \\ \bar{\mathrm{p}}_{\mathrm{loss}} &= \mathrm{K}_{\mathrm{pdc}} * \left(\mathrm{V}_{\mathrm{dc.er(i)}} - \mathrm{V}_{\mathrm{dc.er(i-1)}}\right) + \mathrm{K}_{\mathrm{idc}} * \left(\mathrm{V}_{\mathrm{dc.er(i)}}\right) \end{aligned} \quad (9)$$

The definite real-power component is measured from the combination of AC oscillatory component($\tilde{p}$), DC average component ($\bar{p}$) and power-loss of VSI can be stated in Eqn. (10),

$$\tilde{\mathrm{p}} = \mathrm{P} - \bar{\mathrm{p}} + \bar{\mathrm{p}}_{\mathrm{loss}} \quad (10)$$

The outcome reference current is extracted from above equations is stated in Eqn. (11),

$$\begin{bmatrix} \mathrm{i}_{\mathrm{cr}.\alpha}^* \\ \mathrm{i}_{\mathrm{cr}.\beta}^* \end{bmatrix} = \frac{1}{\mathrm{v}_{\mathrm{ts}.\alpha}^2 + \mathrm{v}_{\mathrm{ts}.\beta}^2} \begin{bmatrix} \mathrm{v}_{\mathrm{ts}.\alpha} & -\mathrm{v}_{\mathrm{ts}.\beta} \\ \mathrm{v}_{\mathrm{ts}.\beta} & \mathrm{v}_{\mathrm{ts}.\alpha} \end{bmatrix} \begin{bmatrix} \mathrm{P} \\ \mathrm{q} \end{bmatrix} \quad (11)$$

Hence, the defined reference current component in $\alpha\beta$ orthogonal frame is re-converted into standard *abc* frame using inverse-Clarke's transformation process as shown in Eqn. (12),

$$\begin{bmatrix} i_{cr.a}^* \\ i_{cr.b}^* \\ i_{cr.c}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{cr.\alpha}^* \\ i_{cr.\beta}^* \end{bmatrix} \quad (12)$$

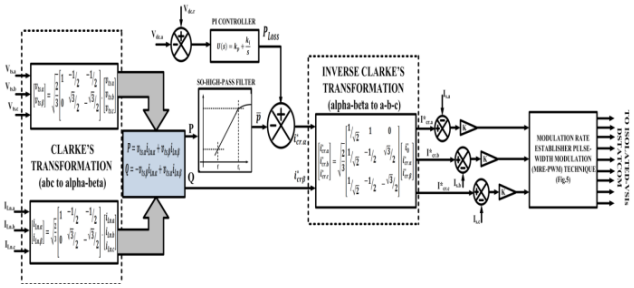

Figure-4. Schematic representation of IRP-PI control theory.

The schematic representation of IRP-PQ control theory is depicted in Figure-4, the extracted reference current ($i_{cr.abc}^*$) is processed with measured currents for generation of switching states to proposed 9-switch isolated-VSI of DSTATCOM using proposed Modulation-

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Rate Establisher Pulse-Width Modulation (MRE-PWM) technique.

PROPOSED MODULATION RATE ESTABLISHER-PULSE WIDTH MODULATION (MRE-PWM) TECHNIQUE

The proposed 9-switch isolated-VSI uses the single DC capacitor for sharing the currents between the two VSIs such as VSI-1 and VSI-2 both are differentiated by common switches. Hence, the current utilization for VSI-1 and VSI-2 is reduced up to 50% which implies the usage of low-rated switching devices with enhanced efficiency. The switching states of isolated-VSIs is relies on usage of reference current signal which is extracted from IRP-PQ control theory, these current quantities are multiplied with a constant 'k' to get reference voltages. Let the reference voltage of A-phase for VSI-1 is to be ($V^*_{cr.a1}$) and VSI-2 is to be ($V^*_{cr.a2}$). These reference voltage signals are processed to attain suitable switching states using PWM scheme. The regular PWM techniques in [19] are not perfectly operated because of common switches, for this a novel Modulation Rate Establisher based Pulse-Width Modulation (MRE-PWM) technique is proposed in this work. Assume that, reference voltages of both VSIs are $V^*_{cr.a1}$ and $V^*_{cr.a2}$ stated by,

$$V^*_{cr.a1} = V_1 \sin(2\pi f_1 t + \emptyset_1)$$
$$V^*_{cr.a2} = V_2 \sin(2\pi f_2 t + \emptyset_2) \quad (13)$$

Where, V_1 and V_2 are the magnitude of reference voltages, f_1, f_2 are the frequencies of reference voltages, $\emptyset_1, \emptyset_2$ is phase-angle. Let the distributed rate of voltage-utilization is to be defined as α, it ranges ($0 \leq \alpha \leq 1$). The equation for α is stated in Eqn. (14),

$$\alpha = \frac{V_1}{V_1 + V_2} \quad (14)$$

An offset value α is affixed to variations of reference voltages for both VSI-1 and VSI-2. The offset value determines the rate of modulation and is located on origin of divided carrier signal. Hence, the offset of respective VSIs are stated as,

$$\text{offset}_1 = 1 - \alpha$$
$$\text{offset}_2 = -\alpha \quad (15)$$

Thus, rate of modulation of phase-A is stated in Eqn. (16),

$$m_{u1} = \frac{V^*_{cr.a1}}{V_{dc}/2} + 1 - \alpha$$
$$m_{u2} = \frac{V^*_{cr.a2}}{V_{dc}/2} - \alpha \quad (16)$$

The maximum range of three-phase reference values $r_1 and\ r_2$ are defining for three-phase operation. Finally, the modulation and apportionment rate are stated in below Eqns. (17) & (18),

$$\alpha = \frac{|r_1|}{|r_1| + |r_2|} \quad (17)$$

$$m_1 = \frac{V^*_{cr.1}}{V_{dc}/2} + (1 - \alpha).e$$
$$m_2 = \frac{V^*_{cr.2}}{V_{dc}/2} - \alpha.e \quad (18)$$

Where,

$V^*_{ir} = [V^*_{cr.ai} \quad V^*_{cr.bi} \quad V^*_{cr.ci}]^T$

$m_i = [m_{ai} \quad m_{bi} \quad m_{ci}]^T$

$e = [1 \quad 1 \quad 1]^T$

$i = 1, 2;\ -1 \leq m_i \leq 1.$

A significant digital logic design is used for establishment of distributed modulation rate with definite offset values. These are compared with triangular carrier signals to attain suitable switching states for both VSI-1 and VSI-2 of isolated-VSI topology. The schematic diagram of MRE-PWM technique is depicted in Fig.5. The over-all representation of 9-switch isolated-VSIs DSTATCOM for PQ enhancement with proposed MRE-PWM technique is depicted in Figure-6.

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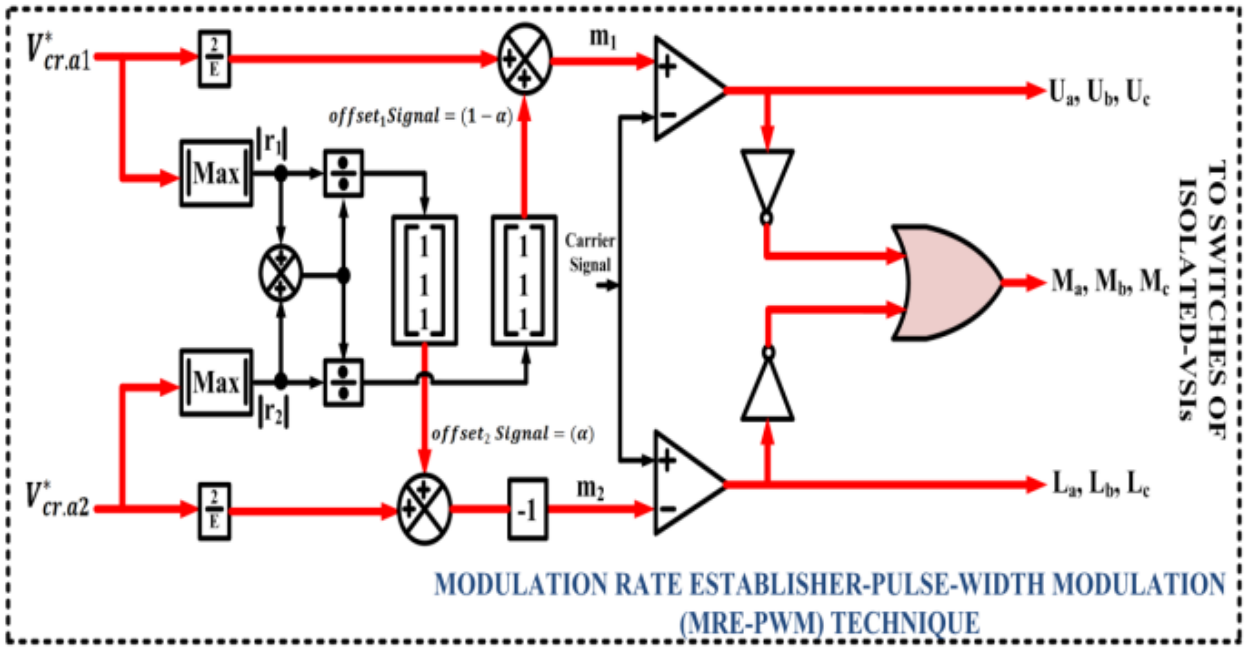

Figure-5. Proposed modulation rate establisher-pulse-width modulation (MRE-PWM) technique.

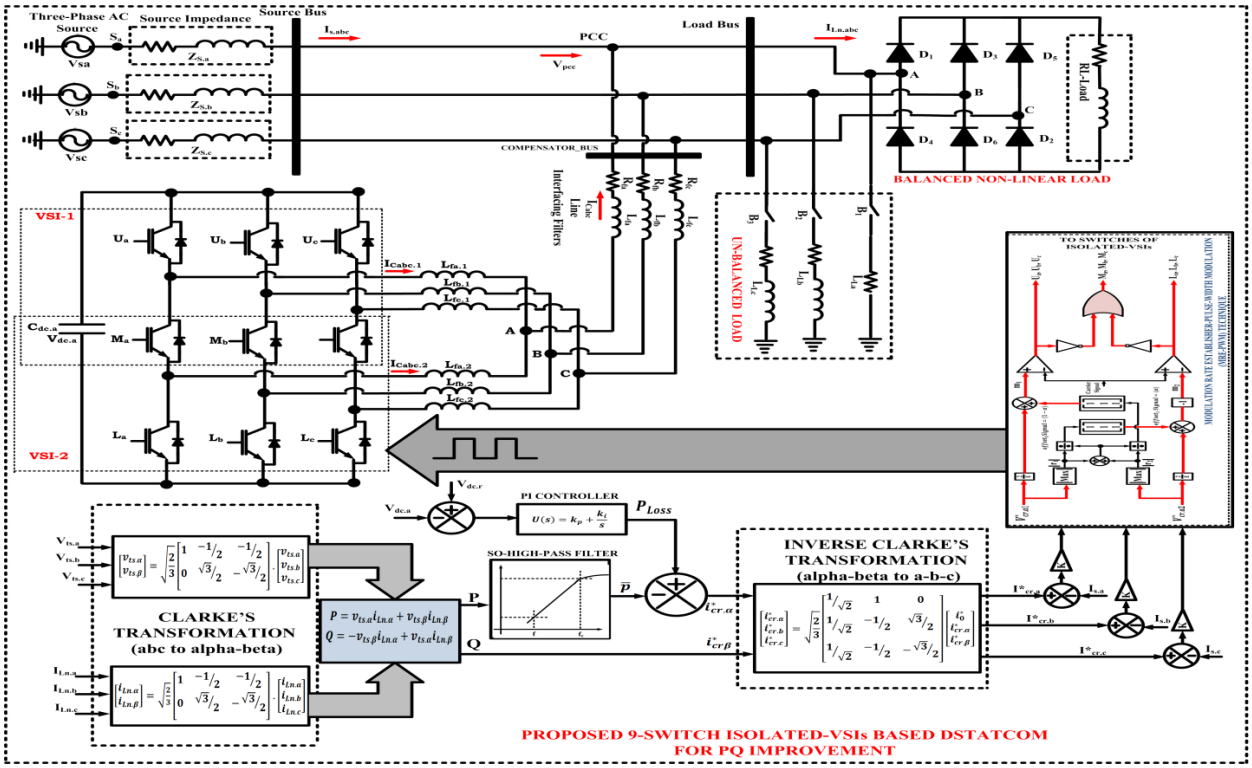

Figure-6. Over-all representation of 9-switch isolated-VSIs DSTATCOM for PQ enhancement with proposed MRE-PWM technique.

SIMULINK RESULTS AND DISCUSSIONS

The performance evaluation of proposed 9-switch isolated-VSIs DSTATCOM with MRE-PWM technique is verified under balanced, un-balanced and variable non-linear load conditions by using Matlab-Simulink computational tool, simulation results are presented. The system specifications of proposed scheme are depicted in Table-2.

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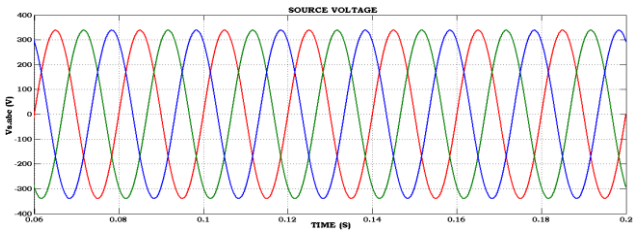
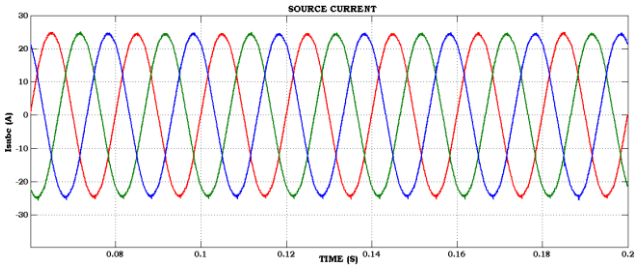
Table-2. System specifications of proposed scheme.

S. No	System Specifications	Values
1	Source Terminal Voltage	$V_{st.abc}$-415V (rms), F_{st}-50Hz
2	Source Terminal (line) Impedance	R_s-0.13Ω, L_s-0.92mH
3	Balanced Non-Linear Load Impedance	R_{Ln}-20Ω, L_{Ln}-30mH
4	Unbalanced Non-Linear Load Impedance	$R_{Ln.a}$-25Ω, $L_{Ln.a}$-30mH, $R_{Ln.b}$-25Ω, $R_{Ln.c}$-25Ω, $L_{Ln.c}$-30mH,
5	DC Capacitor	$C_{dc.a}$-4000µF
6	Line Interfacing Filter (Isolated-VSIs)	R_f-0.1; L_f-5mH
7	PI Control	K_{pdc}-0.5; K_{idc}-0.01

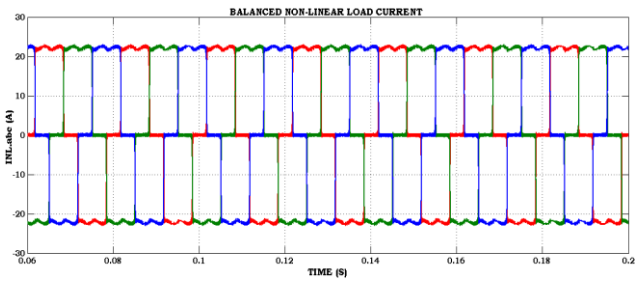
PERFORMANCE OF PROPOSED 9-SWITCH ISOLATED-VSIS DSTATCOM WITH MRE-PWM CONTROL SCHEME UNDER BALANCED NON-LINEAR LOAD



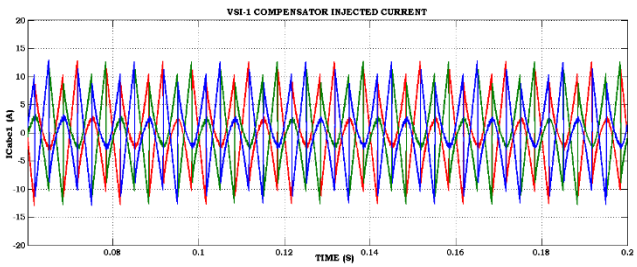
(a) Source terminal voltage



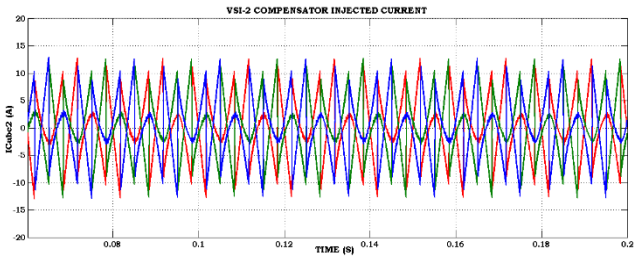
(b) Source or PCC current



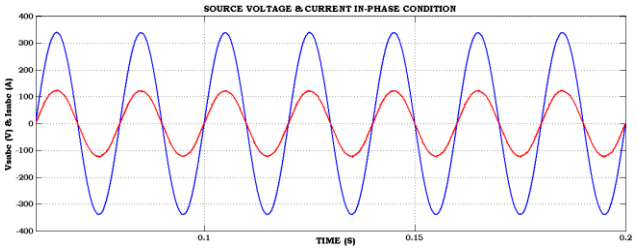
(c) Balanced non-linear load current



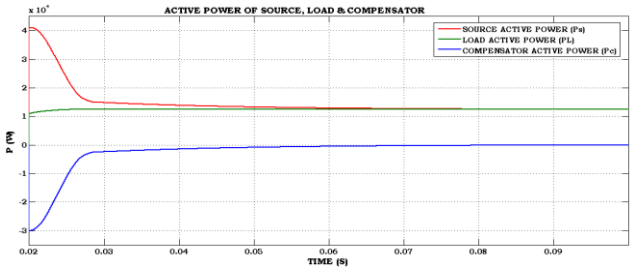
(d) VSI-1 Compensator injected currents



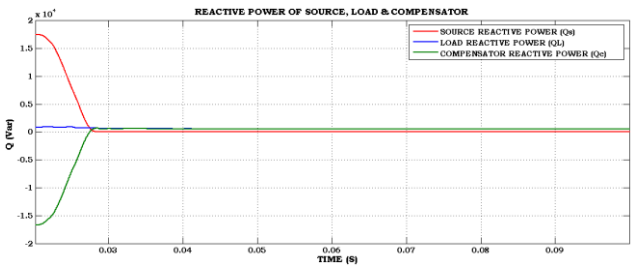
(e) VSI-2 Compensator injected currents



(f) Source terminal voltage and current in-phase (unity-PF) condition



(g) Active or real-power of source terminal, non-linear load and isolated VSI-compensator



(h) Reactive-power of source terminal, non-linear load and isolated VSI-compensator

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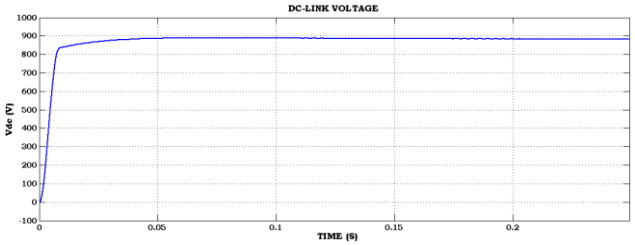
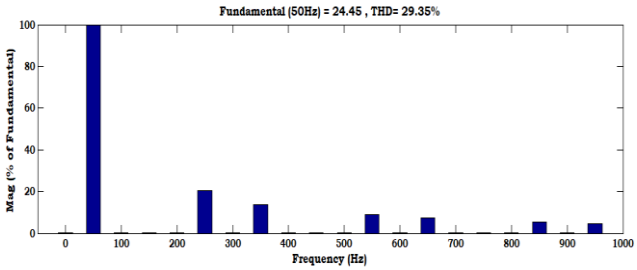
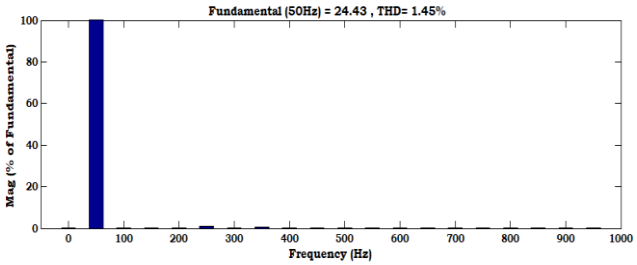


(i) Common DC-link voltage



(j) THD Value of balanced non-linear load current



(k) THD Value of source terminal current

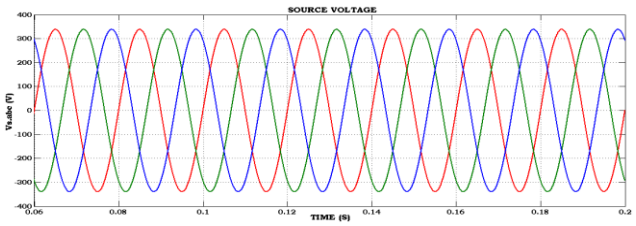
Figure-7. Simulated Results of Proposed 9-Switch Isolated-VSIs DSTATCOM with MRE-PWM Control Scheme under Balanced Non-Linear Load.

The simulated results of proposed 9-switch isolated-VSIs DSTATCOM with MRE-PWM control scheme under balanced non-linear load are depicted in Figure-7. They includes, (a) Source Terminal Voltage, (b) Source or PCC Current, (c) Balanced Non-Linear Load Current, (d) VSI-1 Compensator Injected Currents, (e) VSI-2 Compensator Injected Currents, (f) Source Terminal Voltage & Current In-Phase (Unity-PF) Condition, (g) Active or Real-Power of Source Terminal, Non-Linear Load & Isolated VSI-Compensator, (h) Reactive-Power of Source Terminal, Non-Linear Load & Isolated VSI-Compensator, (i) Common DC-Link Voltage (j) THD Value of Balanced Non-Linear Load Current, (k) THD Value of Source Terminal Current, respectively. The 3-phase distribution system is powered by three-phase 415Vrms voltage with a fundamental frequency of 50Hz is used to drive the balanced (Diode-Bridge) non-linear load. The source/PCC current of distribution network is proliferated due to the switching of non-linear loads; it disrupts the PCC current and may produce heat losses, damaging thermal security of other loads in distribution network.

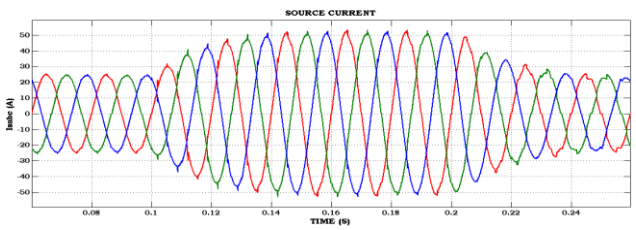
To achieve the perfect compensation, the required compensation current of 24A is shared by both VSI-1 and VSI-2 of isolated-VSIs device. The VSI-1 produces the 12A and VSI-2 produces the 12A, these dual-VSIs are integrated as parallel form to attain requisite compensation current of 24A comply with PQ enhanced features. With this compensation, the source terminal and non-linear load current maintained as constant with a value of 24.5A and 24A, respectively with constant PCC/source terminal voltage of 340V at peak magnitude. It regulates the harmonic current distortions, reactive-power control and load balancing at PCC and maintains PCC/source current and voltage as sinusoidal, balanced, linear and fundamental nature. Based on this compensation, the source/PCC current is in-phase coordination with source/PCC voltage to represent unity-power factor at PCC level.

The three-phase AC source produces the rated real-reactive power of 12.5KW and 0.01 KVar to fulfill the load demand as required real-reactive power of 12.4 KW and 0.55KVar, respectively. The required real power for non-linear load has been supported by source's real power, but the reactive-power of load is supported by DSTATCOM which regulates the reactive-power of load. The isolated-VSIs DSTATCOM injects the required reactive power of 0.55KVar and it doesn't support any real-power in PQ compensation mode. The input DC value of isolated-VSIs is always maintained as constant of 880V which reduces the flow of circulation currents and reduces the switching losses of VSIs. The source and load currents are equal in non-compensation mode due to presence of non-linear balanced loads. The measured THD of non-linear balanced load current is 29.35%, due to switching of balanced non-linear load device. The THD of source/PCC current is 1.45%, thus complying with IEEE-519-1992 standards due to presence of proposed isolated dual-VSIs DSTATCOM driven by proposed MRE-PWM technique.

PERFORMANCE OF PROPOSED 9-SWITCH ISOLATED-VSIS DSTATCOM WITH MRE-PWM CONTROL SCHEME UNDER VARIABLE BALANCED NON-LINEAR LOAD



(a) Source terminal voltage



(b) Source or PCC current

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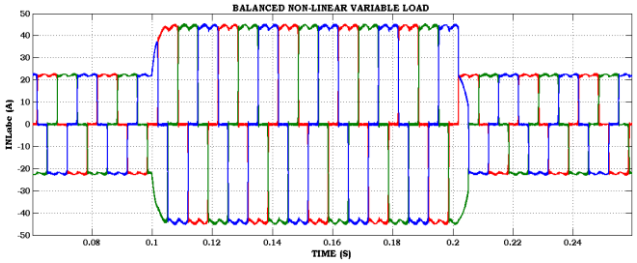
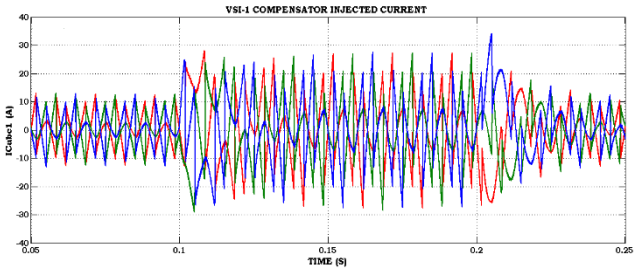
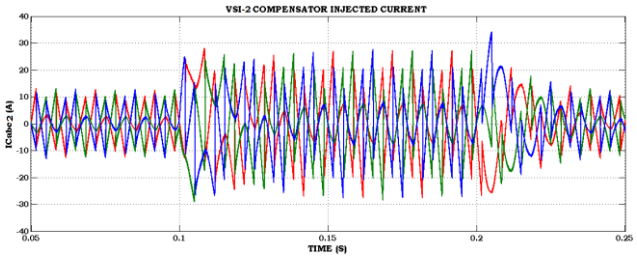


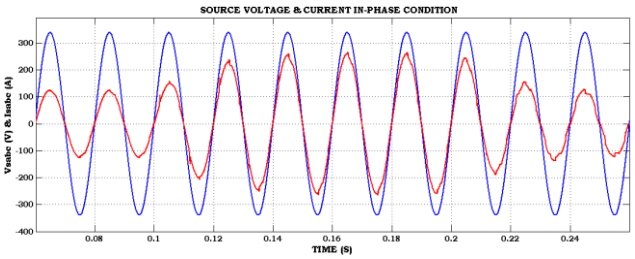
(c) Balanced non-linear load current



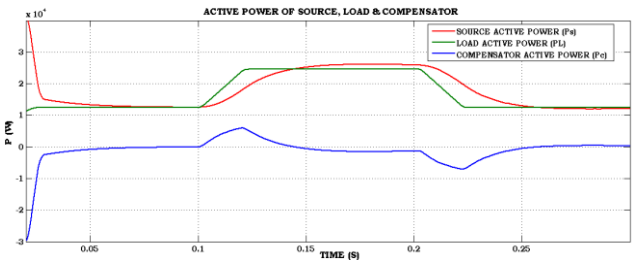
(d) VSI-1 Compensator injected currents



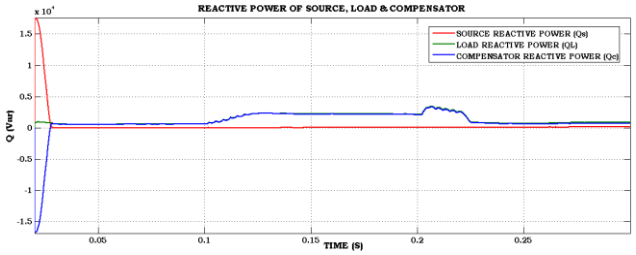
(e) VSI-2 Compensator injected currents



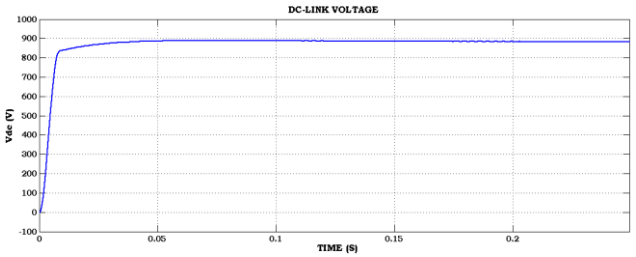
(f) Source terminal voltage and current in-phase (unity-PF) condition



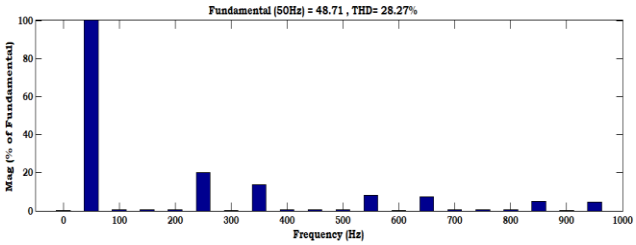
(g) Active or real-power of source terminal, non-linear load and isolated VSI-compensator



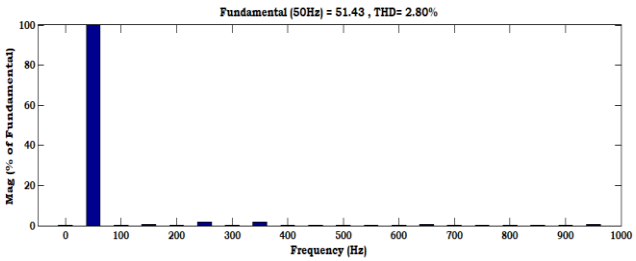
(h) Reactive-power of source terminal, non-linear load and isolated VSI-compensator



(i) Common DC-link voltage



(j) THD Value of balanced non-linear load current



(k) THD Value of source terminal current

Figure-8. Simulated Results of Proposed 9-Switch Isolated-VSIs DSTATCOM with MRE-PWM Control Scheme under Variable Balanced Non-Linear Load

The simulated results of proposed 9-switch isolated-VSIs DSTATCOM with MRE-PWM control scheme under variable balanced non-linear load are depicted in Figure-8. Due to this sudden switching of load at time between 0.1 sec<t< 0.2sec, which produces the sudden deviations in source/PCC current and affecting stable operation of loads integrated at PCC level.

At instant before t-0.1 sec, the required compensation current of 24A is shared by both VSI-1 and VSI-2 to achieve the required compensation currents provided by isolated-VSIs DSTATCOM. The VSI-1 produces the 12A and VSI-2 produces the 12A, these dual-VSIs are integrated as parallel form to attain requisite compensation current of 24A comply with PQ enhanced features. With this compensation, the source terminal and

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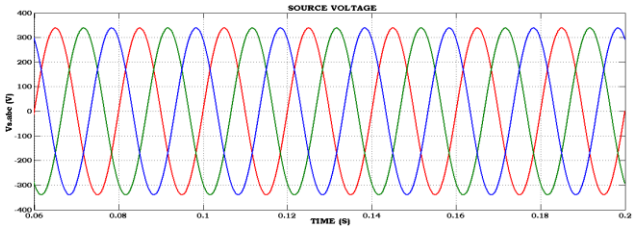
non-linear load current maintained as constant with a value of 24.5A and 24A, respectively with constant PCC/source terminal voltage of 340V at peak magnitude.

During sudden load switching 0.1 sec<t<0.2 sec, the required compensation current of 52A is shared by both VSI-1 and VSI-2 to achieve the required compensation currents provided by isolated-VSIs DSTATCOM. The VSI-1 produces the 26A and VSI-2 produces the 26A, these dual-VSIs are integrated as parallel form to attain requisite compensation current of 52A comply with PQ enhanced features. With this compensation, the source terminal and non-linear load current maintained as constant with a value of 52.5A and 49.5A, respectively with constant PCC/source terminal voltage of 340V at peak magnitude. It regulates the sudden load change distortions, harmonic current compensation, reactive-power control and load balancing at PCC, maintains PCC/source current and voltage as sinusoidal, balanced, linear, fundamental nature and unity-power factor at PCC level.

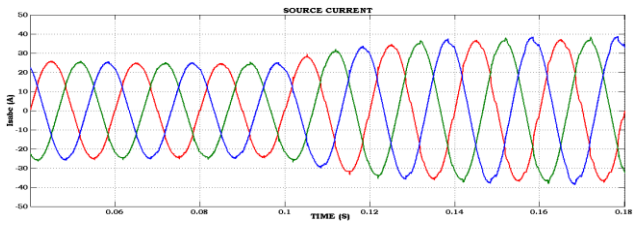
At instant before t-0.1 sec, the three-phase AC source produces the rated real-reactive power of 12.5KW and 0.01 KVar to fulfill the load demand as required real-reactive power of 12.4 KW and 0.55KVar, respectively. The required real power for non-linear load has been supported by source's real power, but the reactive-power of load is supported by DSTATCOM which regulates the reactive-power of load. The isolated-VSIs DSTATCOM injects the required reactive power of 0.55KVar and it doesn't support any real-power in PQ compensation mode.

During sudden load switching at 0.1 sec<t<0.2 sec, the three-phase AC source produces the rated real-reactive power of 25.1KW and 0.05 KVar to fulfill the variable load demand as required real-reactive power of 24.9 KW and 2.2KVar, respectively. The required real power for non-linear load has been supported by source's real power, but the reactive-power of load is supported by DSTATCOM which regulates the reactive-power of load. The isolated-VSIs DSTATCOM injects the required reactive power of 2.2KVar and it doesn't support any real-power in PQ compensation mode. The input DC value of isolated-VSIs is always maintained as constant of 880V which reduces the flow of circulation currents and reduces the switching losses of VSIs. The source and load currents are equal in non-compensation mode due to presence of variable-balanced non-linear load. The measured THD of non-linear load current is 28.27%, during switching of variable balanced non-linear load device. The THD of source/PCC current is 2.80%, thus complying with IEEE-519-1992 standards.

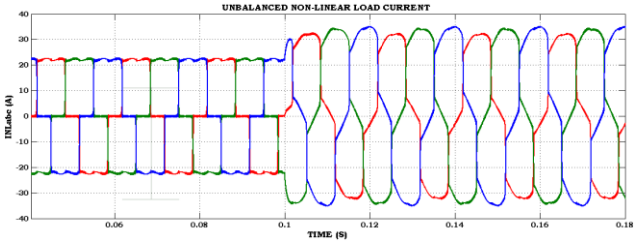
PERFORMANCE OF PROPOSED 9-SWITCH ISOLATED-VSIS DSTATCOM WITH MRE-PWM CONTROL SCHEME UNDER SWITCHING OF BALANCED TO UNBALANCED NON-LINEAR LOAD



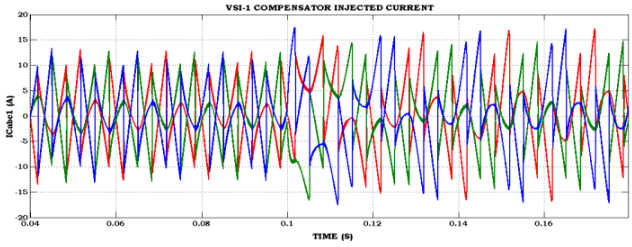
(a) Source terminal voltage



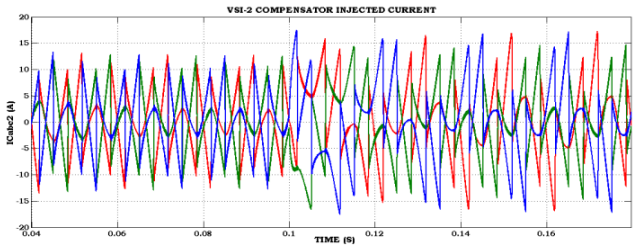
(b) Source or PCC current



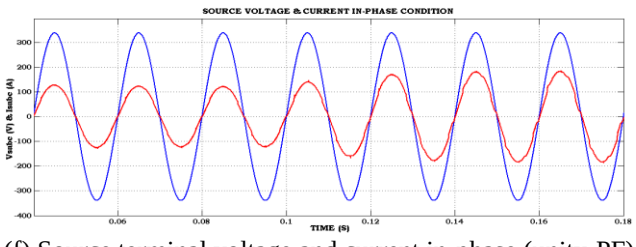
(c) Balanced non-linear load current



(d) VSI-1 Compensator injected currents



(e) VSI-2 Compensator injected currents



(f) Source terminal voltage and current in-phase (unity-PF) condition

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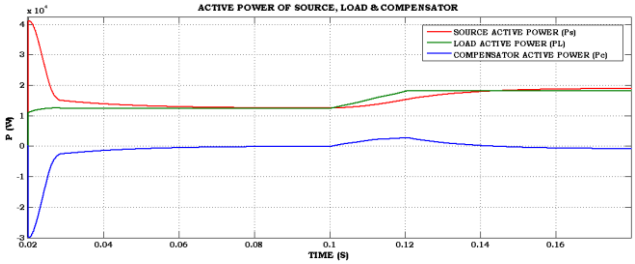
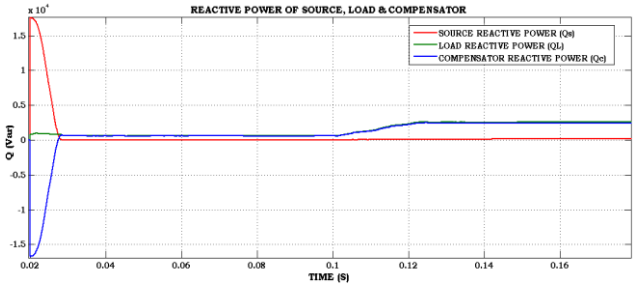
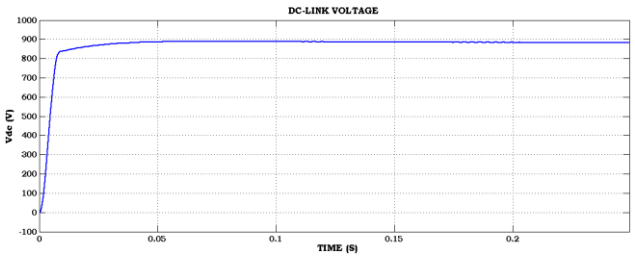


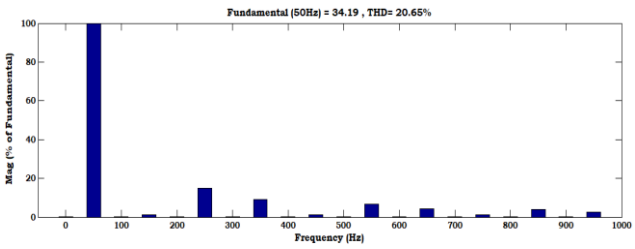
(g) Active or real-power of source terminal, non-linear load and isolated VSI-compensator



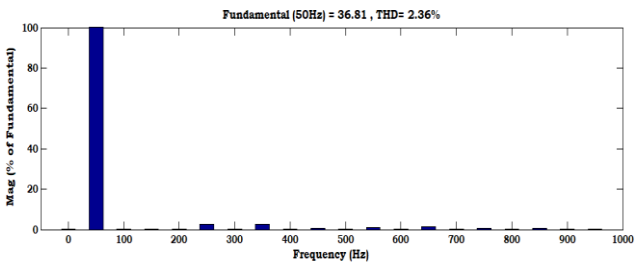
(h) Reactive-power of source terminal, non-linear load and isolated VSI-compensator



(i) Common DC-link voltage



(j) THD Value of balanced non-linear load current



(k) THD Value of source terminal current

Figure-9. Simulated Results of Proposed 9-Switch Isolated-VSIs DSTATCOM with MRE-PWM Control Scheme under Switching of Balanced to Un-Balanced Non-Linear Load.

The simulated results of proposed 9-switch isolated-VSIs DSTATCOM with MRE-PWM control scheme under switching of balanced to unbalanced non-linear load are depicted in Fig.9. Due to this sudden switching of load at time t-0.1 sec, which produces the sudden deviations in source/PCC current, it disrupts the stable operation, may produce heat losses, damaging thermal security of other loads in distribution network.

During balanced non-linear load switching at instant before t-0.1 sec, the required compensation current of 24A is shared by both VSI-1 and VSI-2 to achieve the required compensation currents provided by isolated-VSIs DSTATCOM. The VSI-1 produces the 12A and VSI-2 produces the 12A, these dual-VSIs are integrated as parallel form to attain requisite compensation current of 24A comply with PQ enhanced features. With this compensation, the source terminal and non-linear load current maintained as constant with a value of 24.5A and 24A, respectively with constant PCC/source terminal voltage of 340V at peak magnitude.

During sudden switching of unbalanced load at instant after t-0.1 sec, the required compensation current of 35A is shared by both VSI-1 and VSI-2 to achieve the required compensation currents provided by isolated-VSIs DSTATCOM. The VSI-1 produces the 17.5A and VSI-2 produces the 17.5A, these dual-VSIs are integrated as parallel form to attain requisite compensation current of 35A comply with PQ enhanced features. With this compensation, the source terminal and non-linear load current maintained as constant with a value of 36A and 34A, respectively with constant PCC/source terminal voltage of 340V at peak magnitude. It regulates the sudden load change distortions, harmonic current compensation, reactive-power control and load balancing at PCC, maintains PCC/source current and voltage as sinusoidal, balanced, linear and fundamental nature. Based on this compensation, the source/PCC current is in-phase coordination with source/PCC voltage to represent unity-power factor at PCC level.

At instant before t-0.1 sec, the three-phase AC source produces the rated real-reactive power of 12.5 KW and 0.01 KVar to fulfill the load demand as required real-reactive power of 12.4 KW and 0.55 KVar, respectively. The required real power for non-linear load has been supported by source's real power, but the reactive-power of load is supported by DSTATCOM which regulates the reactive-power of load. The isolated-VSIs DSTATCOM injects the required reactive power of 0.55KVar and it doesn't support any real-power in PQ compensation mode.

At instant after t-0.1 sec, the three-phase AC source produces the rated real-reactive power of 19.5KW and 0.02 KVar to fulfill the load demand as required real-reactive power of 18.2 KW and 2.5 KVar, respectively. The required real power for non-linear load has been supported by source's real power, but the reactive-power of load is supported by DSTATCOM which regulates the reactive-power of load. The isolated-VSIs DSTATCOM injects the required reactive power of 2.5 KVar and it doesn't support any real-power in PQ compensation mode. The input DC value of isolated-VSIs is always maintained

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as constant of 880V which reduces the flow of circulation currents and reduces the switching losses of VSIs. The source and load currents are equal in non-compensation mode due to presence of variable-balanced and unbalanced non-linear load. The measured THD of non-linear load current is 20.65%, during switching of variable balanced non-linear load device. The THD of source/PCC current is 2.36%, thus complying with IEEE-519-1992 standards. The THD comparison of non-linear load current and source/PCC current under without DSTATCOM and with proposed 9-switch isolated-VSIs DSTATCOM under various load devices is depicted in Table-3 followed by bar-chart is depicted in Figure-10.

Table-3. THD Comparison of non-linear load current and source/PCC current under without DSTATCOM and with proposed 9-switch isolated-VSIs DSTATCOM under various load devices.

THD (%)	Non-Linear Load Current			Source/PCC Current		
	Balanced Load	Un-Balanced Load	Variable Load	Balanced Load	Un-Balanced Load	Variable Load
Without DSTATCOM	30.15%	22.38%	29.15%	29.23%	20.12%	27.98%
With Isolated VSIs DSTATCOM	29.35%	20.65%	28.27%	1.45%	2.36%	2.80%

The performance comparison of proposed isolated-VSIs DSTATCOM over Conventional Topologies is illustrated in Table-4. Over the conventional techniques, the proposed isolated-VSIs DSTATCOM carries high current sharing between the VSIs with a reduced THD value of 1.45% well within IEEE-519 compliances. The proposed isolated-VSIs DSTATCOM carries low KVA rating capacity VSIs with a power of 3 KVA which is very low over the conventional techniques. The dual-VSIs DSTATCOM requires 12 switches and the proposed isolated-VSIs DSTATCOM requires only 9 switches which reduces the size, cost and complex design of DSTATCOM.

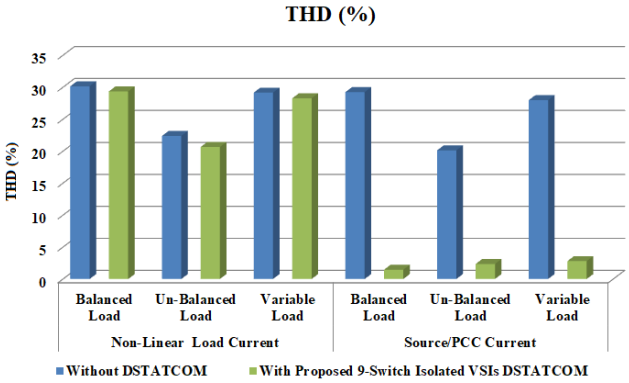

Figure-10. Bar-Chart of THD comparisons.

Table-4. Performance comparison of proposed isolated-VSIs DSTATCOM over conventional topologies.

	Three-Phase DSTATCOM [6]	Zig-Zag Transformer-DSTATCOM [10]	Dual-VSI DSTATCOM [12]	Proposed Isolated-VSIs DSTATCOM
Current Sharing by VSI	24 A	18A	14.5A	12.5A
THD of Source Current	10.4%	4.2%	2.88%	1.45%
KVA Power Value	20 KVA	12 KVA	8 KVA	3 KVA
Number of Switches	6 no.s	6 no.s	12 no.s	9 no.s

CONCLUSIONS

The performance of proposed 9-switch isolated-VSIs DSTATCOM is verified during compensation of harmonic currents, reactive-power regulation, load balancing and power-factor improvement under balanced, unbalanced and variable load conditions. Over the conventional dual-VSIs DSTATCOM requires more switching devices likely 12 devices and the proposed 9-switch isolated-VSIs requires only 9 switches which provides the current sharing between the VSIs. Thus, it reduces the device ratings, cost, size and complex design, reliable operation, increases the efficiency of over-all compensation scheme over the conventional topologies. The switching of isolated-VSIs are relies on usage of reference current signal which is extracted from IRP-PQ control theory followed by novel MRE-PWM technique. The proposed MRE-PWM driving proposed 9-switch isolated-VSIs DSTATCOM compensate various current-PQ issues and maintain PCC specifications as balanced, sinusoidal, linear and fundamental nature.

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