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SINGLE-PHASE MULTI-LEVEL INVERTER: NEW PARALLEL TOPOLOGY FOR PHOTOVOLTAIC SYSTEMS

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ABSTRACT

In recent years, the multilevel DC/AC static converters are increasingly used for their benefits especially in terms of reduction of total harmonic distortion (THD) of the output current and reduced voltage stress on semiconductors at switching moments. In this article, a parallel structure of inverter is proposed for systems using photovoltaic panels. Although the proposed structure requires a number of voltage sources more than that used in other structures proposed in the literature, this structure has the advantage of being simple, contains only semiconductors for switching (no additional components as switching capacitors are required), and easy logic of control of semiconductors. The used modulation is based on the sinusoidal fundamental frequency pulse width modulation technique with single carrier. The proposed structure with its command scheme is adapted to voltage source inverter (VSI) applications. The inverter performances are evaluated through simulations in Matlab-Simulink environment on a nine-level inverter example.

Keywords: parallel multilevel inverter, photovoltaic panel, total harmonic distortion, switching losses, voltage stress.

INTRODUCTION

Currently, multi-level inverters are preferred over conventional two or three-level inverters due to their confirmed advantages. Actually in the literature there are many papers which present and discuss various topologies of multi-level inverters and mention the benefits of their structures [1]. This is indeed the case of the following advantages:

- Reduction of stress voltage applied to the power semiconductors, which allows these inverters to be able to transfer higher powers with dv / dt and di / dt significantly lower than those obtained with inverters at two levels [2], [3];
- Reduction of electromagnetic noise (EMI) and the total harmonic distortion (THD) of the output waves, which reduces the size of the output filter [4], [5].

Certainly, multilevel inverters also have disadvantages such as: the number of semiconductors and voltage sources (isolated or not) necessary for the operation of these inverters, which increases with the increase in the required number of voltage levels. Also, the majority of structures of multi-level inverters require the use of other components such as capacitors or transformers [6]-[8], which conducts to a more complex structure and an increase in the overall price of the inverter [4].

This article presents a parallel topology of multi-level inverter switches. This topology needs as many voltage sources connected in series as the levels required. This is why this solution is suitable for solar systems since the batteries and photovoltaic panels are necessarily connected in series to have sufficient voltage for the DC bus. The remainder of this article is organized as follows: In Section II, a review of the main topologies of multi-level inverters. Section III presents the principle diagram of the proposed topology first, and the control diagram of the switches secondly. In section IV, the simulation results are presented justifying the correct operation and performance of the proposed solution. Finally, in section V, this article is completed by a conclusion.

MULTILEVEL INVERTER TOPOLOGIES OVERVIEW

Generally, multilevel inverters are classified into three categories: Neutral-point-clamped (NPC) inverters (see Figure-1), Flying capacitor (FC) inverters (see Figure-2), and Multi-cell multilevel (ML) inverters (see Figure-3).

Neutral-point-clamped (NPC) inverters are the most widely used multilevel inverter topology in high power applications. Figure-1 shows some variants of this topology. Figure-1ab shows the topology of a three-level and five-level inverter respectively. However, in this type of circuit diagram, the power losses are asymmetrically distributed between the power switches, which lead to a limitation (due to the most heavily used switches) of the power capability at the output of the inverter. For this reason, improvements are made on the basic NPC topology to overcome this drawback: Figure-1c shows the use of clamping diodes to balance the converter; while Figure-1d shows the active neutral-point-clamped (ANPC) topology, where clamping diodes are replaced by transistors with antiparallel diodes for providing a controllable pathway for neutral current [9].

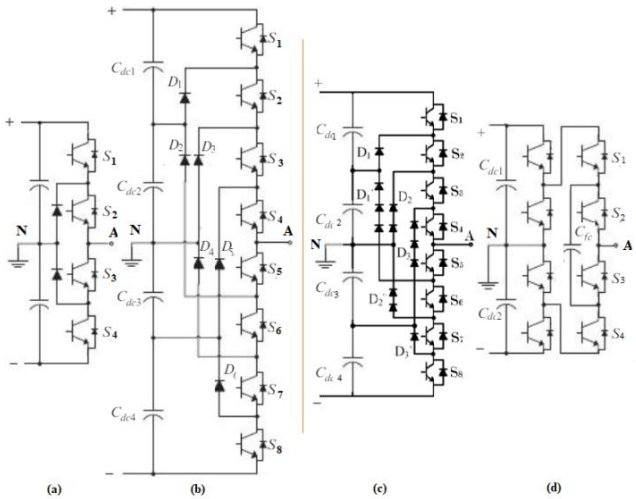

Figure-1. Phase leg of NPC inverter topologies: (a) 3 levels diode clamped NPC, (b) 5 levels diode clamped NPC, (c) 5 levels NPC with balancing diodes, (d) 5 levels ANPC inverter.

The structure of multilevel flying capacitor inverters suffers from several disadvantages which limit its use in practice; among these major drawbacks we can cite:

- Need for capacitor with sufficient value for each voltage level;
- Need for charging circuit for each flying capacitor;
- Need for complicated procedures to balance capacitor voltages.

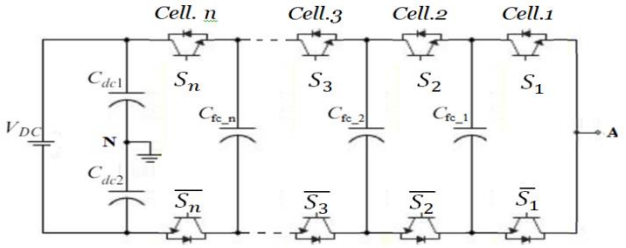

Figure-2. Multi-cell multilevel inverter topology with flying capacitors

The Multi-cell multi-level inverters are based on the use of cascaded power cells. The different cells are controlled in a way to have all the configurations allowing producing the required output voltage levels. For this category of converters, a distinction is made between multi-cell cascade H-bridge (CHB) topologies, which require isolated power supply for each basic cell (see Figure-3a), and modular multi-level converters (MMC) whose cells share the same DC voltage source as shown in Figure-3b.

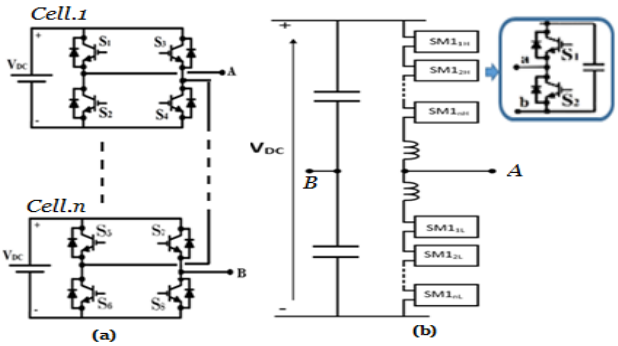

Figure-3. Cascaded Multi-cell multilevel inverter topologies: (a) Cascaded H-Bridge (CHB) (b) modular multilevel converter (MMC).

The major advantage of multicellular topologies is that they are modular, which makes it easier to design and maintain. However, they require a large number of active and passive components. Also, there is the problem of unbalanced voltages across capacitors [1].

In the literature of multilevel inverters, several structures are proposed to improve the three classic topologies mentioned above. The improvements concern, on the one hand, to reduce the number of components and switches required, and on the other hand, to reduce stress on the switches. The structure proposed in [4] is composed of two asymmetric sub-circuits (see Figure-4).

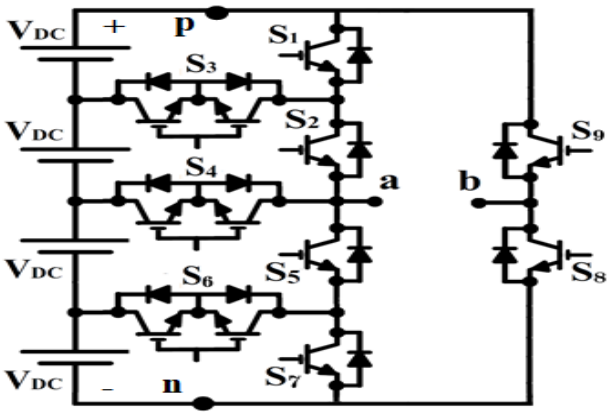

Figure-4. Scheme of Nine-Switches Nine-Levels inverter.

The basic module of this topology (Figure-5c) uses a combination of one or more T-type modules (Figure-5a) and a single half-bridge module (Figure-5b). The T-type module makes it possible to have (0, Vdc and 2Vdc) voltages at its output (terminal A) depending on the closed switch (S2, S0 and S1) respectively. While the half bridge (Figure-5b) allows to have a symmetrical voltage (taking as reference the potential of point n for a positive output, and as reference the potential of point n' for a negative output). The concept of this structure can be simply duplicated to achieve as many voltage levels as required.

It should be noted that in this topology (Figure-4), the switches must resist to different voltage constraints.

So all switches except S8 and S9 must only support voltage Vdc, while switches S8 and S9 must be able to block the entire voltage. However, the last two switches operate at the fundamental switching frequency, which greatly reduces switching losses in these switches.

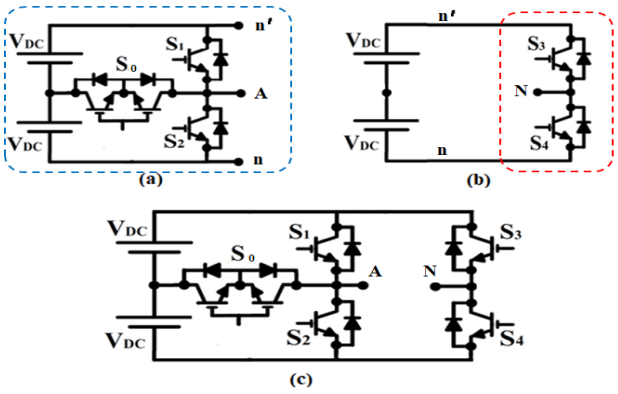

Figure-5. Main sub-modules used as basic units of MLIs: a) T-type b) half-bridge; c) Combination of T-type and half-bridge sub-modules.

PROPOSED MULTI-LEVEL PARALLEL TOPOLOGY

Basic Structure and Switches Control Strategy

The parallel topology proposed in this work, is inspired by the basic sub-module shown in Figure-5a and Figure-6a. In fact, the output (Figure-6a) is taken at point A as in Fig 5a, but the neutral is fixed at point N, unlike in Figure-5c, where the neutral point toggles between points n and n' (via switches S3 and S4) according to the desired sign of the output voltage. Figure-6b shows the scheme of an inverter with 5 levels, the performed modification to the switches SH1 and SL1, is justified by the fact that these switches must withstand negative voltages when switch SH2 or SL2 are on.

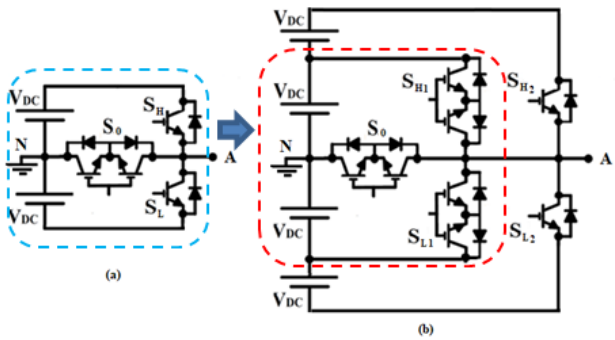

Figure-6. Parallel structure; (a) T-type sub-module, (b) Five levels inverter.

Figure-7 shows the proposed parallel structure for 2k+1 levels inverter. Each voltage source is associated with a switch. The number of voltage levels in this structure can therefore be simply increased by adding pairs of voltage sources and associated switches. It should be noted that for symmetry reasons number of voltage sources must be pair. The switches (SH1, SH2 … SH2k+1) are used to have positive voltages, and the switches (SL1, SL2 … SL2k+1) for negative voltages; while the S0 switch is closed to have the zero level.

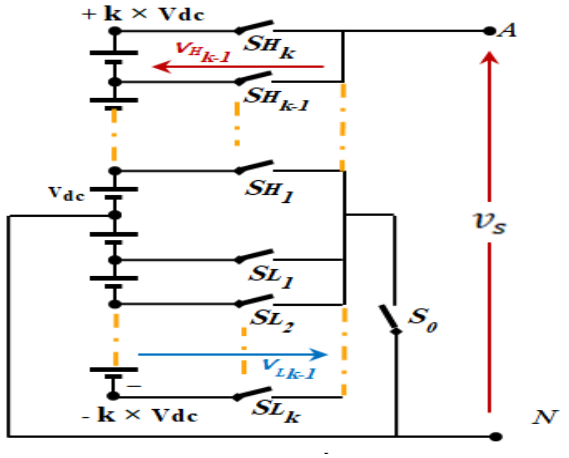

Figure-7. Single-phase inverter topology of (2k+1) levels (PVSI) topology.

Table-1 illustrates the states of the switches to obtain the different possible voltage levels for a nine levels inverter. It may be noted that always only one switch is closed at a time.

Table-1. Parallel-nine-level inverter: Voltage levels and corresponding switch states.

Switch ON	S_{H4}	S_{H3}	S_{H2}	S_{H1}	S_0	S_{L1}	S_{L2}	S_{L3}	S_{L4}
Output Voltage	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	$-4V_{dc}$

All The switches except SH2k+1 and SL2k+1 must be bidirectional in voltage, because, once a switch is closed, it imposes a negative voltage on the other open switches. Table-2 gives the different voltages applied to the blocked switches. It is clear that each switch must withstand a forward voltage equal to twice the voltage of the switched level, and a maximum reverse voltage (for the switch (S0) connected to the neutral point) equal to the voltage corresponding to the maximum level.

Table-2. Voltages at the terminals of each switch used in the proposed structure (Case of a 9-level inverter).

Switch ON	Voltage applied to the switch								
	S_{H4}	S_{H3}	S_{H2}	S_{H1}	S_0	S_{L1}	S_{L2}	S_{L3}	S_{L4}
S_{H4}	0	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$7V_{dc}$	$8V_{dc}$
S_{H3}	V_{dc}	0	$-V_{dc}$	$-2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$7V_{dc}$
S_{H2}	$2V_{dc}$	V_{dc}	0	$-V_{dc}$	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$
S_{H1}	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$5V_{dc}$
S_0	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	V_{dc}	0	V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$
S_{L1}	$5V_{dc}$	$4V_{dc}$	$3V_{dc}$	$2V_{dc}$	$-V_{dc}$	0	V_{dc}	$2V_{dc}$	$3V_{dc}$
S_{L2}	$6V_{dc}$	$5V_{dc}$	$4V_{dc}$	$3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0	V_{dc}	$2V_{dc}$
S_{L3}	$7V_{dc}$	$6V_{dc}$	$5V_{dc}$	$4V_{dc}$	$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0	V_{dc}
S_{L4}	$8V_{dc}$	$7V_{dc}$	$6V_{dc}$	$5V_{dc}$	$-4V_{dc}$	$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	0

The control strategy of this inverter consists of closing one switch corresponding to the required voltage level. The switches are closed according to the sequence shown in Figure-8 (full arrow to increase the voltage level and empty arrow to decrease it). It should be noted that all the switches (according to the control sequence mentioned above and Table-2 of voltages applied to the switches) have a voltage not exceeding Vdc before and after switching, this greatly reduces the voltage constraints on the switches used in this topology [4].

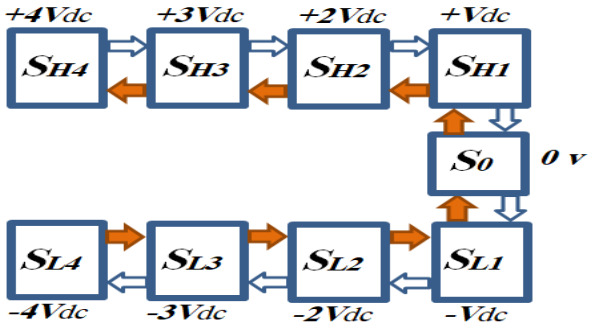

Figure-8. Switch control sequence and output voltage corresponding to the closed switch.

Since this structure requires as many voltage sources as the number of levels required, it can be a very interesting solution in photovoltaic systems, where the solar panels are connected in series to construct the PV string. Indeed, the proposed topology takes advantage of the series connection of the PVs [9]-[14]. Figure-9a shows the wiring diagram from PV to conventional inverters (two or three levels), while Figure-9b shows how to access to required voltage levels.

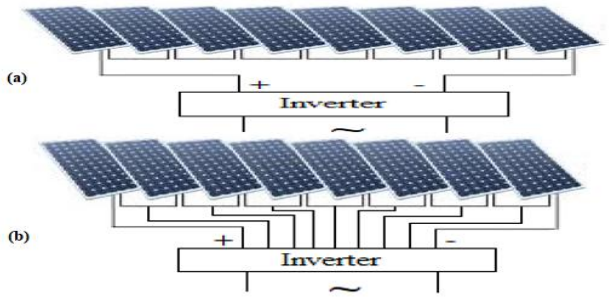

Figure-9. Inverter power supply: (a) for classical inverters; (b) for proposed nine-levels inverter.

Multilevel PWM Scheme

One of the advantages of multi-level inverters is that they obtain an almost sinusoidal wave, this leads to a significant reduction in the size of the output filter. But to achieve this objective it is necessary to greatly increase the number of voltage levels, which considerably increases the complexity and the price of the converter. One solution to this problem is to use PWM with a rather low modulation frequency compared to those used with 2 or 3-level inverters [4]. The major advantage of a low modulation frequency is the reduction of switching losses.

Although there are many techniques for pulse width modulation, the multi-carrier-based sinusoidal pulse-width modulation (MSPWM) technique (based on the use of multiple carriers) is one of the most generally used modulation methods for multi-level structures [4], [9], [14]. The Hybrid Multilevel PWM (HMPWM) consisting of a combination of modified MSPWM and the fundamental frequency modulation (FFM) is a novel technique proposed in [4]. In this article, a single-carrier modulation is used, to achieve the PWM control. The proposed scheme of used PWM is shown in Figure-10. It can be seen that it is much simpler to implement this control since it utilizes just comparators and a multiplexer (no phase shifters). The use of multiplexer is justified since in this proposed topology only one switch is on at any time. This proposed scheme has also the advantage of

varying (via the peak value) the RMS amplitude of reference sin wave voltage (in the entire range from 0 to k×Vdc) without any modification of the structure. Figure-11 shows the different signals obtained according to the proposed modulation scheme. The multiplexer is used to control the switches according to the look-up table (see Table-3) depending on the voltage level.

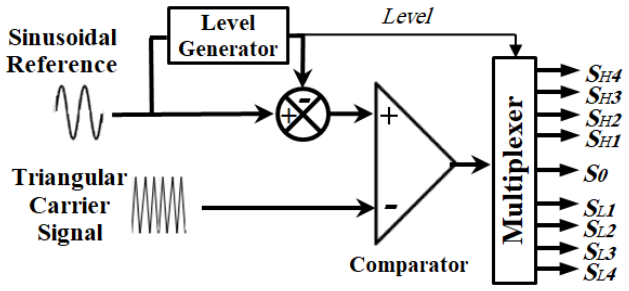

Figure-10. Block diagram of the proposed PWM scheme controlling the nine power switches.

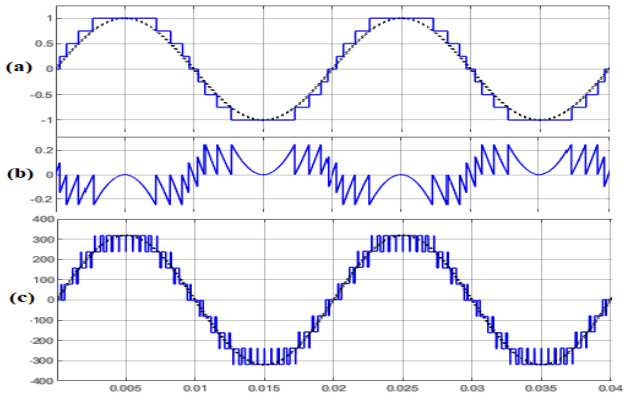

Figure-11. Control and Reference signals corresponding to nine levels: (a) Output signal of the generator block of the voltage levels without PWM with sinusoidal waveform; (b) Reference signal, (c) Output voltage with PWM.

Table-3. Look-up table of pairs of switches to be switched according to the actual voltage level.

v_s	Switches States								
	S_{H4}	S_{H3}	S_{H2}	S_{H1}	S_0	S_{L1}	S_{L2}	S_{L3}	S_{L4}
$4V_{dc}/3V_{dc}$	1/0	0/1	0	0	0	0	0	0	0
$3V_{dc}/2V_{dc}$	0	1/0	0/1	0	0	0	0	0	0
$2V_{dc}/V_{dc}$	0	0	1/0	0/1	0	0	0	0	0
$V_{dc}/0$	0	0	0	1/0	0/1	0	0	0	0
$-V_{dc}/0$	0	0	0	0	0/1	1/0	0	0	0
$-2V_{dc}/-V_{dc}$	0	0	0	0	0	0/1	1/0	0	0
$-3V_{dc}/2V_{dc}$	0	0	0	0	0	0	0/1	1/0	0
$-4V_{dc}$ $/-3V_{dc}$	0	0	0	0	0	0	0	0/1	1/0

Case of a nine-level inverter.

SIMULATION RESULTS AND PERFORMANCES EVALUATION

The following simulations of the proposed inverter in this article are performed using MATLAB / SIMULINK. Table-4 listed below summarizes the simulation parameters.

Table-4. Simulation system parameters.

Parameters	values
Matlab Sample time Ts	0.5e-5 s
DC Source Voltage Vdc	125 V
PWM frequency	None, 1 kHz, 5 kHz
Load Active Power	10 kW
Load Inductive Reactive Power	10 kVAR / 2 kVAR
Load Nominal Voltage (RMS)	480 V
Load Nominal Frequency	50 Hz

These simulations are performed for a nine-level, nine-switch single-phase voltage inverter used without an output filter. The performance evaluation of the proposed multi-level inverter is based on the comparison of the output current THDs, in different situations, in particular, for different loads and PWM frequencies. The switching frequencies are chosen not to be high in order to reduce the power losses in the semiconductor components and the loads used are inductive. The output voltage of the inverter must have a frequency and an effective value fixed by a sinusoidal reference signal.

Figure-12 to Figure-17 show the simulation results corresponding to the output voltage (part (a)), the output current (part (b)) and the total harmonic distortion (part (c)) for different loads and PWM frequencies. All simulations are performed in the following order: 480V, 230V, 380V and 125V for RMS reference voltage.

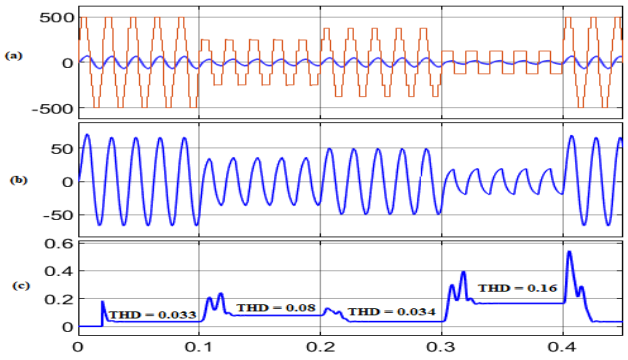

Figure-12. Simulation results (case of a 10kW / 10kVar load, without modulation).

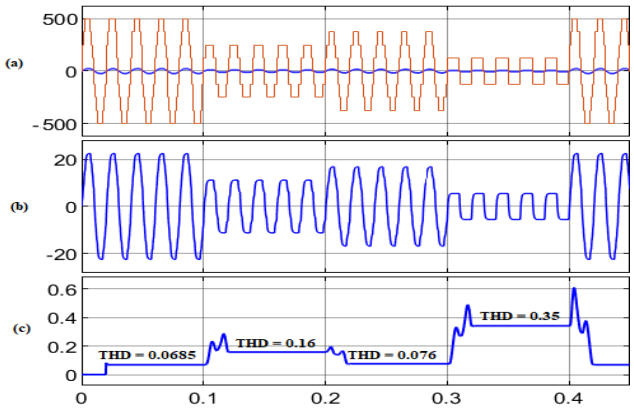

Figure-13. Simulation results (case of a 10kW / 2kVar load, without modulation).

It can be seen from Figure-12 and Figure-13 that the THD obtained varies in a wide range (between 3.3% and 35%) depending on the RMS value of the inverter output voltage and the nature of the load. Indeed, the THD of the absorbed current decreases when the load becomes more inductive. The use of this multi-level inverter without PWM (with the aim of further reducing switching losses and stress of switches) can be interesting in the case of heavily inductive loads and only operating in the regime corresponding to a voltage covering all voltage levels of the inverter.

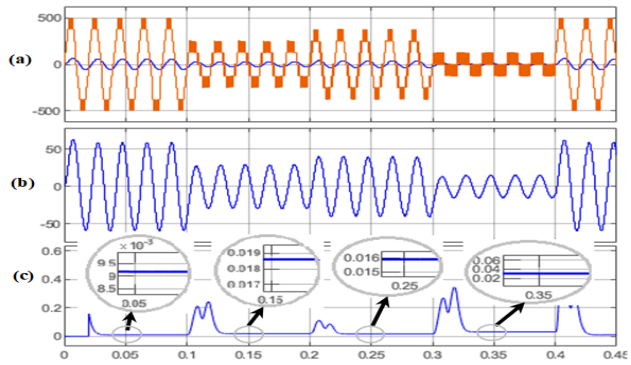

Figure-14. Simulation results (case of a 10kW / 10kVar load, PWM frequency 1 kHz).

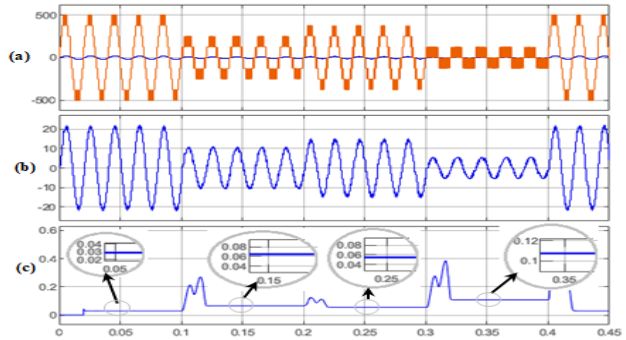

Figure-15. Simulation results (case of a 10kW / 2kVar load, PWM frequency 1 kHz).

Figure-14 and Figure-15 show the improved THD when the PWM frequency is only 1 kHz (frequency considered quite low compared to the frequencies used in conventional inverters [1]). It is between 0.9% and 10% for different loads and different RMS Voltage, compared to the interval 3.3% to 35% in the previous case.

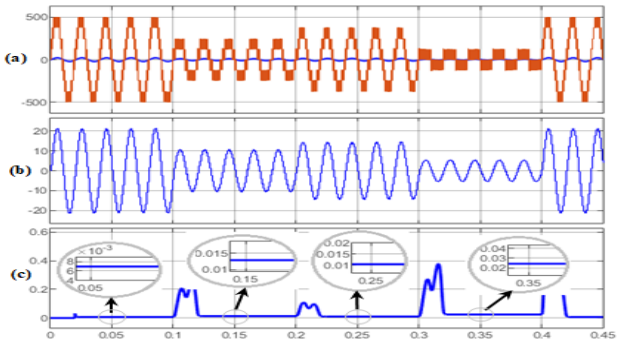

Figure-16. Simulation results (case of a 10kW / 2kVar load, PWM frequency 5 kHz).

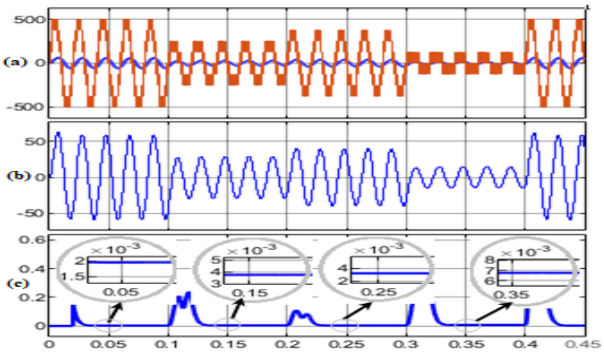

Figure-17. Simulation results (case of a 10kW / 10kVar load, PWM frequency 5 kHz).

It is clear that with a PWM frequency of 5 kHz (according to Figure-16 and Figure-17), the THD of the current absorbed by the load is less than 0.7% for the different inductive loads used for simulation and this is achieved without an output filter, when all the levels of the inverter are used. The advantage of having a low THD of the output current of the inverter is the simplicity of filtering the output voltage with a very modest filter whose capacitance and / or inductance values are considerably reduced.

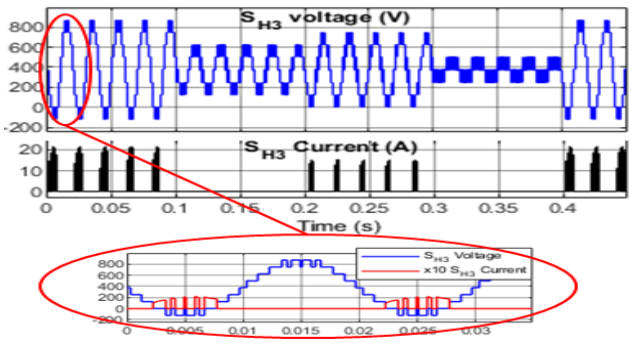

Figure-18. Voltage applied to the switches before and after switching (case of SH3).

The Figure-18 shows the voltages applied to the switch SH3, we notice that all the switching operations are carried out at a voltage of + Vdc or –Vdc, which decreases the constraints on the semiconductors and the switching time, and consequently switching losses.

CONCLUSIONS

In this article, the proposed parallel topology of a multi-level single-phase inverter has been presented. The design of this structure was developed from basic sub-modules. Compared to conventional multi-level inverters, this structure has the following advantages:

- Only requires switches (no additional components such as capacitors;
- The number of switches is reduced (equal to the number of levels required);
- The voltage stresses on the switches are reduced.
- Structure that can be duplicated to construct a three-phase multilevel inverter without adding supplementary voltage sources.

The major disadvantage of this structure is that each switch must hold out twice the voltage of the switched level; but on the other hand, each switch is only solicited for one or two time intervals per period of the fundamental signal. The switches control strategy was developed using a single modulating triangular signal. The proposed scheme makes it possible to control the switches with or without PWM on the one hand, and to vary the RMS value of the output voltage of the inverter. The simulation results, proves the advantages of the proposed topology and the proposed modulation method. Therefore, the proposed multi-level inverter is a suitable solution for applications using photovoltaic panels.

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