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A LOW-POWER 10-BIT 250MS/s BINARY WEIGHTED CURRENT STEERING DAC FOR HIGH SPEED COMMUNICATION SYSTEMS

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ABSTRACT

In this paper, a high-performance low power 10-Bit, 250 MS/s Binary weighted Current steering DAC is presented. With the advent of high performance (in terms of speed, power and area) digital circuits, the need for data converters with high accuracy and speed for various kinds of applications, has attracted the attention of scientists and technologists all over the world. Constant efforts are being put in to miniaturize the data converters from the point of low power and less area. This proposed Digital to Analog Converter (DAC) is designed using 180nm CMOS Technology for High Speed Communication Systems. The architecture follows Binary weighted current steering technique. This technique is used because; it has a high conversion rate and good linearity. The proposed circuit uses binary-weighted current steering architecture rather than segmentation because this structure achieves a high Spurious-Free Dynamic Range (SFDR) at the high clock frequency. Current steering does not require a buffer because it uses a load resistor directly for the current. The Digital to Analog Converter is designed and implemented in0.18µm CMOS process with supply voltage of 1.8v. The power consumption achieved is 19.79µm & Best SFDR(dB)@F_{in}(MHz) is 68@11.23.

Keywords: Op-amp, current steering, binary-weighted, low power digital-analog converter, SFDR, resolution.

1. INTRODUCTION

In most of the electronic systems the input and output signals are analog in nature. Hence there are analog processing devices like amplifiers as input and output devices. However most of the modifications to be carried out on the input signals before obtaining the outputs are carried out in digital domain. Therefore, there is a need to convert the analog input signals into digital signals at the input end, and after processing them in the digital domain; they have to be converted back into analog signals in most of the applications. The circuits that convert analog signals to digital signals are known as A/D Converters and the circuits that convert digital signals to analog signals are called D/A Converters (DACs) [1, 2].

The penetration of electronics into areas like computers, communications, instrumentation and embedded systems such as mobile phones, camcorders, HDTVs has given rise to the need for DACs with stringent requirements. The requirements span over features like high accuracy, linearity, reliability, high speed, low power and so on. There are various approaches adopted to achieve specific characteristics like Power, Speed and accuracy. In General, low power consumption can be reduced by lowering the supply voltage provided to the DAC [3].

Nowadays Digital to Analog converter and analog to digital converter is high in demand for so many applications such as digital TVs, Computer systems, etc. There are many ways to implement digital to analog converters including active and passive components. But, using these types of components consumes large chip size andlarge amounts of power. So, these types of digital to analog converters have not been preferred though they have good linearity. Digital to analog converter is a process of converting digital signal into analog signal. These types of digital converters are used in music players, Tv's, and mobile phones for the conversion of digital data streams into analog audio signals and in televisions and mobile phones to display color images. There are two types of digital to analog converters such as binary weighted resistor type and R-2R type converters. The conversion speed is lower for R-2R DAC when compared to binary weighted type DAC. Binary weighted resistor DAC uses operational amplifier as a summing amplifier and also uses transistors to switch between reference voltage Vref and ground. i.e., high and low terminals. For the data converters, conversion speed should be very fast. When compared to the R-2R DAC the construction and analysis is simple in binary weighted current steering DAC. The current steering DAC architectures help in keeping the load current (i.e. current drawn by the DAC) constant, and in achieving a higher speed of operation the power drawn can be minimized by choosing a low value of current for LSB.

2. Related Work

2.1 DAC Architectures

The block diagram of the digital to analog converter (DAC) is shown in Figure-1, i.e., the input to the digital to analog converter is the binary number and the output of a digital to analog converter is the analog voltage or current signal. The design of an 8-bit 20 GS/s DAC implemented using SiGe technology has also been presented by Haider [15]. This DAC is implemented with a modified segmented current steering architecture where the LSB sub-DAC is implemented with a R-2R ladder. In the design of the binary weighted current steering DAC, a new heterojunction bipolar transistor (HBT) ROM based thermometer decoder architecture has been used.

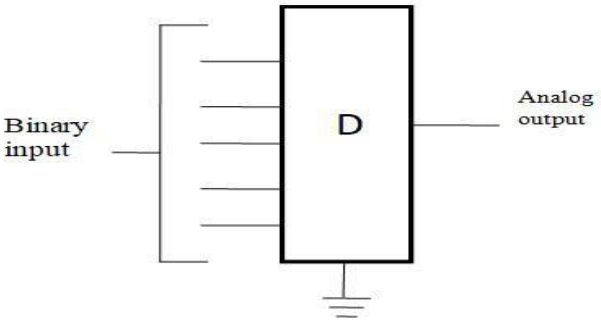

Figure-1. General Block Diagram of DAC.

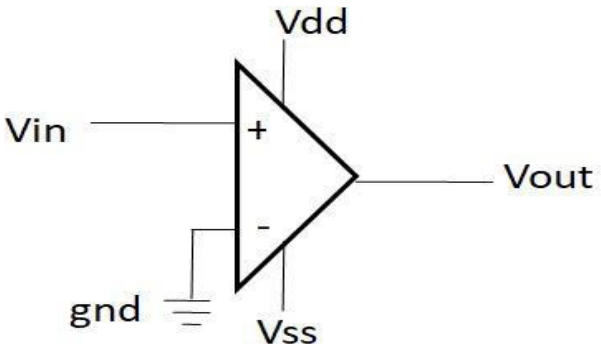

Figure-2. Symbol of Op-amp.

So, the proposed circuit uses Binary Weighted current steering architecture for designing digital to analog converter and to achieve high spurious free dynamic range. Thus, they have the advantage of higher speed and low power consumption. Current steering technique has advantages like high accuracy, high resolution, small chip area and is easily compatible with any CMOS process Technology. The binary-weighted current steering technology offers very high speed when compared to R-2R DAC. So, it is used almost in any field.

2.2 Operational Amplifier (Op-Amp)

The operational amplifier is defined as it a process of amplifying the difference in voltage between two terminals. In Figure-3, the operational amplifier consists of two terminal inputs such as non-inverting terminal input denoted with positive (+) symbol and another one inverting terminal input denoted with negative symbol (-). In the proposed circuit, the input is connected to the non-inverting terminal input. The operational amplifier is used in designing binary weighted current steering digital to analog converter because an op-amp provide low power, high gain and good performance.

2.3. 4-bit Binary Weighted Current Steering DAC

The four-bit digital to analog converter is designed using binary weighted current steering technique with the help of an operational amplifier and one feedback resistor. For this circuit, the current steering technique uses NMOS transistors as shown in Figure-4. Here in this Figure-4, the 4 input bits i.e., D0, D1, D2, D3 are connected to the inverting terminal of an Operational amplifier by connecting all the left side of the NMOS transistors. The right side all the NMOS transistors are connected to the non inverting terminal of an op amp.

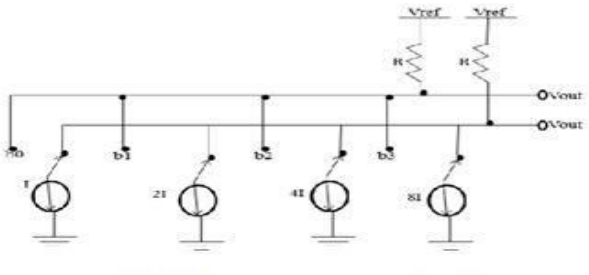

Figure-3. Current steering architecture.

The current steering DAC architectures help in keeping the load current (i.e. current drawn by the DAC) constant, and in achieving a higher speed of operation. The power drawn can be minimized by choosing a low value of current for LSB. The input voltage Vi/p=1V is given to the another NMOS transistor with the current source value idc=0.5µA.The transistor width and length values are considered as width=5µA and length=180nm. The output power was obtained as 11.65µW by using this current steering technique when the supply voltage is considered to be 1.8V.

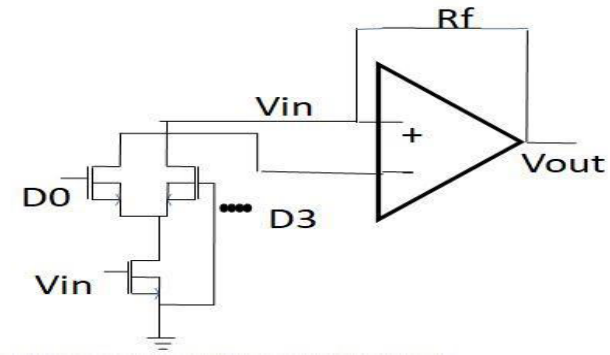

Figure-4. 4-bit binary weighted current steering DAC.

2.4 8-bit Binary Weighted Current Steering DAC

The 8- bit digital to analog converter is designed using binary weighted current steering technique with the help of an operational amplifier and one feedback resistor. For this circuit, the current steering technique uses NMOS transistors as shown in Figure-5. Here in this Fig.5, the 8 input bits i.e., D0, D1,.…D7 is connected to the inverting terminal of an Operational amplifier by connecting all the left side of the NMOS transistors. The right side all the NMOS transistors are connected to the non inverting terminal of an op amp.

The input voltage Vi/p=1V is given to another NMOS transistor with the current source value idc=1µA. The output power was obtained as 12.54µW by using this

current steering technique when the supply voltage is considered to be 1.8V.

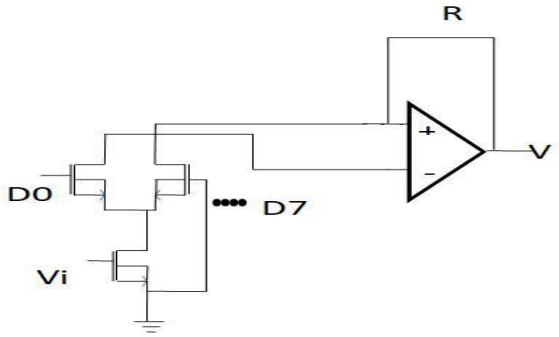

Figure-5. 8-bit Binary Weighted Current Steering DAC.

3. Proposed10-bit Binary Weighted Current Steering DAC Architecture

The 10-bit digital to analog converter is designed using binary weighted current steering technique with the help of an operational amplifier and one feedback resistor. For this circuit, the current steering technique uses NMOS transistors as shown in Figure-6. Here in Figure-6, the 10 input bits i.e., D0, D1,..…D9 are connected to the inverting terminal of an Operational amplifier by connecting all the left side of the NMOS transistors. The right side all the NMOS transistors are connected to the non inverting terminal of an op amp. The input voltage Vi/p=1V is given to another NMOS transistor with the current source value i_{dc}=5µA. The output power was obtained as 19.79µW by using this current steering technique when the supply voltage is considered to be 1.8V.

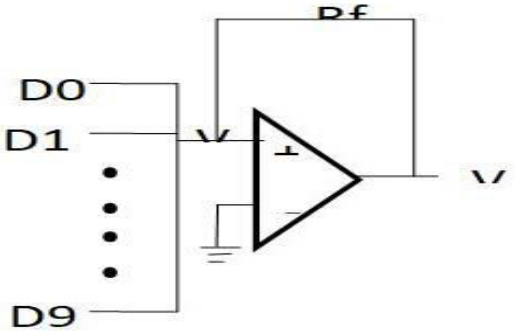

Figure-6. Block diagram of 10-bit binary weighted current steering DAC.

In Figure-6, the proposed circuit is designed by using operational amplifier. For the two stages operational amplifier the gain is observed to be 81.07dB. In the circuit, the inputs i.e. D0, D1,…..D9 are given to the op-amp and the feedback resistance used in the circuit is to minimize the power consumption. The proposed circuit was designed with the current steering technique with current source value given as idc=5µA is observed to optimize power consumption.

The proposed circuit is operated with the help of an operational amplifier and with the binary weighted current steering digital to analog converter technique with the less power consumption.

The operational amplifier obtained the gain of 81.07dB. The 10 bits i.e., D0, D1 …D9 with the input voltage Vin is given to the operational amplifier by using current steering technique. The feedback resistance R_f is given from the output to the positive terminal of an op-amp. In this proposed circuit, the two stage operational amplifier is used as a summing amplifier which gives a weighted sum of the binary input based onthe reference voltage denoted as V_{ref}. For the four bit digital to analog converter, the relationship between the output voltage Vout and the given binary input is calculated by using the formula as,

$$V_{out} = -V_{ref}.\frac{R_f}{R}\left[\frac{d1}{2^1}+\frac{d2}{2^2}+ - - - - - +\frac{dn}{2^n}\right]\ldots\ldots \quad [1]$$

In the Equation [1], the negative sign in the analog output is due to the connection of a summing amplifier which inverts the polarity i.e., when the analog output is connected to the summing amplifier it takes the input as positive, as it inverted the polarity from Negative to Positive.

An n-bit DAC is calculated by using the formula as,

$$V_{out} = -V_{ref}\frac{R_f}{R}\sum_{i=1}^{n}\frac{ai}{2^i} \ldots\ldots\ldots \quad [2]$$

The parameters for the proposed circuit were analyzed using current steering technique. For the 10-bit binary weighted current steering DAC the power value is obtained as 19.79µWwhen the supply voltage is given as 1.8V and the current source value is given as idc=5µA. For the 8 bit binary weighted current steering DAC the power value is obtained 12.54µW when the supply voltage is given as 1.8V and the current source value is given as idc =1µA. For the 4-bit binary weighted current steering DAC the power value was obtained as 11.65µW when the supply voltage value is given as 1.8V and the current source value is given as idc=0.5µA.

4. RESULTS AND DISCUSSIONS

The simulated result for the 10-bit binary weighted current steering DAC is shown in Figure-7. The simulated waveform consists of 10 bit inputs. The output is verified by doing the theoretical calculations for the input bits. The output voltage value is obtained as 1.8_V when the input voltage is given as 0 to 2.5V. For example, In 8-bit DAC, when the input is considered as 1100 1100, the theoretical output is 0.79V where the simulated output obtained is 0.8V.

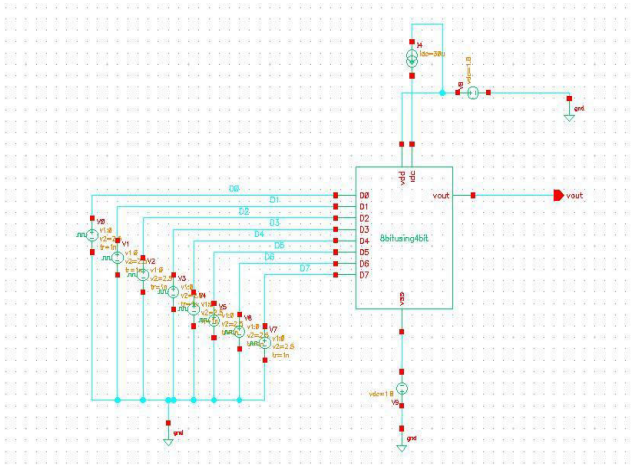

Figure-7. Schematic of 8-bit binary weighted current steering DAC.

Figure-8. Waveforms for the 8-bit binary weighted current steering DAC.

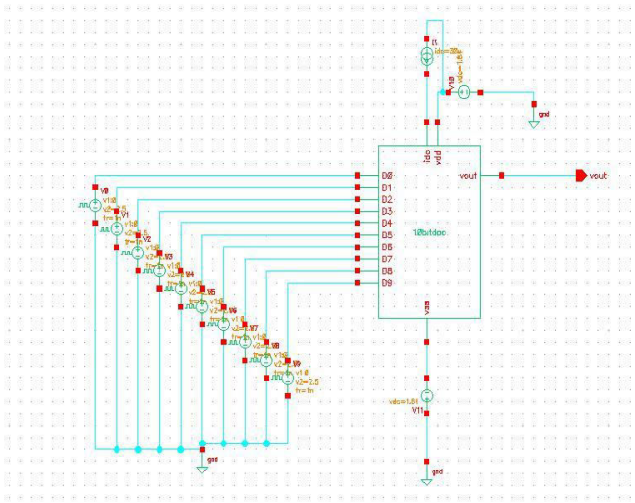

Figure-9. Schematic of 10-bit binary weighted current steering DAC.

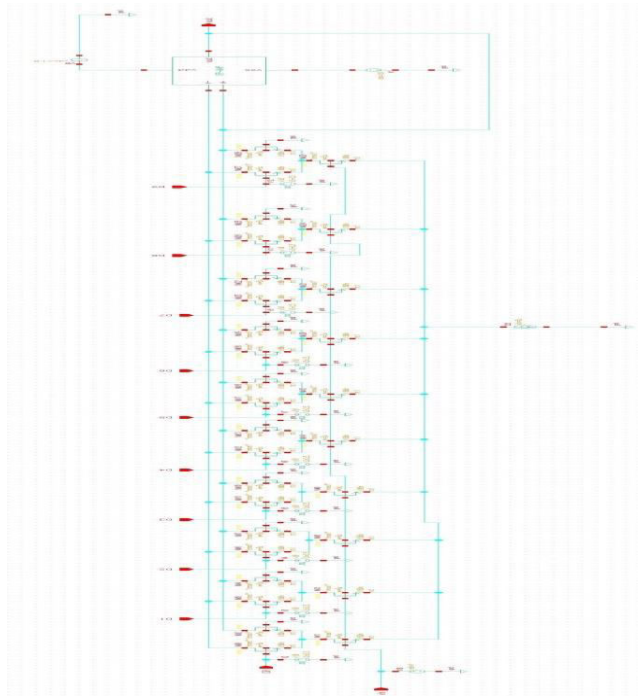

Figure-10. Schematic of 10-bit binary weighted current steering DAC.

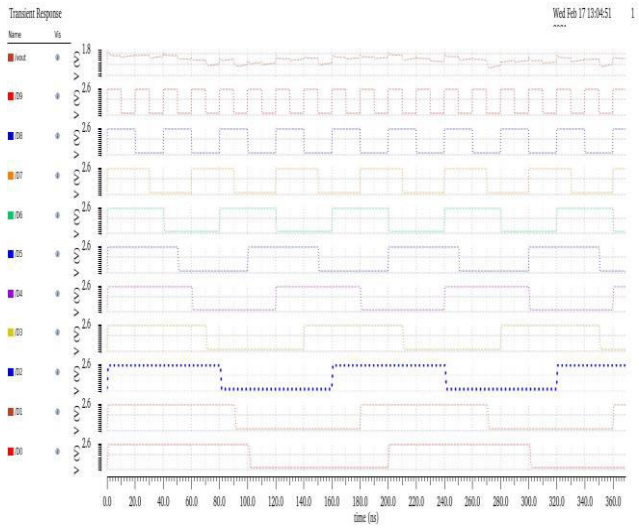

Figure-11. Waveforms for the 10-bit binary weighted current steering DAC.

In this, the 10 bit binary weighted current steering DAC is designed using 180nm technology. Here the result is compared with the binary weighted resistor DAC. The operating voltage is given as 1.8V for both the technologies. In this work, the output is calculated by using binary weighted current steering technique. The obtained result is compared with the weighted resistor DAC. The weighted resistor DAC is designed using an operational amplifier and one feedback resistor. The circuit of weighted resistor DAC is designed with the help of two4 bit DACs and one 2 bit DAC. The power obtained in 10 bit DAC is 150.9µW using binary weighted resistor DAC and the power value is obtained as19.79µW using

binary weighted current steering DAC. Hence, the power consumption obtained is less in binary weighted current steering DAC when compared with the binary weighted resistor DAC.

Table-1. Desired specifications.

Parameter	Specifications
Technology	180nm
Operating voltage	1.8V
Resolution	10bit
Technique	Binary weighted current steering
Power consumption	≤20µW
SFDR	>60dB
Gain	≥70dB

Table-2. Comparison of this work with other works.

Parameters	Binary weighted Resistor DAC	Binary Weighted Current Steering DAC
Resolution(bits)	10	10
Supply Voltage (V)	1.8V	1.8V
DNL/INL(LSB)	0.48/0.38	0.25/0.19
Best SFDR(dB)@f_{in}(MHZ)	45@5	68@11.23
Power Consumption(µWatts)	150.9	19.79
Technology(µm)	0.18	0.18
Chip Area(mm)	2.8	2.44
FOM(x109)	1,712	11,636

5. CONCLUSIONS

In this paper, 10-bit Digital to Analog converter is designed by using Binary Weighted current steering technique. The power consumption in 10-bit Binary weighted current steering DAC was observed to be 19.79µW and in 8-bit, it was observed to be 12.54µWand in 4-bit, it was observed to be 11.65µW. Even though 4-bit was observed to be consuming less power, 10-bit operation is chosen in this design in order to obtain high resolution and SFDR because when the SFDR is high, the power consumption will be less. Here the proposed work is compared with the binary weighted resistor DAC in order to observe less power consumption and best SFDR. Hence the proposed circuit is used in the applications of data converters because of high speed and less power consumption. Further, the obtained parameters can be improved for better performance by increasing the higher order designs.

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