VOL. 17, NO. 3, FEBRUARY 2022 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

# AN ULTRA-LOW POWER TUNNEL FET BASED OTA DESIGN FOR NEURAL AMPLIFIER

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**ABSTRACT**

Tremendous research is going on in healthcare and monitoring systems to develop the quality of Bio-signal Acquisition systems. Analog front end bio-amplifier circuit is a crucial part of the system used to amplify the desired bio-signal in a suitable low-frequency range by consuming some amount of power. It is very challenging to design a high gain operational transconductance amplifier (OTA) with ultra-low power consumption for wearable and implantable devices due to the limit of heat dissipation for protecting the tissues. Hence, this work proposes a Tunnel FET (TFET) device for designing a two-stage OTA because MOSFETs have a sub-threshold swing (SS) limitation of 60 mV/decade. TFET has the advantage of distinctive steep slope characteristics with SS value of less than 60 mV/decade. It provides a high ON-drive current and makes the OTA performance more energy-efficient, especially in ultra-low power and low voltage applications. The TFET based OTA with RC feedback network for the neural amplifier is proposed. The cadence spectre simulated results show a closed-loop gain of 44 dB in the frequency range of 1 Hz to 2.5 kHz with a low power consumption of 3.6 nW with 0.45 V supply voltage.

**Keywords:** tunnel FET (TFET), analog front end (AFE), neural amplifier, ultra-low power.

## INTRODUCTION

A wearable bio-signal acquisition system has attained great potential to monitor the patients' health data and diagnose the diseases earlier. The overall block diagram of the Bio-signal acquisition system is shown in Figure-1. The analog front end (AFE) is the crucial element in consuming the power and is integrated in most wearable wireless sensor systems. It consists of a multi-channel electrode array along with operational tranconductance amplifier (OTA) circuit. The amplifier in the acquisition system must amplify the bio-signals having an amplitude of microvolts in a particular low-frequency range [1], [2]. For example, widely measured bio-signals amplitude and frequency range are mentioned in Table 1. The other elements are Analog to Digital converters and Digital processors are available next to the amplifier circuit for signal processing purpose.

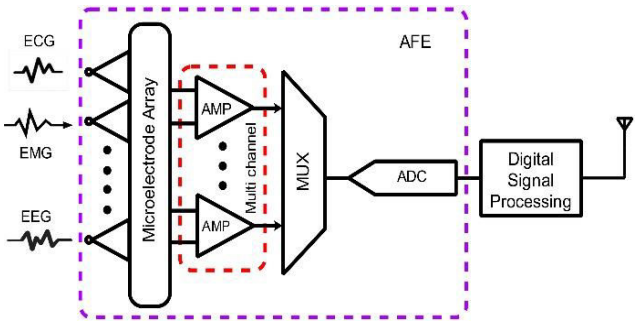


**Figure-1.** Overall block diagram of bio-signal acquisition system.

OTA is the vital building block in most analog circuits. It is an active element and plays a dominant role in implementing analog filters, ADC, DAC, oscillators, sample & hold circuits and amplifiers. Nowadays, op-amp applications are replaced by OTA because of frequency limit [1], [3]. OTA is an amplifier whose differential input voltage is converted into output current, and it is said to be a voltage-controlled current source. Ultra-low-voltage OTA designs with low power consumption are in high demand for most analog circuits to reduce the battery size and weight and increase the battery life [4], [5]. Moreover, in modern, portable and bio-implantable applications, it is necessary the OTA analog circuit to operate in low voltage to prevent the damage of body tissues [1], [2], [6]. Generally, CMOS-based OTA structures operated in weak inversion region are preferred since it provides high transconductance under bias current ($g_m/I_d$) ratio which is nothing but a measure of transconductance generation efficiency [7]-[9].

**Table-1.** Bio-signals amplitude and frequency range [6].

| Bio-Signals | Frequency Range | Amplitude in volts |
|---|---|---|
| Electroencephalographic (EEG) | 0.4 to 40 Hz | 10-20 µV |
| Electro corticographic (EcoG) | 0.5 to 200 Hz | <100 µV |
| ECG sensor | < 1KHZ | 100 µV |
| Neural Spikes | 100 Hz to 7 KHz | 500 µV |
| Local Field Potential (LFP) | < 1Hz | <5 mV |

It will restrict the generation of transconductance $g_m$ per low bias drain current, creating performance issues and the power dissipation becomes not optimal. As the bio-signals amplitude are very weak, it is necessary that analog front end amplifier circuit should have high gain, band width, good linearity with reasonable output voltage swing to enhance the sensitivity of the acquisition system.

Hence there is a significant challenge in designing the OTA to achieve the above performance requirements under the condition of low supply voltage with less power consumption [6], [8]. It is greatly demand that the device used in OTA circuit should have higher value of $g_m/I_d$ to achieve it. In this paper, Tunnel FET (TFET) device based OTA is proposed because it has the advantage of SS of less than 60 mV/decade due to very steep slope characteristics, less leakage, low turn-on voltage and achieve higher $g_m/I_d$ value of more than 100 $V^{-1}$ especially in ultra-low power and low voltage applications [10], [12], [22], [23]. Therefore a 450 mV supply voltage is fixed in the circuit design without affecting the performance of the whole system is adapted. The paper is organized as follows. The section 2 reviews the CMOS based OTA technique and its challenges. The section 3 describes the TFET technology, advantages, modeling and its electrical characteristics. The section 4 shows the design of TFET based two stage OTA and the proposed neural amplifier design. The performance of the output is analyzed through simulation which is discussed in the section 5. Finally, the conclusion is made.

## REVIEW AND CHALLENGES OF CMOS BASED OTA

Typically instrumentation amplifier is widely used in most of Bio-signal processing circuits because it provides good gain and high input impedance circuits. However, it is not suitable for wearable and implantable device systems because the circuit components involved are more bulky, which consumes a huge amount of power [11]. Later Gate driven MOS topology are used to design the OTA but it is not appropriate for low voltage circuits (< 0.5V) because it requires a minimum rail to rail supply of 1.8v for saturation and output voltage swing purposes [7], [21]. To maintain a sensible output voltage swing, the threshold voltage of MOSFET can be minimized but it does not follow the constant electric field scaling. To compensate for the issues related to threshold voltage reduction, later in number of papers [7–9], bulk–driven input stage circuits are preferred, eliminating the requirement of threshold voltage from signal path. However, in bulk driven technique, the performance of OTA was very poor and affects the parameters like dc gain, GBW, slew rate and input referred noise [8]. This is due to the small value of transconductance ($g_{mb}$) obtained in the weak inversion region compare to strong inversion region. The ratio of bulk driven and gate driven transconductance is given by body transconductance effect Ƞ as:

$$\eta = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2\varphi_F + V_{BS}}} \quad (1)$$

Normally the body transconductance effect Ƞ value will be in the range of 0.2 to 0.4 which shows clearly the $g_{mb}$ is very low compared to $g_m$. Where $V_{BS}$ is the bulk to source voltage, $\gamma$ and $\varphi_F$ are process specific parameters. Recently, there are number of techniques are proposed to enhance the bulk driven transconductances such as positive feedback [13], current-shunt technique [14] & double recycling techniques. Despite improving the transconductance of OTA, the stability problems arise due to phase margin degradation, process variations, & device mismatching. In many applications, it is require improving the linearity of OTA which is determined by the analog input stage of the system. The linearity improvement techniques such as source degeneration, adaptive biasing, cross coupling are briefly reviewed in paper [15]. Instead of doing the circuit level approach to improve the transconductance ($g_m$) of the circuit at low power environment, device level approach is preferred recently [12]. Hence in summary, the CMOS based OTA in ultra-low power operation is facing a problem of restriction in improving the transconductance ($g_m$) under weak inversion or subthreshold region which made the circuit becomes energy inefficient due to the limitation SS of 60 mV/decade.

## TUNNEL FET TECHNOLOGY

TFET is a suitable post-Si-CMOS device specially developed for ultra-low power applications. It has a unique characteristic of sub-threshold swing (SS) value of less than 60 mV/decade, which results in operating at very low turn-on voltage and achieving high on-drive current [12].

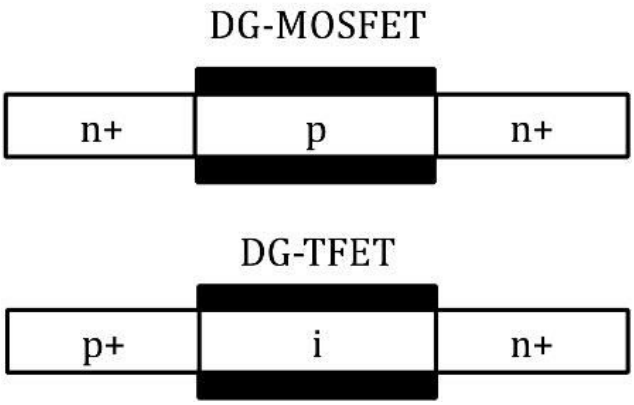


**Figure-2(a).** Structure of double gate n-channel MOSFET and n-channel TFET.

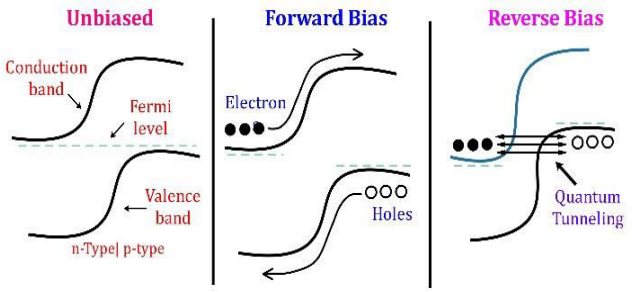


**Figure-2(b).** Current conduction of TFET in three biasing conditions: Unbiased and forward bias no current conduction. In reverse bias, band to band tunneling taken place.

In structure wise, it is similar to MOSFET as shown in Figure 2(a), where N-TFET consists of P+, I, N+ doped region are acted as source, channel & drain but its operations are totally different. Normally in MOSFET, the current conduction mechanism taken place from source to drain which is due to the thermionic emission of electrons. Compare to MOSFET, in N-TFET operates on reverse bias in which current conduction mechanism is due to band to band tunneling as shown in Figure-2(b) where valence band electrons in source is transferred to conduction band of drain [10]. Similarly, in P-TFET the holes present in the valence band of source will transfer to conduction band of drain.

**Tunnel FET Verilog a Model**

The tunneling probability of electrons in the source -channel TFET junction is given by kane-sze as

$$T(b2b) = \exp\left(\frac{-4\sqrt{2m^{*}E_g^3}}{3qh\delta}\right) \quad (2)$$

Where $m^{*}$ and $E_g$ is the relative mass and energy band gap of the material. δ is the tunnel junction electric field. q is the charge of electron and h is Planck's constant. At low voltage condition, hetero-band structure with very low value of band gap ($E_g$) and relative mass materials (e.g. III-V, Ge etc.) are chosen to improve the tunneling probability. To obtain the benefits of TFET in the design of low power circuits, a compact model of TFET is required. Look up table based verilog A model for III-V tunnel FET was developed in [16] and its characteristics were plotted in TCAD simulation due to band to band tunneling of current. Similarly based on the Kane-Sze tunneling formula above, an universal analytic SPICE model was also developed and implemented in simulator using verilog A [17]. The modeling parameters are also specified. In this work, GaN/InN universal hetero-junction TFET verilog A model is implemented in cadence spectre simulator and its simulated electrical characteristics of N-type GaN/InN TFET are shown in Figures 3(a), 3(b) and 3(c).

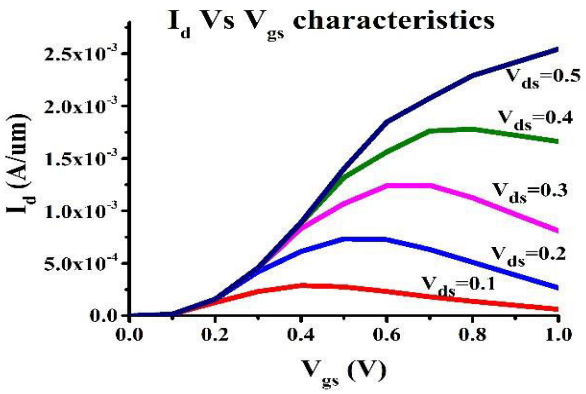


**Figure-3(a).** GaN/InN TFET drain current ($I_d$) versus gate to source voltage ($V_{gs}$) characteristics.

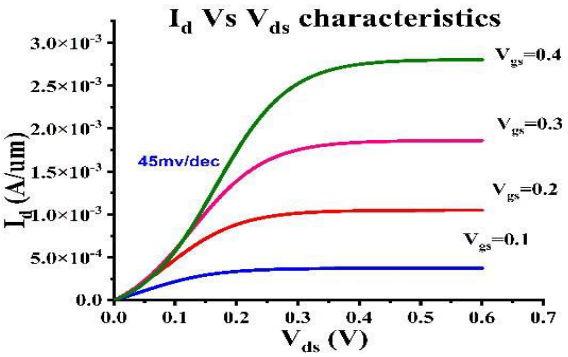


**Figure-3(b).** GaN/InN TFET drain current ($I_d$) versus drain to source voltage ($V_{ds}$).

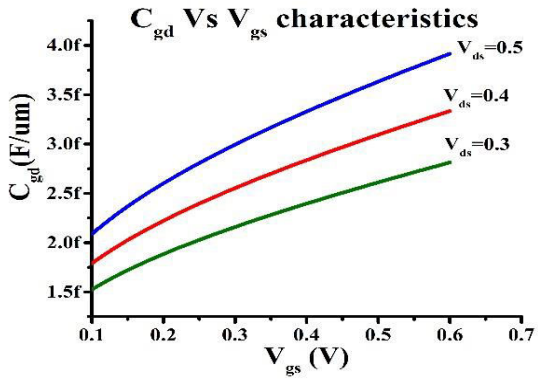


**Figure-3(c).** GaN/InN TFET capacitance ($C_{gd}$) versus gate to source voltage ($V_{gs}$) characteristics.

**Tunnel FET Advantages**

In the conventional technique, the designing of analog circuits is followed by square law which cannot provide the accurate results since the short channel effects are not considered. $G_m/I_d$ is one of the design technique in which advanced and accurate model of the transistors are used where the short channel effects are taken in to account. The power consumption of the transistor is a key factor to be considered especially while it is working in subthreshold region. The performance of the MOS transistor under subthreshold region is determined by a parameter "Transconductance to Drain Current Ratio ($g_m/I_d$)" which is a quantity of net transconductance generation efficiency under very low voltage of operation. In fact, the performances ($g_m$) will be very poor under lower drain current in subthreshold region but it is not a rigorous requirement in biomedical applications where the power dissipation should be optimal. The relationship between the Subthreshold Swing (SS) and ($g_m/I_d$) are given as:

$$\frac{1}{SS} = \frac{\Delta log_{10} I_{DS}}{\Delta V_{GS}} = \frac{1}{\log(10)} \frac{\partial \log(I_{DS})}{\partial V_{GS}} = \frac{1}{\log(10)} \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}} \quad (3)$$

$$\frac{g_m}{I_{DS}} = \frac{log(10)}{SS} \quad (4)$$

The traditional MOSFET has a limitation of SS of 60 mV/decade at room temperature and achieved the $g_m/I_d$ value of 38.5 $V^{-1}$ as per the relation above. But TFET is a promising device particularly operating in low power, high frequency and ultra-low voltage of operation having the SS value of less than 60 mV/dec. This is due to the inherent properties of inter-band tunneling mechanism is occurred between source and channel of TFET. By having a lesser SS, the TFET enhances higher transconductance and $g_m/I_d$ value achieved to be more than 100 $V^{-1}$ as shown in Figures 4(a) and 4(b). In summary, TFET has many advantages in low power Bio medical application such as less leakage current, SS of less than 60 mV/dec, Band to Band tunneling, high operating speed, effective ON/OFF current control and impervious to short channel effects.

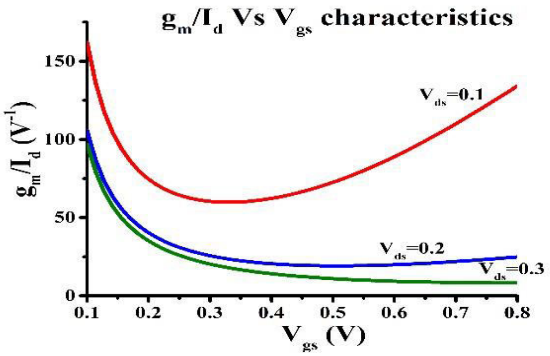


**Figure-4(a).** GaN/InN-TFET-$g_m/I_d$ versus gate to source voltage ($V_{gs}$) characteristics.

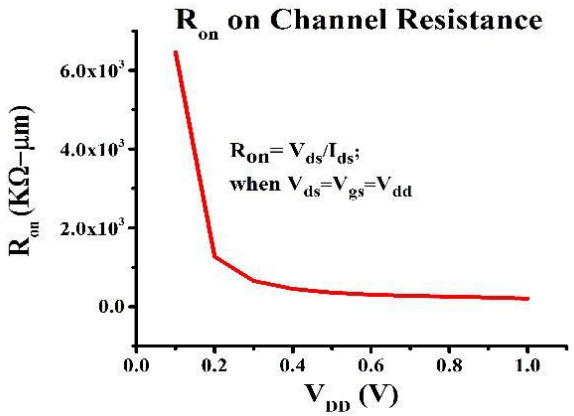


**Figure-4(b).** GaN/InN TFET –ON state channel resistance.

## TUNNEL FET BASED TWO STAGE OTA DESIGN

There are number of OTA architectures namely Telescopic Cascode, Folded Cascode, Two stage and single stage OTA. The very easy one to implement is single stage OTA but it provides low gain since it has low output impedance of architecture. To enhance the DC gain of the amplifier, cascading or adding the number of stages at the output which makes the impedance higher to improve the gain. In Telescopic architecture, number of transistors are stacked on top each other to obtain a high gain output but it produces a very less output voltage swing. Folded cascade also have good architecture for improving voltage swing and gain but it consumes more power. In this work, two stage architecture is proposed which is shown in Figure-5. It is similar configuration to op-amp and consists of two stages. The first stage is made of TFETs T1, T2 & T7 which operates as a differential amplifier with current mirror load of T3 & T4. The transistors T5 & T6 act as a common source amplifier in the second stage. The transistor T8 is used for biasing the current mirrors T8-T7 and T8-T6. A miller capacitance Cc is used to enhance the stability of the circuit. Linearity of OTA is nothing but the output current must be linear in relation with the differential input voltage. It is possible only when the transconductance gm of the TFET should be constant with various input voltage range, in this work cross coupling of TFET is chosen to improve the linearity of OTA. The length and width of TFETs are shown in Table-2.

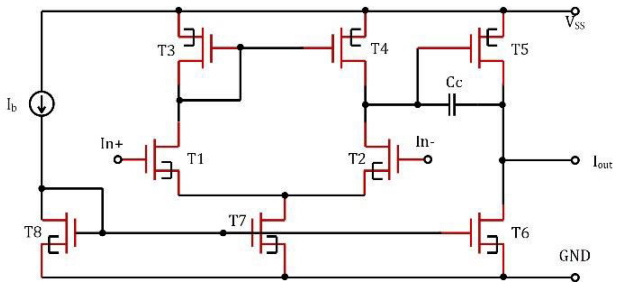


**Figure-5.** Circuit diagram of tunnel FET based two stage OTA with specifications.

**Table-2.** TFET dimensions used in the circuit.

| TFET | Length/Width |
|---|---|
| T1,T2 | 20n/1u |
| T3,T4 | 20n/8u |
| T5 | 20n/5u |
| T6 | 20n/0.5u |
| T7, T8 | 20n/0.7u |
| Vss | 0.45V |
| $I_b$ | 8nA |

### Neural Amplifier Design using Tunnel FET based OTA

The Figure-6 shows Hetero-junction TFET based neural amplifier in which OTA with closed loop topology connection is implemented through capacitive feedback network ($C_1$ $C_2$) and pseudo resistors ($R_p$) [18-20]. The pseudo resistors ($R_p$) are generated by connecting the gate and source of P-TFET and attained a high resistance value of $10^{12}$ Ω. Due to the limited space requirements of capacitance ($C_2$) in the chip implantation, highly resistive pseudo resistors are chosen to provide a large time

constant ($R_pC_2$). It enables the amplifier to operates in lower cut off frequency ($F_L$= $1/2\pi$ $R_pC_2$) and designed to reject or minimize the flicker noise which is set by the value ($1/ R_pC_2$). The mid band gain or voltage gain of the neural amplifier $A_{M\ is}$ set by the parameter ($C_1$ /$C_2$). The higher cut off frequency equation is given by ($F_H$= $G_{OTA}/2\pi$ $A_MC_L$) where $G_{OTA}$ is the gain of the OTA.

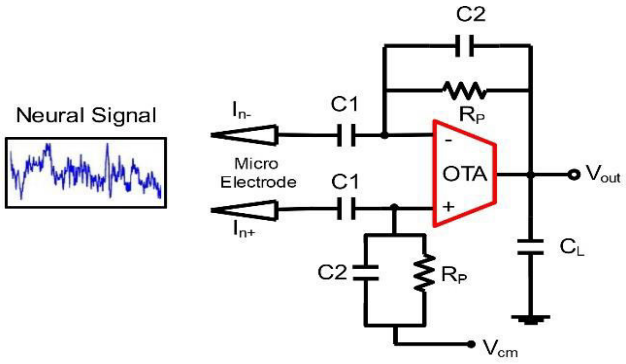


**Figure-6.** Tunnel FET based neural amplifier.

## RESULTS AND DISCUSSIONS

### AC Analysis

To analyze the performance of the proposed TFET based OTA design, an ac analysis is performed through simulation. A frequency response analyze of 1 Hz to 10 MHz is chosen, with an input supply voltage of 0.45 V and 8 nA as a bias current. The TFET width and length values are mentioned in the previous session. An ac magnitude of 1mv is given in one of the OTA input terminal which signal requires to be amplified. The OTA provides an open loop gain of 49dB with phase angle in the frequency range from 1Hz to 5 KHZ is obtained which is shown in the Figure-7(a). A capacitor of 1pf is chosen at the load side. The ac response of amplified output voltage is plotted in the Figure-7(b). Mostly the respond of our proposed OTA are covering in the lower frequency range which falls in the operation of bio-signals as specified. The closed loop OTA of neural amplifier is also analyzed through ac analysis.

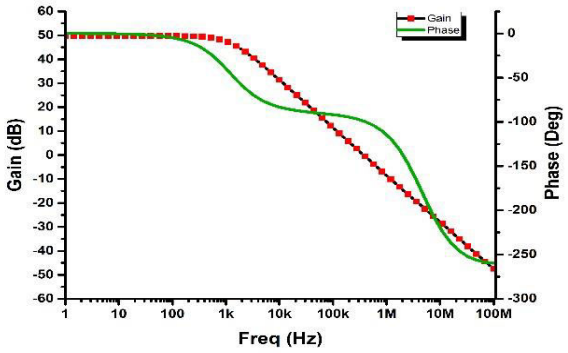


**Figure-7(a).** Gain and phase curve of proposed open loop TFET based OTA.

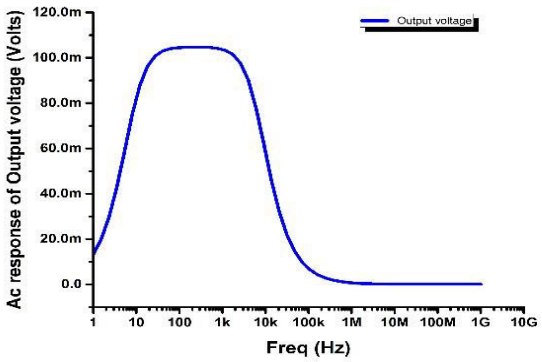


**Figure-7(b).** AC response of amplified output voltage of proposed OTA.

An ac magnitude of 1mV is given in one of the OTA input terminal which signal requires to be amplified. The OTA provides an open loop gain of 49 dB with phase angle in the frequency range from 1 Hz to 5 KHZ is obtained which is shown in the Figure-7(a). A capacitor of 1pf is chosen at the load side. The ac response of amplified output voltage is plotted in the Figure-7(b). Mostly the respond of our proposed OTA are covering in the lower frequency range which falls in the operation of bio-signals as specified. The closed loop OTA of neural amplifier is also analyzed through ac analysis.

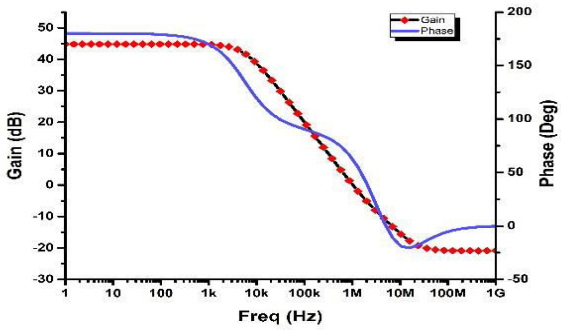


**Figure-8(a).** Gain and phase curve of proposed TFET based neural amplifier.

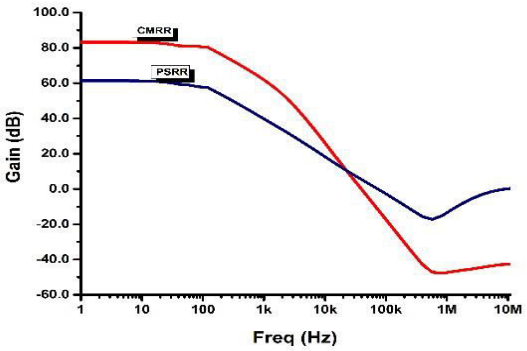


**Figure-8(b).** CMRR and PSRR value of proposed TFET based neural amplifier.

The proposed neural amplifier achieves a gain of 44 db with phase angle in the frequency range from 1Hz to 2.5 KHz, shown in Figure-8(a). A common mode voltage $V_{cm}$ of certain voltage is required in the circuit to do the offset operation. It can be obtained from the supply voltage through resistive network. If we increase the bias current, the gain and phase of the neural amplifier observes to be improving due to the increase in tunnel fet flow of current conduction, however the total power consumption of the amplifier will increase. Due to the power consumption restriction in Bio-medical applications, our proposed circuit is limited to 3.6 nW of power consumption with improved results.

Similarly, the size of the TFET width is chosen to be optimal with good results. Otherwise, the circuit becomes bulky. Here we have used the two-stage OTA design, and if we increase the number of stages for better gain results, the circuit size will become higher. It will lead to the requirement of bias current to be more for making the device active and consumes more power. The CMRR and PSRR values are calculated for the proposed neural amplifier and the curves are shown in the Figure-8(b).

**Transient Analysis**

To perform a transient analysis, a sinewave of 2 mV of peak to peak differential input voltage is applied at the OTA's input terminal as shown in Figures 9(a) & 9(b). Transient analysis output of 1ms is plotted, showing a remarkable output voltage swing of 110 mV with 3.5 nA of peak to peak current. This results due to the performance of the TFET in the lower sub-threshold region of operation at ultra-low power. However, it is observed that output voltage is linear in the frequency range from 1 Hz to 2.5 KHz; further increase in frequency, the output voltage swing is distorted and will not be linear. The proposed design of TFET based neural amplifier exhibits that at a lower kHz frequency range of less than 2.5 kHz, it achieves a maximum gain of 44 dB and operates at sub-nW power of consumption. The benefits of high gain occur in HTFET based neural amplifiers due to the enhanced gm/Id value factor. This arises from high steep slope characteristics of GaN/InN TFET device which develops a high transconductance. Further, the designed circuit has been less sensitive to temperature variation and increased output resistance, which is an additional benefit. It also provides an enhanced results of both CMRR and PSRR value of 83 dB and 61 dB. The above good performance characteristics of the proposed design achieve an input referred noise of 12.1 µVrms at the same bias current of 8 nA, which is acceptable for biosensor applications. Although the OTA architecture used in this design is a simple two-stage circuit, because of the excellent characteristics of GaN/InN HTFET, it consumes extremely low power of 3.6 nW with a better performance index.The sub nW power consumption of main results in this work shows a high possibility for ultra low power analog circuit and sensors applications.

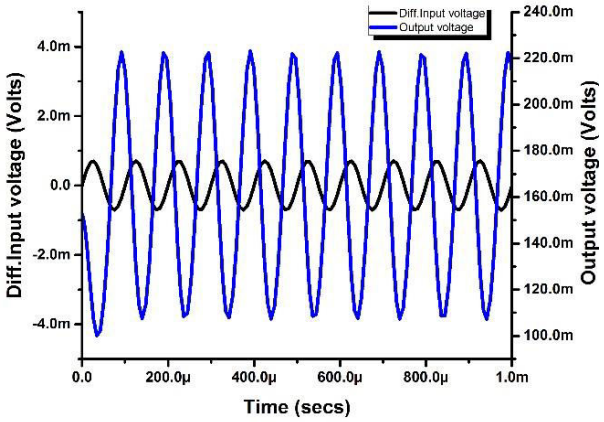


**Figure-9(a).** Transient output voltage of proposed OTA.

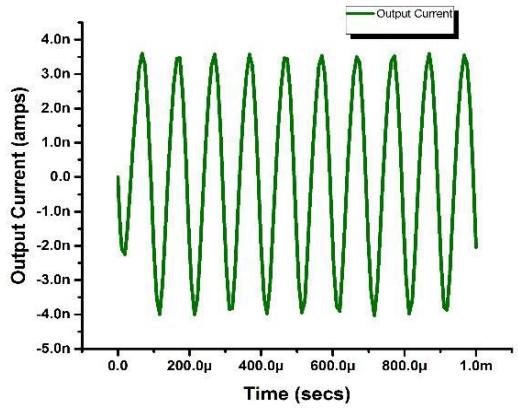


**Figure-9(b).** Transient output current of proposed OTA.

It is observed that the designed neural amplifer has shown a tradeoff between the power and noise. By degrading the power performance, it is possible to reduce the noise level of neural amplifier. It means that the input referred noise level can be further reduced by increasing the power consumption. It can be accomplished by increasing the bias current of the circuit. The performance metrics of HTFET neural amplifier at $C_L$ = 1 pF and $I_{bias}$ = 8nA are summarized in Table-3. In case of low frequency designs with TFET, the flicker noise characteristics is paramount. The flicker noise drops with inversely proportional to the $1/f^2$ pattern. The effect of flicker noise can be diminished by including a high pass filter at lower frequencies or by increasing the gate area of the design. The other noises such as shot noise and thermal noise have not received much attention in HTFET as per the previous studies. The great outcome of high gain with ultra-low power consumption of this amplifier is deserved for wearable sensor medical devices that attain a high significance in the health industry. The summary of previous research work results are tabulated in Table-3.

**Table-3.** Summary of previous research works.

| Parameters | Huichu Liu. *et al* [6] | Trivedi *et al* [9] | Pratyusha *et al* [1] | This work |
|---|---|---|---|---|
| Technology | 20 nm HTFET | 90 nm Vertical Channel TFET | 180 nm CMOS | 20 nm HTFET |
| Supply Voltage | 0.5 V | 1 V | 1.8 V | 0.45 V |
| Bias Current | 10 nA | ~3nA | 3.4 µA | 8 nA |
| Power | 5 nW | 3.6 nW | 6.25µW | 3.6 nW |
| Closed Loop Gain | 39.4 dB | 27.7 dB | 45.38 dB | 44 dB |
| Bandwidth | 12Hz – 2.1 KHz | 36mHz -3.2KHz | 5Hz – 2.92 KHz | 1 Hz to 2.5 KHz |
| CMRR | 56 dB | 64 dB | - | 83 dB |
| PSRR | 70 dB | 55 dB | - | 61 dB |
| OTA Architecture | Telescopic | Folded Cascode | Cascode | Two stage |

## CONCLUSIONS

Due to the limitation of SS of 60 mV/decade, CMOS-based OTA faces challenges in improving its transconductance ($g_m$) under weak inversion or subthreshold region, which results in the whole circuit becoming energy inefficient. Hetero-junction TFET is proposed in this paper to design OTA. It has unique steep slope characteristics. SS of less than 60 mv/dec with high $g_m/I_d$ value makes it a promising candidate for ultra low power analog circuits & wireless sensor applications. A GaN/InN TFET based neural amplifier that employs a two-stage OTA has been proposed to enable a 3.6 nW power consumption. A highly trimmed bias current of 8 nA and supply voltage of 0.45 V provides a mid-band gain of 44 dB & bandwidth from 1 Hz to 2.5 kHz with excellent output voltage swing. This study found that TFET has superior performance compared to CMOS in the design of OTA for ultra-low power Bio-signal acquisition system. In the future, our research focus is to reduce the noise of TFET based neural amplifiers before it implements in an integrated layout.

## ACKNOWLEDGEMENTS

The authors would like to thanks the research management center of AIMST University for funding the open access charge for this manuscript publication.

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