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A DIGITALLY CONTROLLED OSCILLATOR FOR ADPLL USING COMBINATIONAL FREQUENCY MULTIPLIER AND NOVEL VARIABLE DELAY INVERTER

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ABSTRACT

In this article, a novel digitally controlled Oscillator (DCO) for All Digital Phase Locked Loop (ADPLL) is presented. In the proposed DCO, the concept of a combinational frequency multiplier is used to double the frequency range of a conventional digital ring oscillator. However, conventional combinational frequency multiplier circuits can produce a 50% duty cycle only for a single input frequency. Hence, a novel circuit for frequency multiplication is proposed that can produce an output frequency equal to 2 times the input frequencies with a 50% duty cycle for all the frequencies. The proposed DCO is developed by integrating a digitally controlled ring oscillator with the proposed novel combinational multiplier. Digitally controlled delay inverters are used to design both the DCRO and the novel combinational frequency multiplier. A 5-bit DCO is realized using a 4-bit DCRO and the proposed combinational frequency multiplier in 90nm CMOS technology. The resultant frequency range is verified by simulation.

Keywords: ADPLL, DDS, NCO, FPGA-based DDS-ADPLL, FPGA Type-1 ADPLL, resonant sensors.

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1. INTRODUCTION

Digitally controlled Oscillators (DCOs) are a basic element used in All Digital Phase locked loops (ADPLLs). Many DCOS are implemented either as LC-Oscillator type as described in [1]. It can also be implemented with the help of ring oscillators as proposed in [2]. A digitally controlled Ring Oscillator (DCRO) is mainly used as oscillator in clock synthesis of SoCs. Variation in the frequency of the ring oscillator is possible using different approaches for example some of the earlier DCO architectures found in [3] uses a chain of inverters and a mux to select output of one of the inverter to be used as feedback based on the digital code applied to the select lines. In some of the literature like [4] & [5], the digital control of the frequency is achieved by using stacked tristate inverters. A single inverter has an array of tristate inverters connected in parallel. When a Tri state inverter is switched on, it adds extra current to charge or discharge the node, thereby reducing the time required for the signal to propagate. Advanced versions of this oscillator can be found in [6] where injection locking technique is used to improve its phase noise performance. Other variations of digitally controlled ring oscillator can be found in [7] where each inverter output is connected to a stack of varactors that can be switched on and off through a transistor. When the transistor connecting a varactor is switched on it adds extra capacitance to the node and when it is switched off the capacitance doesn't add up to the node. This principle can be used to create a DCO. Further, there are many variations and combinations of the above approaches can be used to build a wide variety of digitally control oscillator as can be found in [8]. But in such approaches a large bank of varactors is required usually of binary weighted sizes. This means increasing the range will considerably increase the size of the circuit.

In this paper, an alternate approach to obtain a wide tuning range DCO using ring oscillator is presented by using the technique of combinational frequency multiplier. This paper is described as follows. In the following sections the proposed circuit and the circuits of sub-components is described, then the design considerations are looked into, followed by it the Modelling of the circuit is done, then ultimately circuit implementation and simulation results are described.

2. PROPOSED ARCHITECTURE AND CIRCUIT

Figure-1 shows a simplified block diagram of the proposed DCO. It consists of three stage ring oscillator, a proposed novel combinational frequency doubler circuit and a multiplexor. Each stage of ring oscillator uses a Variable Delay Inverter (VDI). By applying an appropriate digital code, the delay produced by VDI can be varied. Therefore, allowing the DCRO to produce variable frequencies.

A conventional combinational multiplier is described in [9] and [10]. It is redrawn in Figure-2 for reference. The circuit shown in Figure-2 can produce frequency that is multiple of its input frequency. However, for the output waveform to have 50% duty cycle it is required that the delay introduced by the buffer in Figure-2 should be such that it produces only 90 degrees of phase shift to the corresponding input frequency. Therefore, it is obvious that it will produce a perfect 50% duty cycle waveform only for a single frequency. In other words, when the input frequency is slightly different from the one for which the circuit is designed then the output will not be a perfect square waveform as depicted in Figure-3.

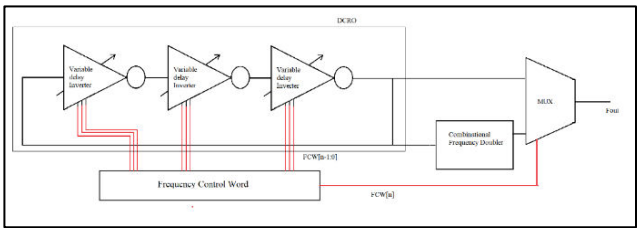

Figure-1. A simplified block diagram of the proposed DCO.

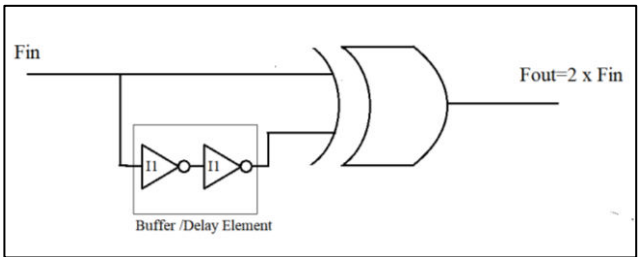

Figure-2. Conventional combinational frequency multiplier.

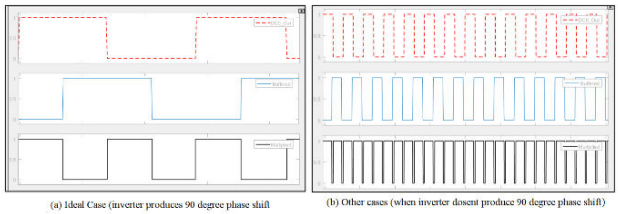

Figure-3. Response of the combinational multiplier to different input frequencies.

To overcome this problem, a novel combinational frequency multiplier that can produce a perfect square wave for a wide range of input frequencies is proposed. The block diagram of the proposed combinational frequency multiplier is as shown in the Figure-4.

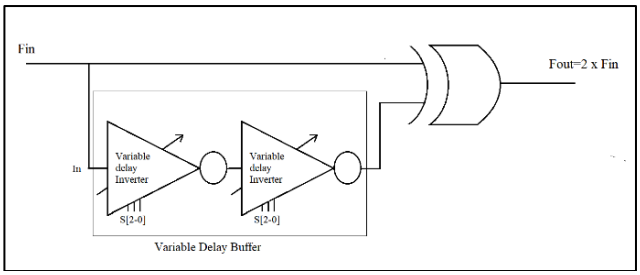

Figure-4. Proposed combinational frequency multiplier to produce double the input frequency with 50% duty cycle.

A digitally controlled, variable delay Buffer (VDB) is derived using two VDIs that are used in DCRO. The Frequency control word applied to DCRO is also applied to the two VDIs used in the Figure-4. As the frequency of DCRO changes due to change in Frequency control word, similarly the delay produced by the VDB also varies. Hence for different frequencies produced by the DCRO, the VDB used in frequency multiplier adjusts its delay such that the same amount of phase shift is produced for all the input frequencies. The circuit of variable delay inverter (VDI) is derived from the circuit proposed by [4]. A similar implementation can also be found in [3]. The delay of the VDI circuit shown in Figure-5 will depend on the input digital code and hence will be able to produce different phase shift based on input command word.

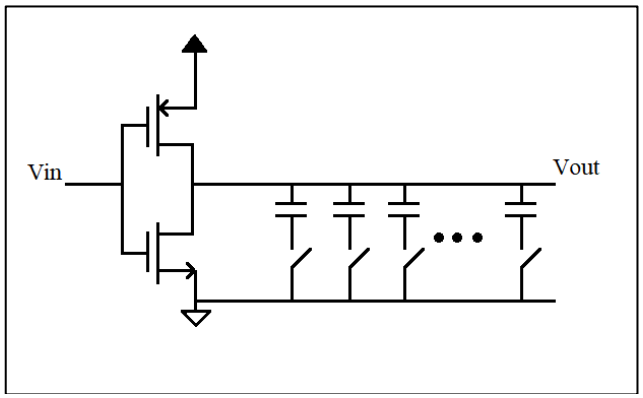

Figure-5. Circuit of the Variable Delay Inverter(VDI).

3. DESIGN OF PROPOSED DCO

If same VDIs is used in the combinational multiplier, the duty cycle will not be 50%. It will be slightly more than 50%. The following mathematical analysis provides an idea about the resultant duty cycle. As the DCRO uses 3 VDIs and its time period is twice the path delay.

$$t_{dcro} = 3 * 2 * t_{inv} \quad (1)$$

But VDB buffer uses only two VDIs, therefore its delay is.

$$t_{buff} = 2 * t_{inv} \quad (2)$$

The DCRO time-period is divided by two to indicate that the frequency at the output of multiplier is doubled.

$$\text{Duty Cycle } (\%) = \frac{t_{buff}}{t_{dcro}/_2} \times 100 = \frac{4*t_{inv}}{6*t_{inv}} \times 100 = 66.66\% \quad (3)$$

To overcome this problem, the VDIs used in the combinational multiplier are designed such that their time constant is a fraction of the time constant of the VDIs used in the DCO. The following simulation shows the variation of delay for different values of Beta.

$$t_{buff} = 2 * t_{inv} * \beta \quad (4)$$

For obtaining 50% duty cycle, the value of β can be found as shown below.

$$\frac{2*t_{inv}*\beta}{6*t_{inv}/_2} \times 100 = 50\% \quad (5)$$

$$t_{buff} = 2 * t_{inv} * \beta \quad (6)$$

$$\beta = 0.75 \quad (7)$$

It can be concluded that to obtain a 50% duty cycle using above multiplier. The inverter used in multiplier should have a delay 0.75 times that of the inverter used in the digitally controlled ring oscillator.

4. MODELLING AND ANALYSIS

An extremely simplified but workable model of CMOS inverter was developed to analytically examine the proposed DCO. The modelling of CMOS inverter is described in the following paragraphs.

In order to model the behavior of the CMOS inverter, its large signal characteristics as shown in the Figure-6 is considered.

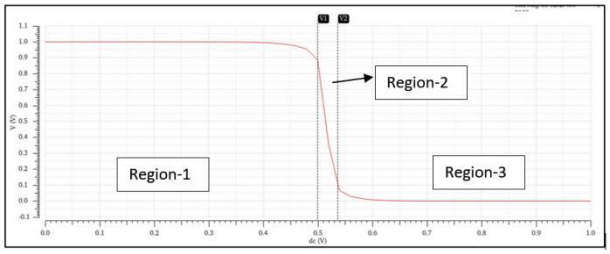

Figure-6. Large signal characteristics of a CMOS inverter.

The large signal behavior is divided into 3 regions for simplicity as shown in Figure-6. Region-1 and 3 corresponds to the non-linear behavior of the CMOS Inverter and in this region CMOS inverter can be assumed to be saturated and cut-off respectively. The region-2 corresponds to the linear region of the CMOS inverter and the inverter can be assumed to be acting like an amplifier.

$$V_{out'} = \begin{cases} V_{dd} & (V_{in} < Lower\ Threshold) \\ KV_{in} & (\text{Low Threshold} < Vin < Upper\ Threshold) \\ 0 & (V_{in} > Upper\ Threshold) \end{cases} \quad (8)$$

To incorporate the delay of the CMOS inverter, a pole is incorporated as shown in Equation (9) in mode-2.

$$V_{out'} = {K.V_{in}}/{(1 + s\tau)} \quad (9)$$

Finally, to incorporate the effect of noise, an extra noise component is added as shown in Equation (10) Noise is very important for modelling oscillators. Noise is assumed to be white for simplicity.

$$V_{out} = V_{out'} + n(t) \quad (10)$$

The functionality of the proposed DCO is tested by creating a model of CMOS Inverter in MATLAB based on the mathematical model described in equations (8)-(10). As described in the section below, the model is used to simulate the effect of beta value on the Duty cycle of the proposed combinational frequency multiplier. The Figure-7 shows the effect of variation of time constant (by varying Beta) of CMOS Inverter over the pulse width of the generated signal.

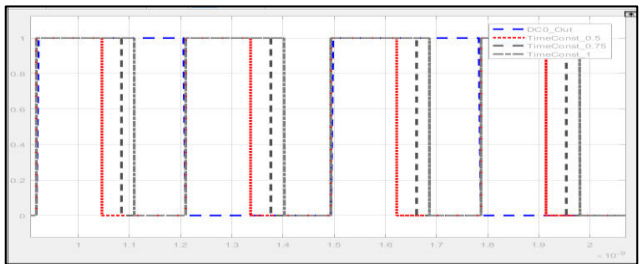

Figure-7. Effect of inverter time constant on the pulse width of the output of combinational frequency multipliers.

The change in duty cycle of the output of the combinational frequency multiplier due to change in time constant of the inverter (Beta value) is described in Table-1.

Table-1. Strouhal number for different geometric cases.

Beta	Duty Cycle
0.5	44.16
0.6	50.53
0.7	55.5
0.75	57.6

It is observed from the simulation that the actual beta value for obtaining 50% duty cycle is around 0.6. slightly less than that of the calculated value in equations (5) and (6), This is due to the non-ideal behaviour of the CMOS inverter.

It is to be noted that combinational frequency multiplier can be built by using a single inverter instead of buffer. This will reduce the number of components and will reduce area and power consumption. However, the output signal will be inverted. To change the polarity, an extra inverter can be added as shown in the Figure-8.

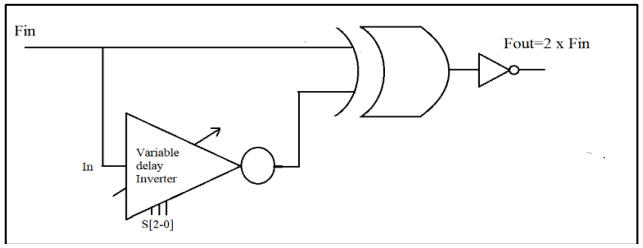

Figure-8. An alternate implementation of frequency multiplier using single VDI.

The circuit proposed in the Figure 8 is utilised to develop the proposed novel DCO with wide tuning range. The circuit of the proposed DCO is as shown in the

Figure-1. The output of the ring oscillator is fed to the combinational frequency multiplier described in Figure 8. This setup produces frequency which is twice the frequency produced by DCRO. The output of the DCRO and the proposed combinational multiplier are fed to a mux which can select either of these signals based on the select input. The select input to the mux acts like a master control that can switch the frequency between. For2xF.

5. SIMULATION RESULTS

A 5-bit proposed DCO circuit is then implemented in cadence using generic 90nm technology as a proof of concept. 1-volt VDD was used. The schematic entry of the circuit of VDI is as shown in the Figure-9. The varactors used are binary weighted.

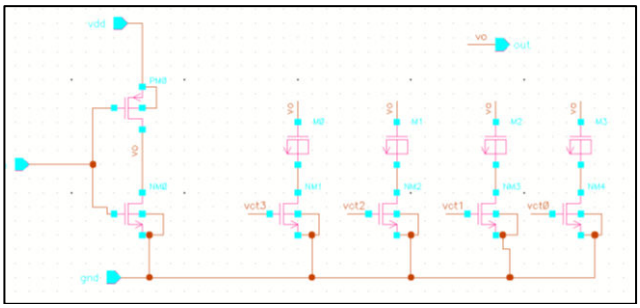

Figure-9. Circuit of VDI in implemented in cadence virtuoso.

The Figure-10 is the schematic of the proposed digitally controlled Oscillator using the combinational frequency doubler circuit. A modified combinational frequency doubler proposed in Figure-4, Figure-8 was used in this circuit. Note that extra buffers are added to increase the drive strength.

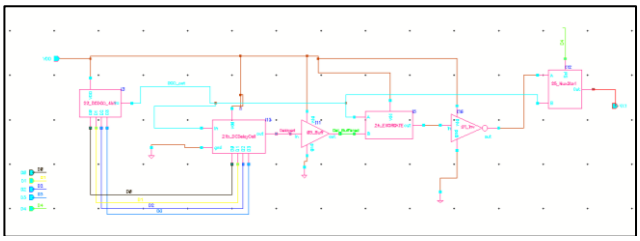

Figure-10. Schematic of the proposed DCO in cadence virtuoso.

The Figure-11 shows the transient response of the proposed frequency multiplier (doubler) for given input. The 1st waveform is the output of DCRO which acts like input to frequency multiplier, the last signal of figure is the output of proposed frequency multiplier. Its frequency is twice that of the input with almost 50% duty cycle.

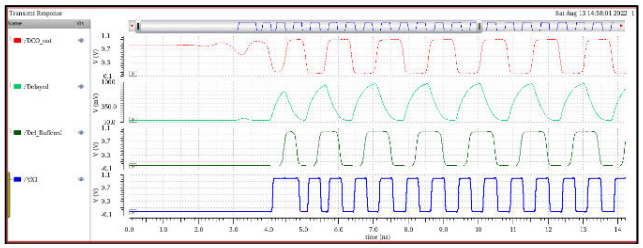

Figure-11. Transient response of the proposed DCO.

Figure-12 shows the frequency range of the proposed DCO. In order to simulate the range, the digital input is applied using pulses of weighted time periods. D0 is applied with a pulse of time period 25ns, D1 with a pulse of 50ns, D2 with 100ns and similarly D3, D4 with pulses of 200ns and 400ns respectively. Therefore, the input patter will run through 5'b00000 to 5'b11111 from 0ns to 400ns. The simulation results shown in Figure-13 corresponds to that of the conventional 4-bit ring oscillator as only the 4-LSBs are connected to it, it produces 16 different frequencies ranging from 1.29GHz to 0.67GHz. During sweep from 5'b00000 to 5'b11111, the LSB sequence and hence the frequency plot is repeated with same range. The simulation result shown in figure12-b corresponds to the proposed circuit. It can be observed that as the input is swept the output frequency varies from 2.9GHz to 0.67GHz.

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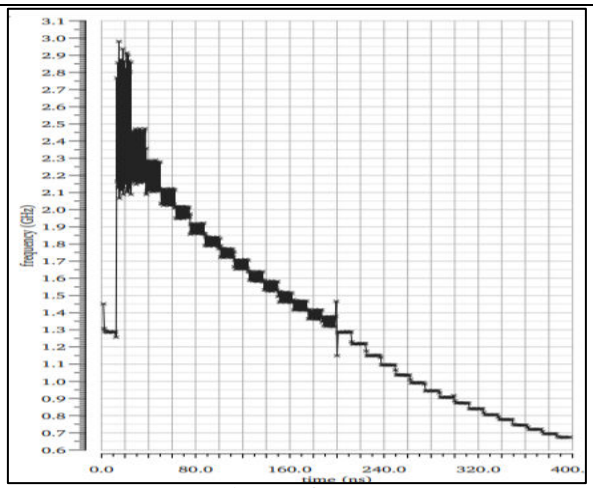
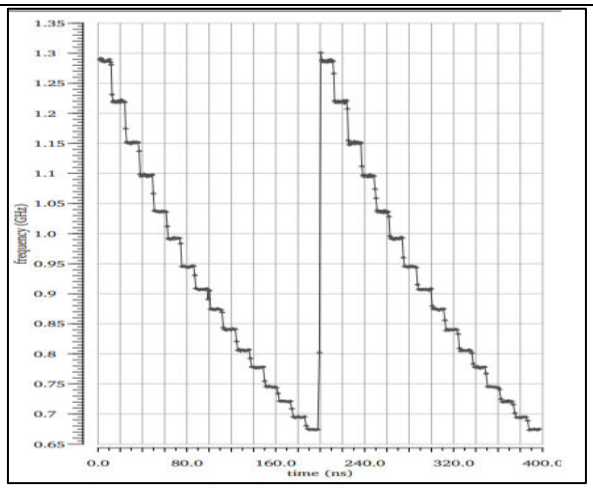


(a) Proposed DCO frequency Range



(b) Conventional DCO frequency range

Figure-12. Transient response of the proposed DCO.

6. CONCLUSIONS

In this paper a novel digitally controlled Oscillator using the concept of frequency multiplication is proposed. A novel combinational frequency multiplier is also proposed that can produce 50% duty cycle for all the applied input frequencies. A simplified and effective model of CMOS inverter is developed to analytically describe the behavior of the proposed DCO. Ultimately a 5-bit version of the proposed DCO is designed and simulated in CADENCE Virtuoso using generic 90nm CMOS technology. It was observed that the proposed DCO doubled the frequency range of the conventional 4-bit DCRO. The obtained frequency range of conventional DCRO is 0.67GHz-1.29GHz and that of the proposed DCO is from 0.67GHz - 2.9GHz.

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