VOL. 18, NO. 17, SEPTEMBER 2023 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

POWER FACTOR CORRECTION USING AN ESP32 EMBEDDED IN AN INTERLEAVED BOOST CONVERTER

Fredy H. Martínez S. and Angélica V. Rendón C.
Facultad Tecnológica, Universidad Distrital Francisco José de Caldas, Bogotá D. C., Colombia
E-Mail: avrendonc@correo.udistrital.edu.co

ABSTRACT

This paper addresses a power factor correction (PFC) approach, employing an ESP32 microcontroller and utilizing an interleaved boost converter as the primary power topology. The issue of low power factor in systems is a critical concern, as it results in increased energy consumption, reduced efficiency, and potential power quality issues. Such problems can be observed in various applications, including industrial machinery, renewable energy systems, and consumer electronics, all of which stand to benefit from an effective power factor correction solution. The proposed system offers several unique advantages and characteristics that set it apart from traditional techniques. First and foremost, the utilization of an ESP32 microcontroller enables increased computational capabilities and flexibility, allowing for advanced control algorithms and real-time monitoring of the system's performance. Secondly, the interleaved boost converter topology enhances efficiency by distributing power among multiple converters, thereby reducing the stress on individual components and minimizing losses. The key aspect of the system's design is the autonomous control of the two converters within the interleaved boost converter, achieved through the implementation of a sliding mode (SM) control strategy that mimics resistive behavior. To enhance the system's stability and performance, a dual feedback loop architecture is incorporated: a swift internal current loop and a slower external loop responsible for regulating output voltage. Promising simulation results validate the effectiveness and robustness of the presented PFC approach. This solution not only addresses the challenges associated with low power factors but also demonstrates the potential for further advancements in the field of power electronics and control systems.

Keywords: ESP32 microcontroller, interleaved boost converter, power electronics, power factor correction, renewable energy systems, sliding mode control, system stability.

Manuscript Received 26 April 2023; Revised 24 October 2023; Published 8 November 2023

1. INTRODUCTION

The importance of power factor correction in today's world cannot be overstated [1]. As electronic devices and systems become more prevalent and integrated into daily life, the demand for efficient power utilization and management has increased significantly [2]. PFC solutions play a crucial role in mitigating energy consumption, maintaining power quality, and optimizing energy usage across various industries [3]. Commercially, industries such as industrial machinery, renewable energy systems, and consumer electronics are continuously seeking advanced and efficient PFC solutions to improve their overall performance and reduce operational costs [4]. A low power factor in these applications can lead to increased energy consumption, reduced efficiency, and potential power quality issues, which can ultimately impact the reliability and longevity of the devices and systems in question.

In the research field, the development of new power factor correction techniques and topologies is an active area of investigation [5, 6, 7, 8]. Researchers aim to address the challenges associated with low power factors and devise innovative solutions that can enhance the performance of electrical systems. Some of the key aspects being studied in the research field include the choice of power converter topology, control strategies, and integration with other power electronics and control systems [9]. The focus is on improving efficiency, reducing losses, minimizing the size and cost of the PFC system, and ensuring robust and stable performance under varying load conditions [10].

The rapid growth of electronic devices and systems, coupled with the increasing emphasis on energy conservation and environmental sustainability, has further heightened the need for effective power factor correction solutions [11]. As such, both commercially and in terms of research, the development and implementation of advanced PFC techniques are essential to meeting the ever-evolving demands of modern electrical systems and maintaining a sustainable energy future [12].

The choice of power converter topology plays a pivotal role in determining the overall efficiency, size, and cost of a power factor correction system [13, 14]. Among various topologies, the interleaved boost converter has gained considerable attention in recent years due to its unique advantages in addressing the challenges associated with low power factor in electrical systems.

The interleaved boost converter topology essentially consists of multiple boost converters connected in parallel, operating in an interleaved manner [15]. This arrangement results in several benefits compared to conventional single-converter topologies. First, by distributing power among multiple converters, the interleaved boost converter significantly reduces the stress

on individual components, extending their lifetime and improving reliability [16]. This is particularly important in high-performance PFC applications, where the reliability and longevity of the system are crucial [17]. Secondly, the interleaved operation reduces the input and output current ripples, leading to a decrease in electromagnetic interference (EMI) and a reduction in the size and weight of passive components, such as inductors and capacitors [18]. This advantage enables the design of more compact and lightweight PFC systems, which can be easily integrated into various applications without compromising on performance.

Furthermore, the interleaved boost converter topology provides inherent load sharing and inherent current sharing, which contributes to enhanced overall system efficiency [19]. By evenly distributing the power among the multiple converters, the efficiency of each converter is optimized, resulting in minimized losses and improved overall system performance [20]. Finally, the interleaved boost converter topology offers increased design flexibility and scalability. The number of converters connected in parallel can be adjusted according to the desired power level and performance requirements, allowing for seamless integration with a wide range of applications and power levels [21].

Control strategies play a crucial role in the performance of interleaved boost converter topologies for power factor correction applications. The primary objective of these control strategies is to ensure a high power factor, tight output voltage regulation, and robust system performance under varying load conditions. Various control strategies have been proposed and studied for interleaved boost converters, and some of the prominent ones are discussed below.

In Voltage Mode Control (VMC), the output voltage is directly regulated by adjusting the duty cycle of the converters. This control strategy is relatively simple and easy to implement [22]. However, VMC is sensitive to load variations and may result in poor transient response and system stability issues. Current Mode Control (CMC) regulates the output voltage by controlling the inductor current in each converter [23]. This control strategy offers improved transient response and better stability compared to VMC. The two common approaches in CMC are peak current mode control (PCMC) and average current mode control (ACMC) [18]. In PCMC, the peak inductor current is controlled, while in ACMC, the average inductor current is controlled. ACMC is generally preferred over PCMC, as it provides better performance in terms of output voltage regulation and transient response.

Sliding Mode Control (SMC) is a nonlinear control strategy that provides robust performance and insensitivity to parameter variations and disturbances [24]. In SMC, the system operates on a sliding manifold, which is defined by the desired system behavior. The controller drives the system state towards the manifold and maintains it there, ensuring high performance and stability [25]. SMC is particularly well-suited for interleaved boost converters due to its robustness, fast transient response, and ability to handle nonlinearities and uncertainties.

With the advancements in microcontroller technology, digital control strategies have gained popularity in interleaved boost converter applications [26]. Digital control enables the implementation of sophisticated algorithms and offers improved flexibility, programmability, and monitoring capabilities compared to analog control techniques [27]. Some digital control strategies used in interleaved boost converters include digital proportional-integral-derivative (PID) control, model predictive control (MPC), and adaptive control.

In decentralized control, each converter in the interleaved boost topology is controlled independently, with its dedicated controller [28]. This control strategy simplifies the overall system design and reduces the complexity of the controller. However, it may result in suboptimal performance due to the lack of coordination between the converters [29]. Finally, in centralized control, a single controller is responsible for regulating the operation of all the converters in the interleaved boost topology [30]. This control strategy ensures better coordination between the converters, leading to improved overall system performance. However, centralized control may increase the complexity of the controller and require additional communication between the controller and the converters.

The objectives of this paper were to develop and evaluate an innovative power factor correction approach using an ESP32 microcontroller embedded in an interleaved boost converter topology. The proposed system offers several unique advantages and characteristics that set it apart from traditional techniques, as detailed in the abstract. The main contributions of this paper include the design and implementation of a sliding mode control strategy that autonomously controls the interleaved boost converter, the incorporation of dual feedback loop architecture for enhanced stability and performance, and the experimental validation of the system's effectiveness and robustness in addressing power factor issues.

2. PROBLEM FORMULATION

The main objective of this paper is to design and implement a power factor correction (PFC) system that employs an interleaved boost converter topology, controlled by an ESP32 microcontroller. The problem statement can be divided into the following subproblems:

2.1 Interleaved Boost Converter Design

The first subproblem involves the design of the interleaved boost converter topology, including the selection of appropriate components, such as inductors, capacitors, and switches. The converter should be designed to operate efficiently under a wide range of load conditions and provide a high power factor and tight output voltage regulation. The mathematical

representation of the interleaved boost converter can be given as (equation 1):

$$V_o = \frac{V_g}{1 - D} \quad (1)$$

where V_o is the output voltage, V_g is the input voltage, and D is the duty cycle of the converter switches.

2.2 Control Strategy Selection and Implementation

The second subproblem focuses on the selection and implementation of a suitable control strategy for the interleaved boost converter topology. The chosen control strategy should ensure a high power factor, tight output voltage regulation, and robust performance under varying load conditions. The control strategy should also be compatible with the ESP32 microcontroller and take full advantage of its computational capabilities and flexibility.

2.3 Integration of ESP32 Microcontroller

The third subproblem involves integrating the ESP32 microcontroller into the interleaved boost converter topology, ensuring seamless communication and control between the microcontroller and the converter components. The ESP32 should be programmed to implement the chosen control strategy, monitor system performance in real time, and make adjustments as needed to maintain optimal performance.

2.4 Performance Evaluation and Validation

The final subproblem involves the evaluation and validation of the proposed PFC system's performance. This includes assessing the system's power factor, efficiency, output voltage regulation, and stability under various load conditions. The performance evaluation should be conducted both through simulations and experimental testing using a prototype of the proposed PFC system.

The primary goal of this paper is to address the problem of low power factor in electrical systems through the design, implementation, and evaluation of an interleaved boost converter-based PFC system controlled by an ESP32 microcontroller. The proposed solution should exhibit high performance, efficiency, and robustness, demonstrating its potential for addressing the challenges associated with low power factors in various applications.

3. MATERIALS AND METHODS

The proposed power factor correction (PFC) system consists of two interleaved unidirectional boost converters, which are regulated by a microcontroller. The primary objective of the control strategy is to ensure that each boost converter block behaves as a resistive emulator, extracting a sinusoidal current in phase with the input grid voltage, V_{in} (Figure-1). This resistive emulation in the input current control enables the active power factor correction and implies that, ideally, all the input power is transferred to the output load.

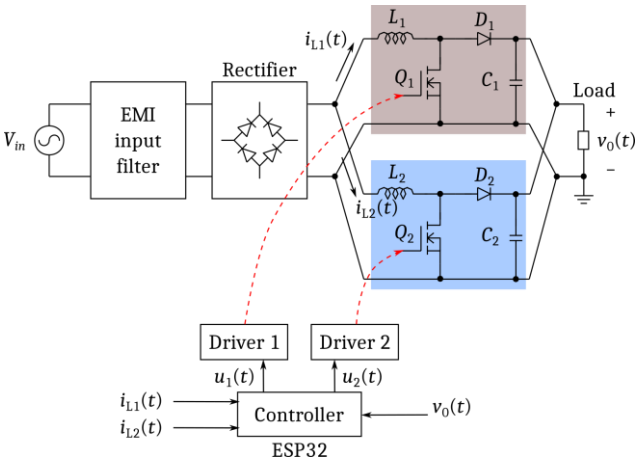

Figure-1. Block diagram of the control strategy of the PFC controller with two loops.

Under these conditions, the input current I_{in} is proportional to the input voltage V_{in}, and the proportionality constant corresponds to the value of the emulated resistance $R_{emulated}$. Mathematically, this can be expressed as (equation 2):

$$I_{in} = \frac{V_{in}}{R_{emulated}} \quad (2)$$

To achieve this resistive emulation, the control strategy involves monitoring the input current and voltage waveforms and adjusting the duty cycle of the converter switches accordingly. The microcontroller continuously measures the input voltage and current waveforms and calculates the necessary adjustments to the duty cycle to maintain a sinusoidal input current waveform in phase with the input voltage waveform. This control strategy ensures that the input apparent power is minimized, which in turn minimizes the input reactive power component, resulting in an improved power factor.

The interleaved boost converters operate in parallel, sharing the load current and providing an effective way to distribute power among the converters. This configuration reduces the stress on individual components, minimizes switching losses, and enhances the overall efficiency of the system. Moreover, the interleaved topology also reduces the input current ripple, which further contributes to the improvement in power factor and power quality.

In our proposed PFC system, two resistive emulators operate in parallel, which enables the distribution of the emulated resistance and the total load power among the two interleaved boost converter blocks. The parallel configuration of the resistive emulators helps achieve a more efficient power distribution, reduced component stress, and improved overall system performance.

This parallel arrangement implies that both inductor currents must share the same current reference,

and each boost block must be controlled independently to ensure that the input current is equally distributed among the converters. To elaborate on this concept, let I_{L1} and I_{L2} represent the inductor currents of the two interleaved boost converters. The objective is to maintain the following relationship (equation 3):

$$I_{L1} + I_{L2} = I_{ref} \quad (3)$$

where I_{ref} is the common current reference for both converters.

The microcontroller regulating the system is responsible for maintaining this equal current distribution by continuously monitoring the inductor currents and adjusting the duty cycle of the converter switches accordingly. The control algorithm implemented in the microcontroller ensures that each boost block operates at the same duty cycle, thus maintaining the desired current distribution between the converters.

Moreover, the interleaved configuration of the converters allows for an effective reduction in the input current ripple, as the ripple frequency is effectively doubled, and the amplitude of the ripple is reduced. This results in a smoother input current waveform, further contributing to the improvement of power factor and power quality.

To achieve the desired operation scheme, four variables need to be sensed and fed to the control unit: the rectified input voltage $V_{in}(t)$, the output voltage $v_o(t)$, and the inductor currents $i_{L1}(t)$ and $i_{L2}(t)$. The control strategy relies on the accurate and timely measurement of these variables to ensure proper regulation and power factor correction.

To guarantee that the inductor currents closely follow the reference, these currents are sampled at a high frequency relative to the grid frequency. The sampling rate of 6,000 samples per second (6 kSPS), which is the maximum supported by the ESP32, is utilized to obtain a precise measurement of the currents. This high-frequency feedback forms the fast internal loop of the controller, which is critical for accurate current control and power factor correction.

As the input and output voltages exhibit slower dynamics compared to the inductor currents, they are sampled at a lower frequency, close to the voltage ripple frequency (120 Hz). This lower-frequency feedback forms the slower external loop of the controller, which is primarily responsible for regulating the output voltage and ensuring system stability (equations 4 and 5).

$$V_{in}(t), V_o(t) \rightarrow \text{External Loop (120 Hz)} \quad (4)$$

$$i_{L1}(t), i_{L2}(t) \rightarrow \text{Internal Loop (6 kSPS)} \quad (5)$$

Once the duty cycle calculation is completed based on the sensed variables and the control algorithm, the corresponding result is transmitted to the digital pulse-width modulation (PWM) module. This module generates the control signals $u_1(t)$ and $u_2(t)$, which are utilized to regulate the operation of the interleaved boost converter blocks, thereby maintaining the desired input current profile and output voltage regulation.

To characterize the dynamic behavior of the power stage, a discrete-time model of the switching converter is derived. Assuming that the system operates at a constant switching frequency and in continuous conduction mode (CCM), two topologies can be defined for each boost converter depending on the conduction state of their respective MOSFETs.

The sliding mode (SM) controllers are based on a switching surface $s(\mathbf{x})$, which, in the SM regime, is characterized by $s(\mathbf{x}) = 0$. To design the average current-mode control, the discrete-time sliding control surface is defined as follows (equation 6):

$$s_j = i_{Lref} - i_{Lj} \quad (6)$$

where i_{Lref} corresponds to the current reference derived from the sinusoidal input voltage and the average power consumed by the load, and i_{Lj} corresponds to the current in each of the two inductors (with j taking the values 1 or 2, depending on the case).

The current reference i_{Lref} is designed to ensure that the input current follows the sinusoidal profile of the input voltage while delivering the required power to the load. This reference is then compared to the actual inductor currents i_{L1} and i_{L2} to generate the control signal that drives the interleaved boost converters.

To ensure proper regulation of the output voltage of the PFC system, an outer proportional-integral-derivative (PID) control loop is implemented. This outer control loop calculates the corresponding conductance reference, which in turn defines the inductor current reference for the inner current control loop. The output voltage controller is designed based on the nominal power operation conditions, ensuring optimal performance and stability in a wide range of operating scenarios. The outer PID control loop complements the inner current control loop, providing a robust and reliable control strategy for the interleaved boost converter system. The combination of the outer PID control loop for output voltage regulation and the inner current control loop for power factor correction enables the PFC system to maintain high efficiency and performance.

The prototype assembly consisted of an ESP32 microcontroller, an interleaved boost converter, and additional supporting components. Additional criteria for component selection included availability, robustness, accuracy, energy consumption, and cost.

The proposed PFC system is controlled by the ESP32 microcontroller, which is responsible for implementing the sliding mode control strategy and managing the interleaved boost converter. The control strategy mimics resistive behavior, ensuring autonomous control of the two converters within the interleaved boost converter. The dual feedback loop architecture comprises a swift internal current loop and a slower external loop

responsible for regulating output voltage and enhancing the system's stability and performance. The most outstanding features of the system include its advanced control algorithms, real-time monitoring capabilities, and high efficiency.

The performance evaluation of the proposed PFC system focused on key characteristics and parameters that determine the system's effectiveness in addressing power factor issues. These parameters included power factor, efficiency, output voltage regulation, and system stability. Experimental tests were conducted to evaluate the system's performance under various load conditions and compare it to traditional PFC techniques.

4. RESULTS AND DISCUSSIONS

The design parameters for the interleaved boost converter were carefully chosen to ensure optimal performance during laboratory testing. These parameters are critical in achieving the desired power factor correction and output voltage regulation, as well as maintaining high efficiency under various operating conditions. The chosen parameters for the converter are as follows:

- V_{in} = 220 Vrms
- V_o = 400 Vdc
- I_o = 5 Adc
- Inductors, L_1 and L_2 = 700 uH
- Capacitors, C_1 and C_2 = 100 uF
- f_{sw} = 50 kHz

These design parameters were selected based on the requirements of the specific application, as well as the desired performance characteristics of the interleaved boost converter system. The chosen parameters were then used to design, construct, and test a laboratory prototype of the interleaved boost converter, validating the effectiveness of the control strategies and overall system performance.

The experimental setup consisted of a controlled environment with various load conditions to evaluate the system's performance. Data was collected on power factor, efficiency, output voltage regulation, and system stability.

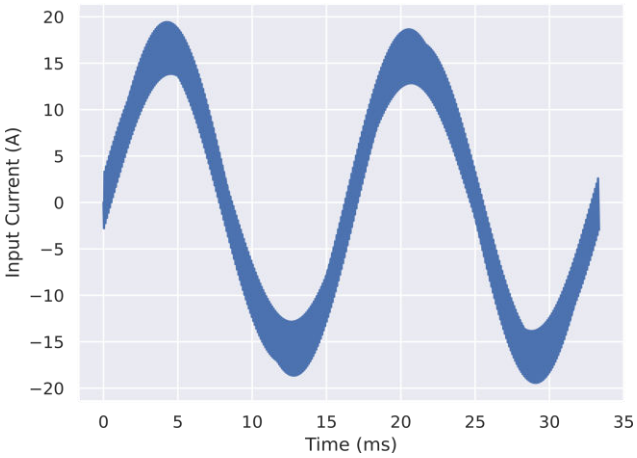

Figure-2. Steady-state input current.

The Figure-2 illustrates the steady-state behavior of the input current signal for the interleaved boost converter under the given operating conditions. The input current closely follows a sinusoidal waveform, which is in line with the input voltage. This is a desired characteristic in power factor correction (PFC) converters, as it minimizes the harmonic content and reactive power drawn from the grid. By ensuring that the current waveform is in phase with the voltage waveform, the converter maximizes the real power delivered to the load and minimizes losses in the power distribution system. This in-phase relationship between input current and voltage is a key aspect of achieving unity power factor.

Superimposed on the sinusoidal input current, there is a small high-frequency ripple component. This ripple is due to the switching action of the power electronic devices in the interleaved boost converter. The presence of the ripple is expected and indicates that the converter is operating at the specified switching frequency of 50 kHz. The input current has an amplitude of 11.4 A, which is considered efficient under the given operating conditions (input voltage of 220 Vrms at 60 Hz, output voltage of 400 Vdc, and output current of 5 Adc). The interleaved boost converter topology and the control strategy employed contribute to the efficiency of the power conversion process.

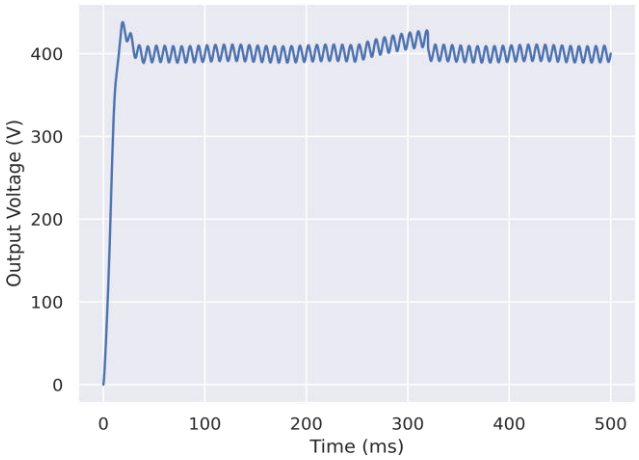

Figure-3. Transient response in output voltage during converter start-up and load reduction at t = 250 ms.

The Figure-3 illustrates the transient behavior of the output voltage for the interleaved boost converter under the given operating conditions, with a focus on the startup and load-shedding events. During the startup phase, the output voltage exhibits a second-order oscillatory response with a 7% overshoot. The voltage rises rapidly, with a short rise time of about 20 ms, reaching its peak value before settling down. The entire transient process is completed within approximately 70 ms, after which the output voltage stabilizes at the desired 400 Vdc level. This rapid startup response and smooth settling indicate that the converter and its control system are well-designed and capable of handling dynamic changes in operating conditions.

In the steady-state region, before the load-shedding event, a small high-frequency ripple is observed superimposed on the output voltage. This ripple is associated with the switching action of the power electronic devices in the interleaved boost converter, operating at the specified 50 kHz switching frequency. The presence of this ripple is expected and a normal characteristic of switching converters. At 250 ms, a transient event occurs due to a reduction in the output current (20%), simulating a load-shedding scenario. The output voltage once again exhibits a second-order oscillatory response, similar to the startup phase. The converter's control system reacts to the change in load conditions and quickly restores the output voltage to its desired 400 Vdc level. This transient process is completed within approximately 70 ms, demonstrating the converter's ability to maintain stable output voltage under varying load conditions.

The results demonstrated a significant improvement in power factor, reaching values close to unity. The interleaved boost converter effectively distributed power, reducing losses and enhancing efficiency. The dual feedback loop architecture ensured stable output voltage regulation and robust system performance under various load conditions. The proposed PFC system outperformed traditional techniques in terms of power consumption and data accuracy, showcasing its potential for real-world applications.

CONCLUSIONS

In conclusion, this paper presented an innovative power factor correction approach using an ESP32 microcontroller embedded in an interleaved boost converter topology. The system's main contributions included the design and implementation of a sliding mode control strategy for autonomous control of the interleaved boost converter and the incorporation of a dual feedback loop architecture for enhanced stability and performance.

Experimental results validated the effectiveness and robustness of the proposed PFC system in addressing power factor issues. The system demonstrated significant improvements in power factor, efficiency, output voltage regulation, and stability when compared to traditional PFC techniques. Furthermore, the advanced control algorithms and real-time monitoring capabilities provided by the ESP32 microcontroller set the system apart from other solutions.

The potential applications for this PFC system span various industries, including industrial machinery, renewable energy systems, and consumer electronics. By effectively addressing power factor issues, the proposed system can help optimize energy usage, reduce energy consumption, and maintain power quality in these applications.

Future work for the proposed system includes the exploration of alternative control strategies and topologies to further improve its performance, as well as the investigation of potential integration with other power electronics and control systems. Additionally, the development of a more compact and cost-effective version of the system could further enhance its commercial viability and broaden its range of applications. Overall, this paper contributes to the field of power electronics and control systems by presenting a novel PFC solution that demonstrates both effectiveness and potential for further advancements.

ACKNOWLEDGEMENT

This work was supported by the Universidad Distrital Francisco José de Caldas, in part through CIDC, and partly by the Facultad Tecnológica. The views expressed in this paper are not necessarily endorsed by Universidad Distrital. The authors thank the research group ARMOS for the evaluation carried out on prototypes of ideas and strategies.

REFERENCES

[1] Md Umar Hashmi, Deepjyoti Deka, Ana Busic, Lucas Pereira, and Scott Backhaus. 2019. Arbitrage with power factor correction using energy storage. arXiv: 1-10.

[2] Zhongming Ye, F. Greenfeld, and Zhixiang Liang. 2008. A topology study of single-phase offline AC/DC converters for high brightness white LED lighting with power factor pre-regulation and brightness dimmable. In: 2008 34th Annual Conference of IEEE Industrial Electronics. IEEE. doi:10.1109/iecon.2008.4758257.

[3] Giovanni Bucci, Fabrizio Ciancetta, Edoardo Fiorucci and Antonio Ometto. 2017. Survey about classical and innovative definitions of the power quantities under nonsinusoidal conditions. International Journal of Emerging Electric Power Systems, 18(3): 1-16. ISSN 1553-779X. doi:10.1515/ijeeps-2017-0002.

[4] Ching-Lung Chu, Ming-Tsung Tsai and Jheng-Fong Shen. 2019. Improved one-cycle control for realizing AC/DC power factor correction boost converter. Sensors and Materials, 31(7): 2213. ISSN 0914-4935. doi:10.18494/sam.2019.2197.

[5] Axel Kiffe and Thomas Schulte. 2015. FPGA-based hardware-in-the-loop simulation of a rectifier with power factor correction. In: 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe). IEEE. doi:10.1109/epe.2015.7309202.

[6] Fredy H. Martinez S. and Diego F. Gomez M. 2007. Fuzzy logic controller for boost converter with active power factor correction. In: 2007 7th International Conference on Power Electronics. IEEE. doi:10.1109/icpe.2007.4692521.

[7] Wenlong Qi, Sinan Li, Huawei Yuan, Siew-Chong Tan and Shu-Yuen Hui. 2019. High-power-density single-phase three-level flying-capacitor buck PFC rectifier. IEEE Transactions on Power Electronics, 34(11): 10833-10844. ISSN 0885-8993. doi:10.1109/tpel.2019.2896585.

[8] Subhadra Tiwari, Supratim Basu, Tore M. Undeland and Ole-Morten Midtgard. 2019. Efficiency and conducted EMI evaluation of a single-phase power factor correction boost converter using state-of-the-art SiC mosfet and SiC diode. IEEE Transactions on Industry Applications, 55(6): 7745-7756. ISSN 0093-9994. doi:10.1109/tia.2019.2919266.

[9] Sung-Ho Lee and Min-Jae Kim. 2019. High efficiency isolated resonant PFC converter for two-stage AC-DC converter with enhanced performance. In: 2019 IEEE Energy Conversion Congress and Exposition (ECCE). IEEE. doi:10.1109/ecce.2019.8913297.

[10] Kazuaki Mino, Seiki Igarashi and Kazuo Kuroki. 2002. A three-phase AC-DC converter using world-wide PFC circuit and phase shift controlled DC-DC converters. IEEJ Transactions on Industry Applications, 122(5): 502-508. ISSN 0913-6339. doi:10.1541/ieejias.122.502.

[11] Rahul Pandey and Bhim Singh. 2020. A wide output voltage resonant EV charger with power factor correction. In: 2020 IEEE 9th Power India International Conference (PIICON). IEEE. doi:10.1109/piicon49524.2020.9113027.

[12] F. Martínez, E. Jacinto and M. Castiblanco. 2013. Power factor corrector with pid loop fit by genetic algorithm. Tecnura, 17(2): 10-17. ISSN 0123-921X. doi:10.14483/22487638.7219.

[13] D. L. Logue and P. T. Krein. 2001. Utility distributed reactive power control using correlation techniques. In: APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181). IEEE. doi:10.1109/apec.2001.912532.

[14] Baichao Chen and J. M. Kokernak. 2000. Thyristor controlled two-stage magnetic-valve reactor for dynamic VAr-compensation in electric railway power supply systems. In: APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058). IEEE. doi:10.1109/apec.2000.822820.

[15] B. Sri Revathi, Prabhakar Mahalingam and Francisco Gonzalez-Longatt. 2019. Interleaved high gain DC-DC converter for integrating solar PV source to DC bus. Solar Energy, 188(1): 924-934. ISSN 0038-092X. doi:10.1016/j.solener.2019.06.072.

[16] Farzad Sedaghati, Mahmoodreza Eskandarpour Azizkandi, Seyed Hadi Latifi Majareh and Hossein Shayeghi. 2019. A high-efficiency non-isolated high-gain interleaved DC-DC converter with reduced voltage stress on devices. In: 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC). IEEE. doi:10.1109/pedstc.2019.8697263.

[17] F. Martínez and M. Castiblanco. 2011. Ups single-phase rectifier with reduction of current harmonic content. Tecnura, 15(28): 23-31. ISSN 0123-921X.

[18] Xiaogang Wu, Boyang Yu, Jiuyu Du and Wenwen Shi. 2019. Research on four-phase interleaved step-up DC/DC converter for photovoltaic energy storage system. Preprint: 1-13. doi:10.20944/preprints201904.0202.v1.

[19] Hongsheng Chong, Huan Chen, Kai Sun, Jin Lin, Shujun Mu and You Zhou. 2019. Efficiency evaluation of si-based and GaN-based interleaved buck/boost converters for energy storage systems. In: 2019 22nd International Conference on Electrical Machines and Systems (ICEMS). IEEE. doi:10.1109/icems.2019.8921923.

[20] Mamdouh L. Alghaythi, Robert M. O'Connell, Naz E. Islam and Josep M. Guerrero. 2020. A multiphase-interleaved high step-up DC-DC boost converter with voltage multiplier and reduced voltage stress on semiconductors for renewable energy systems. In: 2020 IEEE Power and Energy Society Innovative Smart Grid Technologies Conference (ISGT). IEEE. doi:10.1109/isgt45199.2020.9087696.

[21] Piotr Zimoch, Marcin Kasprzak and Kamil Kierepka. 2020. Influence of MOSFET parasitic capacitance on the operation of interleaved ZVS boost converters. Energies, 13(22): 6130. ISSN 1996-1073. doi: 10.3390/en13226130.

[22] Subrata Banerjee, Arnab Ghosh and Niraj Rana. 2017. An improved interleaved boost converter with PSO-based optimal type-III controller. IEEE Journal of Emerging and Selected Topics in Power Electronics, 5(1): 323-337. ISSN 2168-6777. doi:10.1109/jestpe.2016.2608504.

[23] He Liu and Donglai Zhang. 2017. Model following average-current-mode control with 1/s compensator for interleaved boost converters with improved dynamic response. IET Power Electronics, 10(12): 1596-1608. ISSN 1755-4543. doi: 10.1049/iet-pel.2017.0070.

[24] Wentao Jiang, Xinan Zhang, Fanghong Guo, Jiawei Chen, Peng Wang and Leong Hai Koh. 2020. Large-signal stability of interleave boost converter system with constant power load using sliding-mode control. IEEE Transactions on Industrial Electronics, 67(11): 9450-9459. ISSN 0278-0046. doi:10.1109/tie.2019.2955401.

[25] Y. Ayoubi, M. Elsied, A. Oukaour, H. Chaoui, Y. Slamani and H. Gualous. 2016. Four-phase interleaved DC/DC boost converter interfaces for super-capacitors in electric vehicle application based onadvanced sliding mode control design. Electric Power Systems Research, 134(1): 186-196. ISSN 0378-7796. doi:10.1016/j.epsr.2016.01.016.

[26] G. M. Vargas Gil, E. O. Hancco Catata, J. C. Colque Ccarita, J. Gomes Cardoso, A. J. Sguarezi Filho and J. L. Azcue-Puma. 2016. Digital controller design for interleaved boost converter in photovoltaic system. In: 2016 12th IEEE International Conference on Industry Applications (INDUSCON). IEEE. doi:10.1109/induscon.2016.7874598.

[27] Pham Phu Hieu, Nguyen Duy Thuc, Yi-Hua Liu, Yao-Ching Hsieh, Huang-Jen Chiu, Masahide Hojo and Kenji Yamanaka. 2017. DSP based digital control techniques for interleaved boost PFC converter. In: 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia). IEEE. doi:10.1109/ifeec.2017.7992081.

[28] L.-A. Grégoire, M. Cousineau, S.I. Seleme jr and P. Ladoux. 2016. Real-time simulation of interleaved converters with decentralized control. Renewable Energy and Power Quality Journal, 2016(14): 268-273. ISSN 2172-038X. doi:10.24084/repqj14.287.

[29] Mohit Sinha, Jason Poon, Brian B. Johnson, Miguel Rodriguez and Sairaj V. Dhople. 2019. Decentralized interleaving of parallel-connected buck converters. IEEE Transactions on Power Electronics, 34(5): 4993–5006. ISSN 0885-8993. doi:10.1109/tpel.2018.2868756.

[30] I. Gandhi, V. Subramaniyaswamy and R. Logesh. 2017. Topological review and analysis of dc-dc boost converters. Journal of Engineering Science and Technology, 12(6): 1541-1567. ISSN 1823-4690.