VOL. 18, NO. 19, OCTOBER 2023 ISSN 1819-6608
ARPN Journal of Engineering and Applied Sciences

www.arpnjournals.com

A NOVEL APPROACH TO GENERATE TRIGONOMETRIC FUNCTIONS USING HIGH PERFORMANCE FPGA

B. Khaleelu Rehman[1], Prasanthi Kumari N.[2], Raman Kumar[3], Vetriveeran Rajamani[4] and Mudasar Basha[5]
[1]Department of Electrical and Computer Engineering, Chaitanya Bharathi Institute of Technology (A), Hyderabad, India
[2]School of Computer Sciences, UPES, Dehradun, India
[3]Department of Electrical and Computer Engineering, Nalla Malla Reddy Engineering College, Hyderabad, India
[4]School of Electronics Engineering (SENSE), Vellore Institute of Technology, Vellore, India
[5]Department of Electrical and Computer Engineering, B V Raju Institute of Technology, Narsapur, Telangana, India
E-Mail: khaleelurehmanb_ece@cbit.ac.in

ABSTRACT

This paper describes the novel approach to generate the trigonometric function sine wave with different amplitudes and different frequencies. The proposed design is synthesized using Xilinx ISE 14.7 using Verilog HDL programming language and simulated using the modelsim simulator. The sine wave generation is targeted on the high performance Zynq 7-series Zedoard FPGA (7020) which has a capability of programming language (PL) and processing system (PS). Generation of sine wave is carried out using Xilinx IP Core (DDS) approach with simulation, and synthesis. Zed board works on 28nm technology. Hardware device utilization summary of the design is analyzed along with the timing values. The power report of the design is extracted using the X power analyzer. Power analysis is compared with Micro wind software and X-power analyzer.

Keywords: Xilinx ISE, FPGA, zedboard, modelsim.

Manuscript Received 8 August 2023; Revised 18 November 2023; Published 11 December 2023

1. INTRODUCTION

Modern Electronic equipment such as function generators uses Sine wave generation for calibration, reference, and other purposes. FPGAs are more popular nowadays because of their less delay, less area, and low power consumption. The most important trigonometric functions like sine and cosine waves in digital circuits can be generated, simulated, and synthesized by using different techniques like Direct Digital Synthesizer(DDS) core, CORDIC(Coordinate Rotation and Digital Computer) based algorithm, Double integration, LUT based approach. This article proposes a novel and simple approach to generate the sine wave with the amplitude and frequency. The sine wave can easily be transferable to any targeted chip.

1.1 Sine Look Up Table Generation

The method of generating the samples of sine waves with certain amplitude and frequency can be done by using MATLAB or Python script. The amplitude of samples is converted into binary data and stored in the ROM memory of FPGA. Here this article proposes the generation of sine wave values using online generating sine wave values using the website [1]. This online tool provides one complete cycle with fixed frequency and amplitude levels. For example, one can select the number of points as shown in Table-1. Here in this example, 32 points are taken and similarly, the maximum amplitude is set as 255 the number of samples per row is selected as 8 and the generated samples are taken in decimal format. The hexadecimal format samples can also be generated. The 8 bit binary data is taken as an output. The maximum value for an 8 bit data is 255(2^8-1). All the values in the table can be generated according to the design and according to the frequency and amplitude requirement of the design engineer

Table-1. Sine look up table generator input.

Sine Look Up Table Generator Input	
Number of points	32
Max Amplitude	255
Numbers Per Row	8
○Hex	◉ Decimal

```
{128,152,176,198,218,234,245,253,
255,253,245,234,218,198,176,152,
128,103,79,57,37,21,10,2,
0,2,10,21,37,57,79,103}
```

2. LITERATURE REVIEW

Many researchers proposed trigonometric functions like sine waves, and cosine waves using the hardware description language (HDL). Upadhyaya *et al* [2] proposed a Direct Digital Synthesizer core approach to generate a sine sample using a Spartan 3 FPGA device. The hardware device utilization is discussed and the power analysis is carried out. Bohrn *et al* [3] proposed ASIC Sine wave using Spartan 3 FPGA device and the hardware utilization summary is summarized and the different algorithms are compared. Liu *et al* [4] proposed the AM modulated wave form using a DDS core with the help of a NIOS-II softcore processor and the Quartus II FPGA device. The theoretical frequency and the measured frequency from the oscilloscope are compared. Al-Safi *et*

al [5] proposed the Modulated signals using Xilinx Vivado and Zedboard.FFT analysis is carried out for the sine signal and the synthesis report is tabulated. Many researchers proposed sine wave generation on FPGA [6]-[8].

3. PROPOSED DESIGN

The proposed design for the sine wave generation is discussed below:

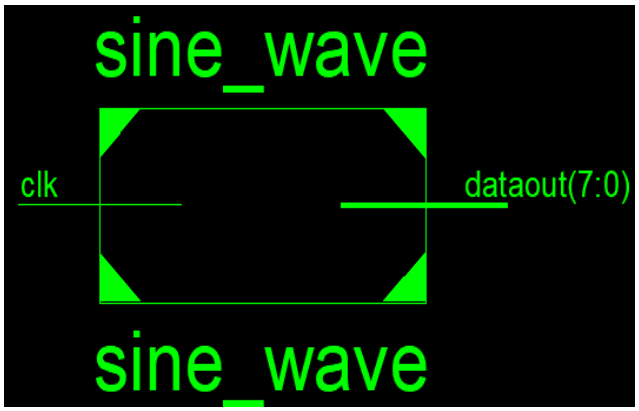


Figure-1. RTL View of sine signal.

Figure-1 shows the RTL view of the sine signal with 1 bit clock signal as an input and the 8 bit output data as the sine wave signal. The RTL schematic of the design consists of the ROM memory and the counter of 32 bits. The counter is incremented and the address of the counter is mapped with the sine wave samples. The counter repeats after 32 values. The first 32 values correspond to each sine wave signal.

3.1 Modelsim Simulation Results

Figure-2 shows the modelsim simulation output of a sine wave signal. The simulation results can also be obtained from the Xilinx I-sim or X-sim but the mentor graphics modelsim simulation will show the analog signal waveform. One complete sine wave takes 32 clock pulses and each clock pulse has 10ns of time, so the total time for one complete cycle is given by the clock period multiplied by the number of clock pulses.320ns can be observed in the output waveform. From the simulation output, it can be observed that the second cycle starts at 320ns and completes the second cycle at 640ns, and so on. All the generated values from the website are plotted. The values generated from table number 1 start from 128 and end at 103. The same values are observed in the simulation output window in the decimal format. The decimal value 128 shown is the start of the second cycle. The frequency of the waveform is the reciprocal of the period i.e. 1/320ns=3.125MHz.So the frequency of the sine waveform is 3.125Mhz. Similarly, different frequency values can be obtained by changing the parameters in Table-1. The table shown below shows the maximum amplitude and the different frequencies of a sine wave signal.

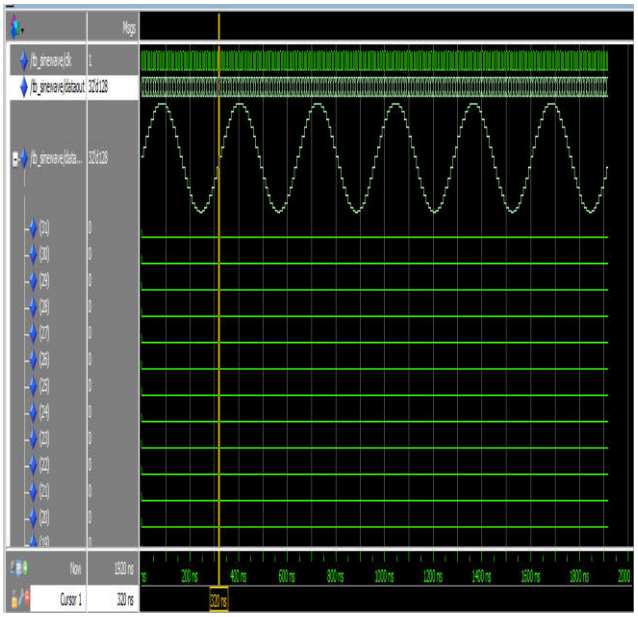


Figure-2. Modelsim simulation of a sine wave.

Table-2. Sine wave signal with different frequencies.

S. No	Number of points	Maximum amplitude	Clock period	Frequency of the signal
1	100	300	10ns	1MhZ
2	200	1500	1ns	5 MHz
3	1000	500	1ns	10Mhz
4	20	1000	1ns	50 MHz
5	10	2000	1ns	100 MHz

The table shown above is the trigonometric sine wave with different frequencies like 1 MHz, 5 MHz, 10 MHz, 50 MHz, and 100 MHz. The generation of a sine wave depends on the number of points chosen, the maximum amplitude of the signal, and the clock period

Table-3. Synthesis report of sine wave generator.

Device Utilization Summary (estimated values)		
Logic Utilization	Used	Available
Number of Slice Registers	13	106400
Number of Slice LUTs	13	53200
Number of fully used LUT-FF pairs	13	13
Number of bonded IOBs	9	200
Number of BUFG/BUFGCTRLs	1	32

Table-3 shows the synthesis report or hardware device utilization summary of the sine wave with a 3.125Mhz signal in zed board FPGA. Zynq 7020 FPGA

board works on 28nm technology and it has programmable logic (PL) and processing system (PS). Several slice register is utilized 13 and the slice Lookup table is 13 and input-output blocks are 9 and it can be verified with the RTL diagram in figure 2. Now let us analyze the timing values of the design. The total combinational time delay for the design is 0.9ns through which logic takes 0.285ns and the routing takes 0.615ns. The maximum frequency of the board is 1000Mhz. The maximum output required time after clock pulse is 0.511ns through which logic is 0.232ns and the routing is 0.279ns.

4. XILINX DDS CORE GENERATION

Figure-3 shows the Xilinx DDS[9] 5.0 IP core to open the IP core the following steps should be open the Xilinx ISE or Xilinx Vivado[10] suite then click file click New project under the project give the name of the project and specify the device details then click IP(Core generator & architecture wizard) then a figure will appear, many IP cores are available in it use the Math functions followed by Trig functions followed by the DDS compiler 5.0. There is an option to use a CORDIC based algorithm to generate the sine wave using an IP core. From the above diagram, the input pins that are disabled are optional to use and the enabled input like aclk, "aclk" shown in the RTL through the IP core is the rising edge clock signal. s_axis_phase_tvalid is the input signal for the phase channel. S_axis_phase_tdata is the input signal of 16 bit width. Out of the 16 bit width, the first 11 bits from LSB are used and the 12th bit to 15th bit is unused. For example the input data 1011 101100110101. The yellow coloured data is the input data and the red coloured data is unused when SIN/COS is configured for the output. M_axis_phase_tvalid is the output TVALID phase channel. M_axis_phase_tdata is the output phase channel. After the IP core instantiation, the output results are shown in the X-Sim simulator. The IP core instantiation RTL parameters and the X-Sim simulation window parameters are the same. Figure-4 shows both the sinusoidal and cosine waveforms in a single output window.

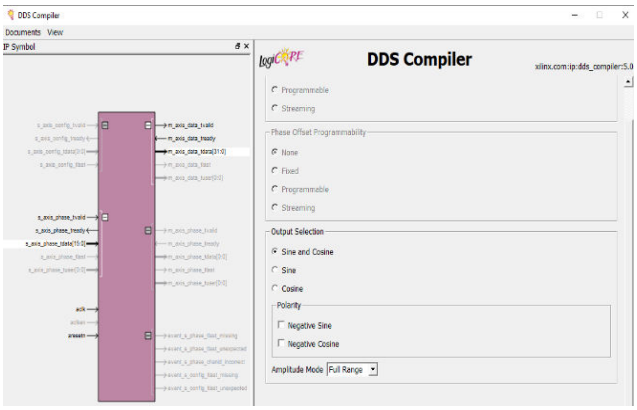


Figure-3. DDS Core sine wave generation.

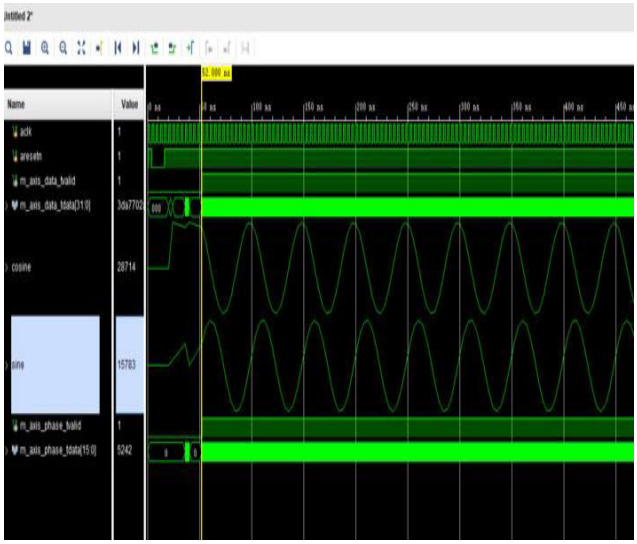


Figure-4. Sine wave simulation output using Xilinx IP Core.

Figure-5 shows the common source amplifier using CMOS technology. Micowind is the backend tool used for designing the layouts of the circuit diagram. The microwind tool using 45nm technology is used for designing the common source amplifier circuit. The length and width of the transistors are chosen at 1000µm and 100 µm respectively. The number of fingers is 5 for NMOS FET and PMOSFET. Power supply (VDD+), ground (VSS), Capacitor, in(Input voltage) and Vout(Output voltage) can be observed in the figure. All the connections are made as per the current mirror CS amplifier. After making all the connections DRC rules have to be checked and then the output window will appear which is shown in Figure-6. The green colour is the input waveform and the red coloured waveform is the amplified version of input for the CS current mirror amplifier. The power dissipated is shown as 1.884mWatts.

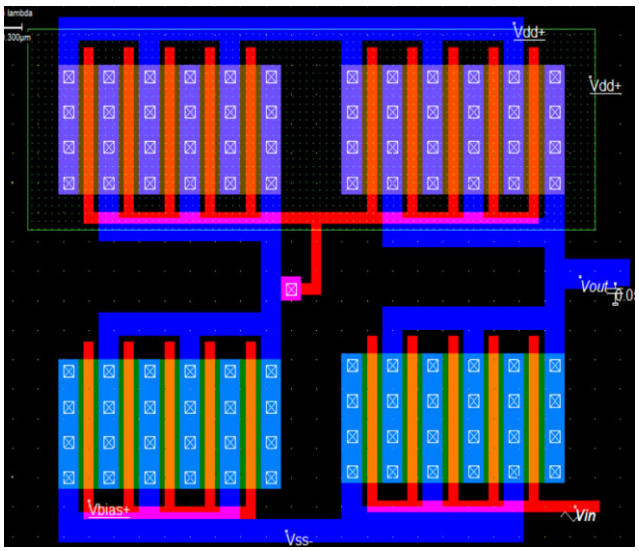


Figure-5. Common source Amplifier using CMOS technology.

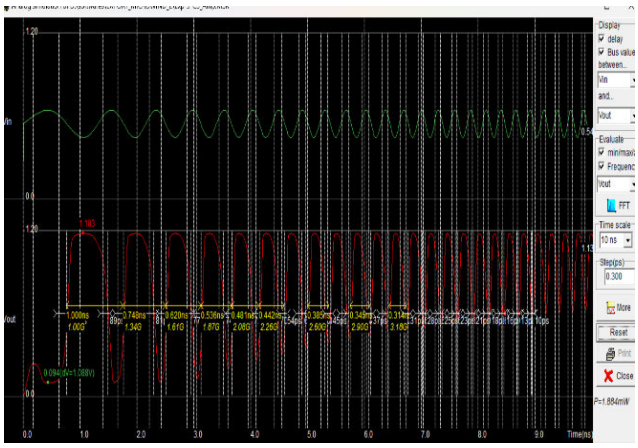
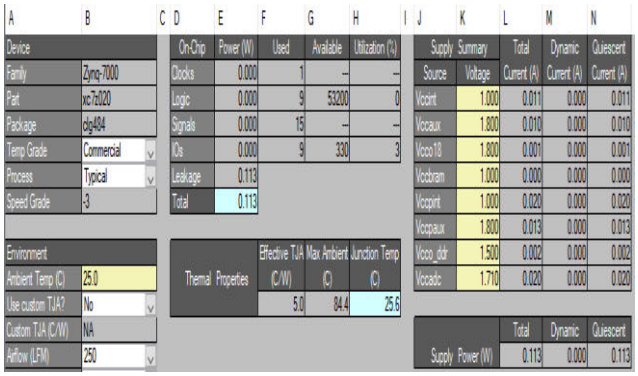


Figure-6. Output of common Source amplifier.

Figure 7 shows the power report of the sine wave generation using 3Mhz frequency. The Zed board FPGA device details and its family XC7z020 are shown in the diagram along with the input-output blocks i.e. 9. To generate a power analysis of the design .pcf file is required. The total power of the design is 0.113 watts.



Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Zynq-7000	Clocks	0.000	1	--	--
Part	xc7z020	Logic	0.000	9	53200	0
Package	clg484	Signals	0.000	15	--	--
Temp Grade	Commercial	IOs	0.000	9	330	3
Process	Typical	Leakage	0.113			
Speed Grade	-3	Total	0.113			

Environment		Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
Ambient Temp (C)	25.0		5.0	84.4	25.6
Use custom TJA?	No				
Custom TJA (C/W)	NA				
Airflow (LFM)	250				

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.011	0.000	0.011
Vccaux	1.800	0.010	0.000	0.010
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.000	0.000	0.000
Vccpint	1.000	0.020	0.000	0.020
Vccpaux	1.800	0.013	0.000	0.013
Vcco_ddr	1.500	0.002	0.000	0.002
Vccadc	1.710	0.020	0.000	0.020
Supply Power (W)		Total 0.113	Dynamic 0.000	Quiescent 0.113

Figure-7. Power report of Sine wave.

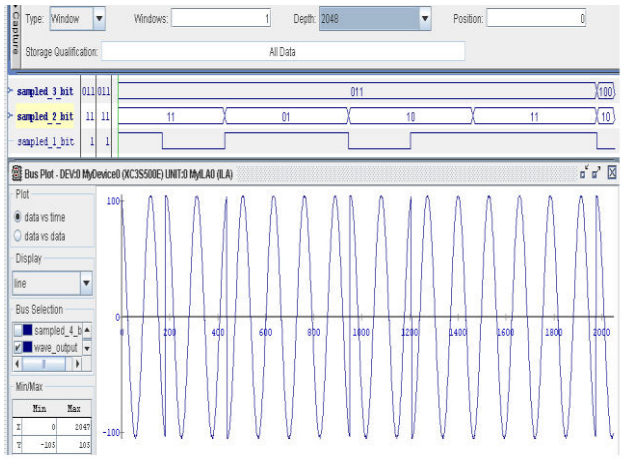


Figure-8. Sine wave generation on FPGA.

Figure-8 shown above is the FPGA implementation of the sine wave after loading a bitstream file into the Zed board FPGA. The 3 most important Intellectual Property Cores (IP) in Xilinx should be instantiated to use the on-chip verification of any signal on the output screen (Laptop/Desktop). ICON, ILA, and VIO are the IP cores used to use the debugging tool chipscope pro analyzer. ICON stands for the integrated controller. ILA stands for Integrated Logic analyzer and VIO stands for Virtual input and output.

5. COMPARATIVE ANALYSIS

Many researchers proposed trigonometric functions on FPGA the below table shows the comparative table of the proposed work with the existing work.

Table-4. Comparison with existing work.

Parameters	Al-Safi et al [5]	Mohammed et al [11]	Proposed work
Number of LUTs	1586	49	13
Number of Flip flops	71	49	13
Number of Bounded IoBs	37	17	9
BUFG	2	1	1

The number of Lookup tables for the proposed work is 13, the Number of Flip flops is 13, Input-output blocks are 9, and Buffer memory is 1. From table number 3 it is observed that the hardware device utilization summary report in the proposed design is much less as compared to the existing one.

6. CONCLUSIONS

FPGA Implementation of sine wave signal is simulated synthesized and targeted on the zynq 7-series FPGA board. The hardware device utilization summary is tabulated and the timing values of the design are measured. Power analysis of the design is verified with 113mw. The trigonometric functions sine and cos are simulated and synthesized using the Xilinx IP core method. Microwind software is used for the generation of sine waves and the amplification of sine waves. The comparative study of the proposed work and the existing work is shown.

ACKNOWLEDGMENT

The authors would like to thank the VLSI Design Lab, Department of Electronics and Communication Engineering, Chaitanya Bharathi Institute of Technology (CBIT), Hyderabad for providing co-operation and laboratory facilities to carry out our research work.

Conflicts of interest

The authors have no conflicts of interest to declare.

REFERENCES

[1] https://www.daycounter.com/Calculators/Sine-Generator-Calculator.phtml

[2] Upadhyaya B. K. 2009. Design and Development of VHDL Based Tuneable Sine Wave Generator Using DDS Technique: Extension to FPGA Implementation. NCC 2009.

[3] Bohrn Marek, Lukas Fujcik and Radimir Vrba. 2011. Novel on-chip sine wave generator. 2011 34th International Conference on Telecommunications and Signal Processing (TSP). IEEE.

[4] Liu, Zeliang. 2013. Design of a typical waveform generator based on DDS/SOPC. Proceedings 2013 International Conference on Mechatronic Sciences, Electric Engineering and Computer (MEC). IEEE.

[5] Al-Safi Amean, Ali Al-Khayyat and Zeyad Aklah. 2021. FPGA-based implementation of MSPWM utilizing 6-input LUT for reference signal generation. 2021 IEEE 11th Annual Computing and Communication Workshop and Conference (CCWC). IEEE.

[6] Lakka Matina, Eftichios Koutroulis and Apostolos Dollas. 2013. Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters. IEEE Transactions on power electronics. 29.1: 356-365.

[7] Liu Yidong, Lihang Fan and Tieying Ma. 2014. A modified CORDIC FPGA implementation for wave generation. Circuits, Systems, and Signal Processing. 33: 321-329.

[8] Yang Heein, *et al*. 2014. Implementation of DDS chirp signal generator on FPGA. 2014 International Conference on Information and Communication Technology Convergence (ICTC). IEEE.

[9] Rehman B. Khaleelu, *et al.* 2022. Xilinx FPGA and Xilinx IP Cores: A Boon to Curb Digital Crime. Digital Forensics and Internet of Things: Impact and Challenges (2022): 131-162.

[10] Rehman B. Khaleelu, *et al*. 2022. FPGA Implementation of Area-Efficient Binary Counter Using Xilinx IP Cores. Sustainable Infrastructure Development: Select Proceedings of ICSIDIA 2020. Singapore: Springer Singapore, 2022. 147-156.

[11] Mohammed, Raya K. and Hamsa A. Abdullah. 2020. Implementation of digital and analog modulation systems using FPGA. Indonesian Journal of Electrical Engineering and Computer Science. 18.1: 485-493.