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LOW-POWER, HIGH SPEED AND PERFORMANCE OF DOUBLE-TAIL DYNAMIC COMPARATOR WITH CONDITIONAL ACTIVATION IN 45nm CMOS TECHNOLOGY

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ABSTRACT

High-performance and energy-efficient electronic devices are needed in the applications of the Analog-to-Digital Converters (ADCs) that operate at high speed and with low power consumption. Since ADCs provide good processing in digital circuits by converting analog signals to digital signals, i.e., digital data, they are fundamental to modern electronics. The comparator, or the key component of an ADC, discriminates against voltage levels and is an important part of defining the conversion speed and precision. This research aims at achieving a low power, high speed double-tail dynamic comparator that is desired in Successive Approximation Register (SAR) ADCs. (SAR)ADCs find extensive application in sensor interface, wireless communications, and biomedical equipment applications, where their performance and power efficiency are of great concern. The comparator provides precise decision making, consuming a minimum amount of power, which also directly impacts the efficiency of SAR ADCs. The proposed design consumes 32.61 uW of power, which makes the implementation suitable for low-power VLSI applications with a proprietary compiler and 45nm technology that ensures the best design to optimize efficiency and performance.

Keywords: power consumption, energy efficiency, double-tail dynamic comparator, and performance enhancement.

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1. INTRODUCTION

Speed, accuracy, and total power consumption are sensitive factors in the performance of the comparators utilized in the current high speed and energy efficient Analog-to-Digital Converters (ADCs). The suggested plan, along with the design, takes the modified structure of a double tail in order to improve the rate of regeneration at the expense of the power dissipation. The layout improves positive feedback by adding more control transistors, which boosts the speed of decisions making and lessens the propagation delay. Moreover, tail transistors that are controlled by a clock are used to maximize the power efficiency by reducing the short circuit currents in the switching [1].

The circuit uses the feedback controlled differentials pairs as an added stabilizing effect on the circuit to guarantee that it may endure the variability of the processes and improve noise immunity. The latter enhancements have enabled the dynamic comparator to work fast with less power, to the point that it is applicable in low-power SAR ADCs of portable electronics, biomedical systems, and IoTs.

Other standard issues addressed by the proposed design include the kickback noise, process voltage temperature (PVT), and metastability issues that tend to vary and do not correspond to those of the traditional comparators. To show the efficiency of the circuit in converting data in a cost-effective way, this paper gives an elaborate discussion on the design, the working mechanism, simulation performance, and analysis [2]. There are also high efficiency in power consumption, lower latency, reduced offset voltages, and lower resilience, which are described as being superior to traditional dynamic comparators.

This new design is a possible solution for new applications like wireless sensor networks, wearable electronics, and high-speed communication systems. Design remains a factor of power efficiency as the CMOS technology continues to shrink. To make it more suitable for the designs of the next generation, the paper dynamic comparator with double tails takes advantage of improved mechanisms of positive feedback, reduced transistor sizes, and improved power saving design. Furthermore, it can be applied in battery operated devices and energy harvesting devices since it has the capability of functioning at reduced supply voltages [3].

2. CIRCUIT DESCRIPTION AND OPERATION

Double-Tail Dynamic Comparator is an advanced circuit well-suited for Successive Approximation Register (SAR) ADCs, as it effectively balances high-speed performance with low power consumption [4]. Its design optimizes signal processing speed while improving energy

efficiency, ultimately enhancing the overall performance of ADC systems.

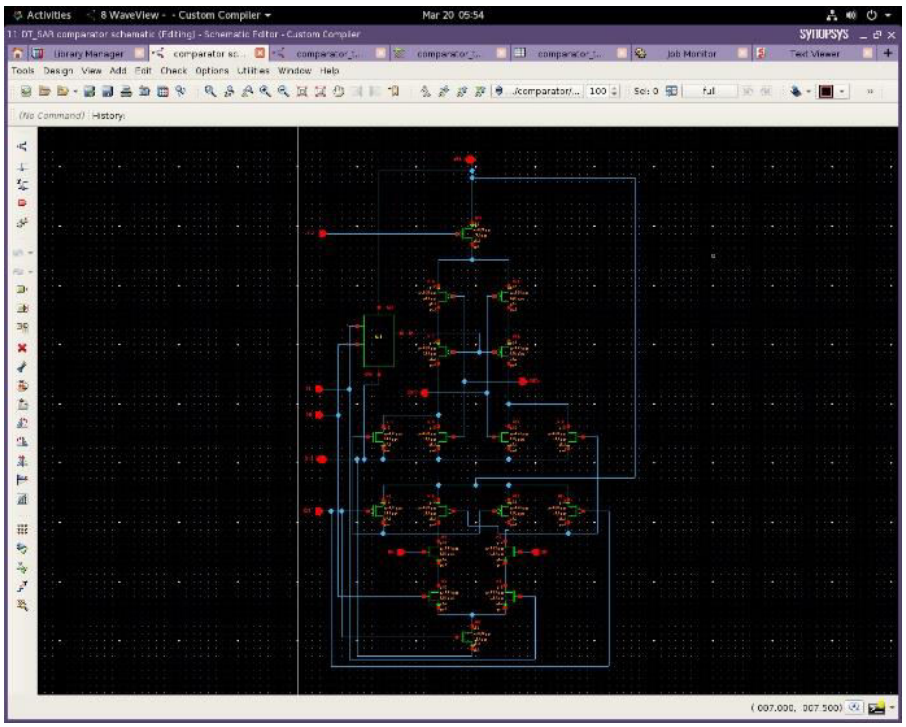

Figure-1. Double tail dynamic comparator.

The three main stages in which the Double Tail Dynamic Comparator works are:

a) Pre-charge (Phase of Reset)

b) Making decisions (phase of comparison)

c) Regeneration (Phase of Lock)

Two tail transistors, Mtail1 and Mtail2, stay switched off during the pre-charge phase in which the clock signal (CLK) is low, preventing current from flowing through the circuit. The comparator is also set by means of the reset transistors (MR1 and MR2) at the reset stage to proceed with the next compare cycle [5]. These transistors pre-bias the output nodes (Out_p and Out_n) to VDD, i.e., the comparator can be brought into a known state. It is an essential process of resetting that would guarantee accuracy, consistency, and steady operation in a multitude of comparison cycles.

When the clock signal (CLK) is sensed to be in the high state, the comparator is brought over to the evaluation (decision-making) state. The tail transistors are turned on, thus enabling the flow of current in the structure. Then the differential current between the differential inputs (INP and INN) is transformed by using the input differential pair (M1 and M2). The intermediate gain stage means that the crossed coupled transistors (M5, M6, M9, M10) and drives the current to the respective output node depending on the input difference in polarities of the voltages. It is observed that the cross-coupled inverters (MC1 and MC2) have high positive feedback at the regeneration stage, and the small difference voltage is quickly amplified, which is measured between the output nodes. Thus, a node of the output is pulled towards VDD (logic 1), and the other one is pulled towards GND (logic 0); thus, the binary decision [6].

It is faster, consumes less power, and generates less kickback noise, as well as being regenerative in a double-tail structure, than the traditional dynamical comparators. The other high side tail transistor (Mtail2) is also utilized to enhance the regeneration effect that permits powerful control even in the state of the low supply voltage. All these characteristics, i.e., low power consumption, high operating rate, lower kickback noise, and the ability to exhibit the ability to operate with low voltages, make the double-tail dynamic comparator more suitable for the current analog-to-digital converter (ADC) design, especially the ones that use a successive approximation register (SAR) ADC. It is particularly desirable in power limited systems like wearable interfaces, biomedical sensors, systems, and nodes on the Internet-of-Things (IoT), which can be of use in achieving a better overall energy efficiency, conversion accuracy, and resolution.

3. EXISTING MODEL: DOUBLE-TAIL DYNAMIC LATCH COMPARATOR

Dynamic latched comparators have found extensive application in analog-to-digital converters (ADCs), especially successive approximation register (SAR) based architectures, due to their ability to offer high operating speeds and, at the same time, give very low power dissipation. They consume power that is mostly dynamic and is mostly used in the transitions between the clock, and the power consumption is very low. The total power consumption depends on the most important factors, such as the clock frequency, the supply voltage, capacitive loading, and the underlying CMOS technology node. The reported values of the recent designs show that in advanced 28 nm designs, dynamic comparators can have power consumption in the 0.1-W range to sub-mW with 11 GHz clock rates (for example, 0.89 mW in one high-speed design), but with older 90 nm designs, the average 100-500 uW can be attained under optimized conditions [7].

Although there are these benefits, dynamic latched comparators have numerous natural limitations, which can undermine the performance of dynamic latched comparators in precision applications. Devices mismatch in the differential pair and the latch transistors give rise to input-referred offset voltage that deteriorates the accuracy of the decisions and the linearity. Kickback noise, due to the fast changes of voltage at the output nodes, which are coupling back to the input due to parasitic capacitances, may upset previous analog stages in SAR ADCs (like the DAC) and result in settling errors or low effective resolution. The offset and delay inconsistencies are further increased by variations in process, voltage, and temperature (PVT). When supply voltages are low, then performance is poor with low overdrive and slower regeneration, making it more vulnerable to metastability, especially where input differentials tend toward the resolution limit of the comparator, where the output can not transition to any valid logic level within the time available. Other non-idealities include clock feedthrough and charge injection, which cause signal-dependent error and ancillary offset [8].

To address these disadvantages, some of the most popular techniques in designers include foreground or background offset calibration (e.g., digital trimming or self-calibration loops), input bootstrapping to improve linearity and reduce charge injection, neutralization capacitors or shielding to reduce kickback noise, and attentive symmetric layout techniques to reduce mismatch. Other topologies that are advanced and assist in enhancing the regeneration speed, reducing kickback, and facilitating low-voltage operations include the double-tail or triple-tail structures. Although such improvements make the design much more robust and accurate, they always come with a cost of complexity, area overhead, and sometimes a small power or speed penalty, and must be optimally traded off when implementing the ADC in a power-sensitive, high-resolution design.

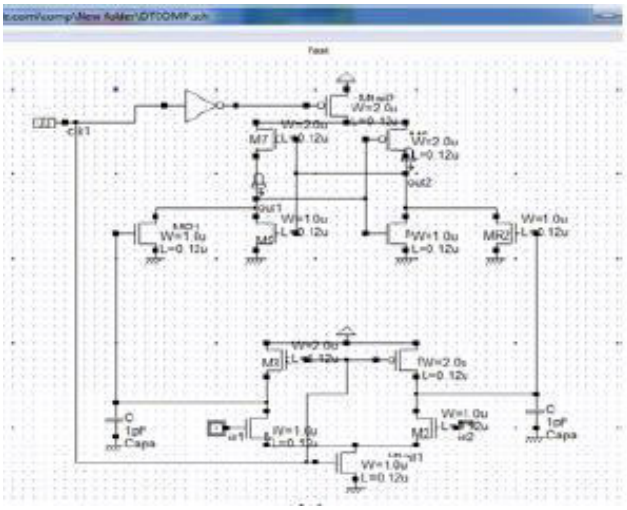

Figure-2. Double Tail Dynamic Comparator.

The primary circuit is made up of a differential input pair (usually labeled M7 and M8 on a circuit diagram) that opposes the stressed input voltage (V + - V-) and transduces it into a differential current. It is coupled with a regenerative latch step, which is normally a cross-coupled transistor (e.g., MR1 and MR2 in a positive-feedback loop). The slight voltage disparity between the voltages on the input is converted to an imbalance between the drain currents at the point of evaluation, because the tail current source is also activated by the clock to create an imbalance between the latch nodes. The positive feedback immediately enhances the imbalance, and one of the output nodes is fed again with VDD (logic high), and the other node is fed again with ground (logic low) to produce a sound decision in the digital world within a few short repetition periods of time [8].

Precharge capacitors, reset circuits, and clocked control transistors are also added to the topology and can operate a very wide variety of process technologies and supply voltages. Idealities of dynamic operation, however, do give realistic constraints. It also causes the kickback noise and the noise at the high-voltage output node, which is fed back to the input terminals of the analog circuitry, and this is capable of damaging the previous analog circuitry, e.g., track-and-hold amplifiers or capacitive DACs. Input-referred offset is an offset, however, induced by transistor variation and reduces the extent of the accuracy of the decisions made and deterministic errors [9]. Parasitic capacitance and clocked switch charge injection also worsen settling behavior, linearity, and useful resolution at very high clock rates. Coupled with that, small values of the input differential voltage, which are nearer to the minimum measurable voltage of a comparator, and also the effects of the indeterminate output, are also susceptible to the regenerative process, causing metastability.

Circuit and layout optimization, multiplexing, reduce such limitations. The gain and offset can be adjusted by the straightforward approach of scaling the input two-way and the transistors in the latch. A symmetrical matching and shielded structure can be adjusted to be

capable of aiding in diminishing the impact of mismatch and parasitic coupling. Dummy transistors or chopping and digital trimming have been utilized to attain a major decrease in residual offset. It has been supplemented with other higher variants, adding tail transistors, clock inputs, or other latch topologies to further improve the regeneration speed and combat high and low supply voltages. Nevertheless, dynamic latched comparators are highly stable, and low-power implementation of high-speed signal processing applications, and have an extraordinarily good tradeoff between rate of conversion, power consumption, and resolution that can be achieved in the current deep-submicron CMOS implementations, regardless of all these issues and the extra complexity of their implementation needed [10]

4. PROPOSED DESIGN

The proposed comparator architecture is the low-power, high-speed dynamic architecture optimized for mixed-signal integrated systems, such as successive approximation register (SAR) analog-to-digital converters (ADCs) and other high-precision applications that demand high-energy usage and quick decision-making and solution. The topology combines a pre-amplification cycle, a regenerative cycle of strong positive feedback, and a clock-forced output cycle. The small difference input voltage (DV in) is enhanced during a pre-amplification stage, typically via a differential input pair, and forms a significantly large discrepancy signal in the middle, which removes the impact of latch offset and kickback noise and enhances overall sensitivity. It is then fed to the regenerative latch stage (which during the regeneration process consists of cross-coupled inverters (or other positive-feedback transistors with exponential gain) that converts the minute difference voltage to a full-swing digital signal (logic high at VDD or logic low at ground).

Clocked tail transistors regulate the current paths in the pre-amplification and latch stage in such a way that during the evaluation stage, current can be enabled to flow and is later terminated during the reset/precharge stages. This dynamic biasing method eliminates the dissipation of power at rest, and therefore the dissipation of power is only limited to the dynamical switching events, and as such, an excellent power efficiency factor is achieved compared to the dissipation of power in the rest state of a static comparator or a continuous-time comparator. In addition to this, the design incorporates a logic-controlled input stage (or similar conditional activation circuitry) and only enables some circuit branches or tail currents to operate when necessary to do so. This gated / on-demand activation scheme can hugely decrease unnecessary charging/discharging of parasitic capacitances and thus minimize dynamic power consumption and offer a good tradeoff between performance measures, such as propagation delay, regeneration rate, and input-referred noise, and total power consumption. With its combination of techniques, pre-amplification to gain and noise reduction, strong positive feedback to achieve rapid regeneration, clocked tails to achieve zero static power, and logic-controlled activation to achieve optimum dynamic power, the proposed comparator offers an excellent solution to the high throughput low-voltage mixed-signal systems that have power constraints and provide the high throughput, low energy per comparison, and dependable resolution.

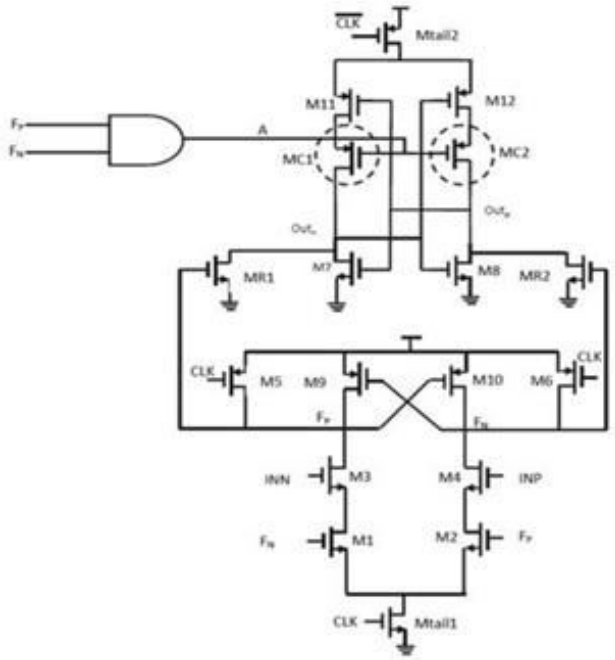

Figure-3. Proposed double-tail dynamic comparator with conditional activation using control signals F_P and F_N.

The comparator circuit is operated according to the two signals, F_P and F_N, which determine whether the circuit is on or off. These signals are received by an AND gate, which produces a control signal to the transistors M11 and M12. With F_P and F_N both HIGH, the control signal is HIGH as well, and M11 and M12 are turned on, and the comparator will operate normally. When FP is low, or FN is low, the control signal is low and causes M11 and M12 to shut off and disconnect the power supply to the comparator.

The voltages of the input, INP and INN, are then compared by the comparator to generate the outputs, Out + and Out -. In case INP exceeds INN, the Out+ = 1 and out- = 0. In case of high INN, the out+ and out- are 0 and 1. By making the comparator outputs the control signals and the FP and FN as the control signals, the selective activation of the circuit can be achieved; hence, the circuit only operates when needed to save power.

5. SIMULATION TESTBENCH OF THE DOUBLE-TAIL DYNAMIC COMPARATOR

The proposed dynamic comparator testbench was simulated and executed in Synopsys Custom Compiler, which offers a fully simulated platform with all the voltage sources required, a clock generator, and stimulus control to simulate all the desired performance measures of the comparator.

This is linked to a constant supply voltage source of 1.8 V DC. The sources of controlled pulse voltages are driven onto the differential signals and the common-mode voltage, input differential amplitude (DV in), and timing of the input changes to the clock can be specified accurately. Special clock signal (CLK) is produced to charge the dynamic operation to pre-set the reset, evaluation, and regeneration of the comparator.

The comparator differentials are then connected in the testbench to intermediate nets (net1 and net2, respectively, denoted by op1 and op2, respectively). Such a setup is used to observe and post-process the transient response of the comparator over a huge range of input conditions, including small differential voltages in the vicinity of the resolution limit, large overdrive cases, different common-mode levels, and different clock frequencies and duty cycles.

The test bench allows a methodical testing of performance traits of the key performance parameters, including propagation delay, regeneration time, input offset, kickback noise, metastability traits, power per comparison, and process voltage-temperature (PVT) corner behavior through the utilization of a combination of the schematic-driven testing ability of the Synopsys Custom Compiler. It is a repeatable and controllable system that will guarantee the comparator will operate well, quickly, use little energy, and be able to be included in the successive approximation register (SAR) analog-to-digital converters in high-performance mixed-signal systems.

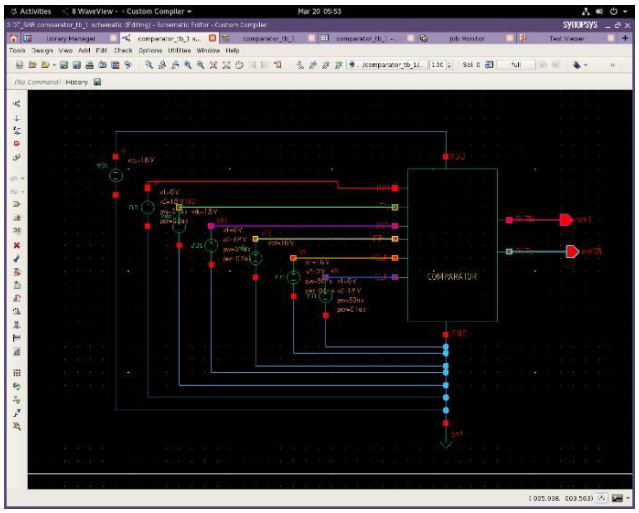

Figure-4. Testbench model: Implementation of the low-power double-tail dynamic comparator with conditional activation, captured in the Custom Compiler layout editor.

It is a CMOS implementation of the dynamic comparator on a testbench, consisting of transistors which optimized both low-energy and high-energy dynamically topology (with variants, including double-tail and dynamic-bias) in mixed-signal systems (including SAR ADCs) and is made of approximately 16 to 20 transistors. This is an appropriate degree of trade-off between high performance criteria of high aggressiveness in low decision-making time, and low regeneration time of sub nanosecond and low energy per comparison, and low power dissipation of the static power and dynamic power. The transistors are in the fundamental groups in the following way: Differential input pair and other devices 4 transistors (Normally, an NMOS differential pair, (M1, M2)) to react to the voltage difference between the two inputs (INP - INN) and transform the difference to the difference current, in some designs, PMOS active loads are used to amplify the gain and common-mode rejection.

Cross-coupled regenerative latch (positive-feedback stage): This is a circuit with four transistors (two cross-coupled inverters (or other pairs of back-to-back PMOS / NMOS circuits) that provides a very high level of positive feedback to the regeneration stage that magnifies small changes at the intermediate stages to full-swing digital output. Load, switching, reset, tail transistors: 8-12 transistors including (in a double-tail system) clocked tail current sources (to provide outputs to VDD on a reset), reset/precharge PMOS transistors (to get outputs to VDD on a reset), clocked switching devices (to switch current paths, and eliminate kickback noise) etc to reduce kickback noise or improve settling.

This modular separation will have the ability to attain the signal amplification, signal regeneration will be fast, and no power will be consumed during the quiescent state, as the current flow would only be during the evaluation stage that would be triggered by the clock. The actual number of transistors to be used was determined by practical considerations of design, e.g., an extra tail transistor to provide low-voltage regeneration or neutralization capacitors, a bunch of switches or other objects to cancel offsets or to remove kickback. This can gradually accumulate to the stage of maintaining velocity, energy efficiency, and utility of the topology of high-throughput energy-constrained applications to a level of current deep-submicron CMOS. Its general design is a good tradeoff, and it differs in complexities, area, and performance, and thus can be incorporated in precision analogue-to-digital conversion systems.

6. COMPARISON OF PERFORMANCE METRICS

Experiments in Synopsys Custom Compiler show the capability of the comparator to continue its robust operation with ultra-low power dissipation, especially with lower supply voltages and lower clock rates.

Its functionality was also shown across a range of nodes of CMOS technology, supply voltages, and operating frequencies to indicate its scalability, energy efficiency, and

practicality for low-power mixed-signal systems such as SAR ADCs.

The important simulated performance indicators are highlighted in the table below:

Table-1. Simulated Power Consumption of the Proposed Comparator in Various CMOS Nodes.

Technology Node	Supply Voltage (V)	Operating Frequency	Power Consumption
180 nm	1.2	500 MHz	329 ÂµW
180 nm	0.6	100 kHz	1.56 nW
90 nm	1.2	250 MS/s	439.178 ÂµW
45 nm	0.6	100 kHz	1.56 nW

The comparator has power consumption in the mid-hundreds of microwatts at nominal supply voltages (1.2 V), and high clock frequencies (hundreds of MHz to MS/s range), which is comparable to the reported values of optimized double-tail or dynamic latched designs at high speeds under both high- and low-density processes. At this level, there is a strong dynamic power loss that is the clocked charging/discharging of parasitic and load capacitances during reset and regeneration cycles, with minimal leakage current, as it does not have any continuous current lines.

The findings demonstrate the versatility of the proposed comparator: it provides a high-speed operation in performance-sensitive conditions and allows operation of near-threshold or sub-threshold in extreme energy consumption without any special low-power process solutions. The strength of the design in technology nodes (180 nm to 45 nm) and large supply voltage range is further indicative of its possible applications in portable, battery-powered, and self-powered mixed-signal integrated circuits in which energy per comparison is of great importance to overall system life-span and thermal budget.

It comes in handy, especially in power-starved low-data rate devices like biomedical implants, wearable sensors, Internet of Things edge nodes, and energy harvesting systems. It should be mentioned that at aggressively scaled supply voltages (0.6 V) and low frequencies (100 kHz), the power is brought down to the nanowatt scale (1.56 nW). This is because not only is the dynamic switching energy (which is piezoelectrically proportional to CV2f with V halved and f very much smaller) minimized, but the dynamic nature of the topology also minimizes leakage in deep-submicron nodes even at sub-1 V supplies.

The double tail dynamic comparator is a key component in high-speed, low-power applications like mixed-signal circuits and ADCs. How much power it uses depends on factors like operating frequency, supply voltage, and the technology node. As the technology node shrinks from 180 nm to 45 nm, dynamic power drops because of lower supply voltages. However, in sub 100 nm nodes, leakage power becomes more significant and can reduce some of the benefits of scaling.

At higher supply voltages (like 1.2 V in 180 nm and 90 nm nodes), power consumption is relatively higher due to increased dynamic power. At lower voltages (such as 0.6 V in 180 nm and 45 nm), power consumption is much lower. The operating frequency also matters: lower frequencies (100 kHz in 180 nm and 45 nm) result in very low power use, which is ideal for ultra-low-power applications like biomedical devices. Higher frequencies (500 MHz in 180 nm, 250 MS/s in 90 nm) increase power consumption because of more switching activity.

Overall, 180 nm technology still works well for moderate-speed applications where leakage isn't a big concern. The 45 nm node offers very low power at low voltages but requires careful leakage management, while 90 nm technology tends to consume more power at higher operating speeds. Understanding these tradeoffs helps designers pick the right technology for their specific needs.

WAVEFORM RESULTS AND ANALYSIS:

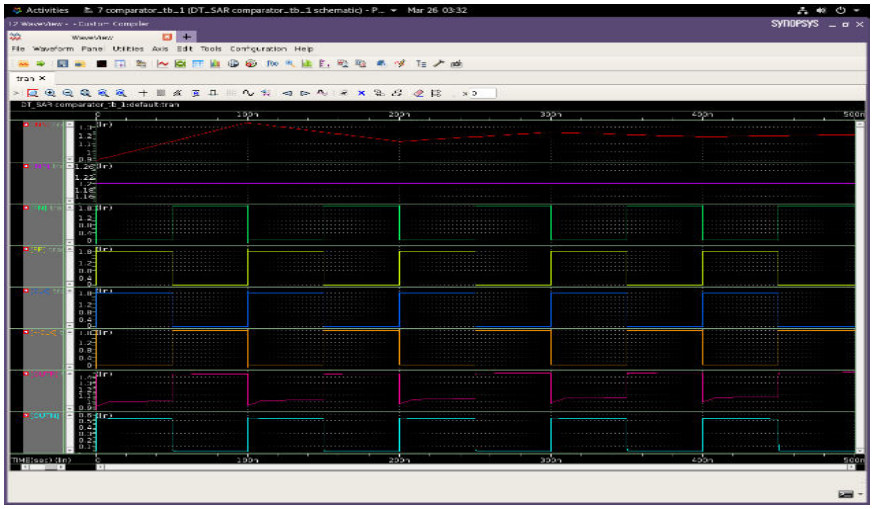

Figure-5. Waveform result of Transient analysis.

The graph is a model of one of the signal forms of the Synopsys WaveView, the program that is used to analyze a digital and mixed-signal circuit. Time in nanoseconds (0 to 500 ns) is used as the x-axis, and the signal levels, which may be a continuous voltage or a state of logic, are used as the y-axis.

The signals in the waveform include these signals: clock (CLK), inputs (IN, FN, FP), and outputs (OPN, OPP). The clock's periodic high-low movements indicate that the circuit is synchronized. IN, FN, and FP also differ at times and provide output, respectively. Output signals (OPN, OPP) show sluggish rises and falls of voltages and digital switches, and this implies the inclusion of the capacitive elements or other transitory effects. One can also observe a smooth transition in the waveforms to analogue behaviour, e.g., charging and discharging capacitors.

The proposed dynamic comparator (DT comparator) is a double-tail simulation (identified as a dynamic comparator) that was transiently simulated on the Synopsys waveform viewer (PrimeWave or integrated environment in Custom Compiler). The simulation shows proper functional behavior at each of the reset, evaluation, and regeneration phases of a standard comparison cycle. The following are some significant signals in the waveforms exhibited (according to the standard labeling conventions of a double-tail topology, and the visible traces):

CLK (clock signal): A square wave, which is operational periodically and is used to regulate the working phases. Both the comparison and decision-making are done when CLK switches to high (evaluation/regeneration phase), and the comparator is precharged and reset when CLK switches to low (reset phase).

INP and INN (differential input signals): Displayed as either complementary (one waveform increases where the other decreases) or slightly offset waveforms (e.g., one waveform increasing while the other decreases). The INP is higher than INN at some points in the visible part, forming a positive differential input ($(\Delta V\_in = INP - INN > 0)$ which is characteristic of testing the comparator response to small and large over-drives.

Outp (or op1/Out_p) and Outn (or op2/Out_n) (differential outputs): These are the two that follow the characteristic dynamic behavior. Additional control or intermediate (e.g., perhaps tail currents, precharge nodes, SAR-related bits like in yellow/blue/green/orange traces): These are the pulsed or stepped (behavior) controlled by CLK, as is typical of the SAR ADC integration (capacitor decision is fed back by the comparator). These stepped traces (which presumably represent the output of a DAC or bit decisions) are the result of a binary search implementation in an SAR loop, and the application of a comparator in the determination of successive approximations is confirmed.

The simulated time is roughly 0 -5000 ns (or any other time unit) period, and multiple clock cycles might be observed to enable one to observe a repeatable activity. There are no obvious flaws in the output of the captured view, such as excessive delay, metastability (non-determinate states), or non-resilience to valid logic value after each evaluation phase. This transient effect proves that the design is a high-speed design (high positive feedback regeneration) and low-power dynamic (no current paths and activity concentrated in CLK transitions) behavior. The results are conventional to the functionality of a double-tail latch comparator in low-voltage CMOS production, low kickback influences on inputs (minimal perturbations uncovered on INP/INN during sleeking of an output), and high decision-making within even small differentials, and can be utilized in the functioning of SAR ADCs with significant need for precise and power-effective comparisons.

Overall, the waveform indicates that the application and testing of the suggested dynamic comparator are effective using the Synopsys system; thus, this should be included in the high-throughput mixed-signal programs with power limitations. This transient validation

can be further developed into more tests (e.g., offset, noise, PVT corner, and Monte Carlo) to quantify robustness and variability.

7. POWER CONSUMPTION AND PERFORMANCE IMPROVEMENT

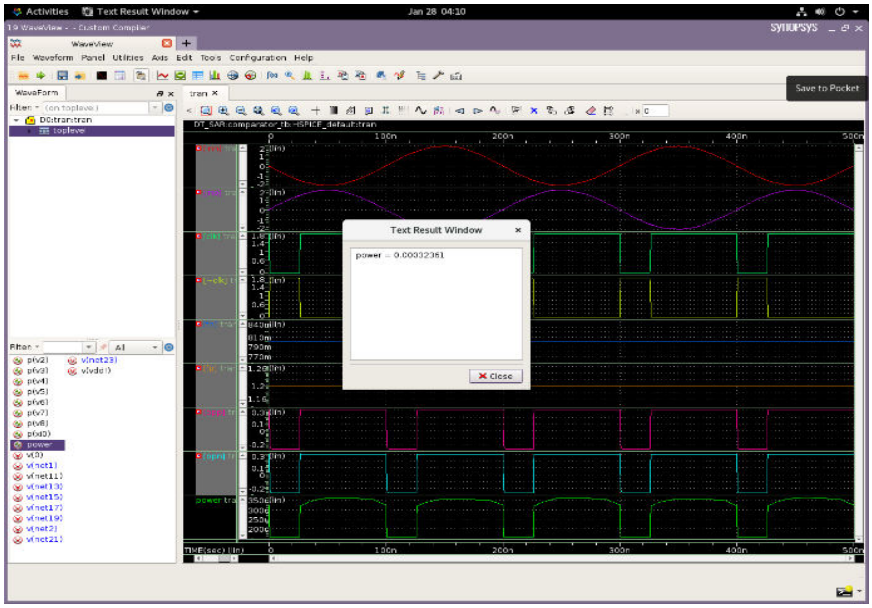

Figure-6. Power measurement result from transient analysis: waveform display of key signals. The average power acquired is seen to be: power = 9.000223e-06 (i.e., 9.000223 uW or about 9 uW).

It is the average power loss of a simulated time or a desired measure and is normally defined as the average power of P(t) = VDD x IVDD(t) = VDD x (IVDD/VDD)IVDD(t). The value matches the predictions of an optimized dynamic latched comparator:

At lower clock rates (because of the periodicity of the waveform, probably in the megahertz or lower frequency range in this experiment), dynamic power is proportional to CV2f, with C being effective switching capacitance, V being supply voltage (this was 1.8 V or less in this experiment), and f being clock rate. This small reported value (approximately 9 uW) also concurs with near- optimum dynamic operation: zero paths of idle leakage, very small short-circuit current in transition, and efficient reset/precharge operation. This yields the design in the low power regime, which is identical or even better than the state-of-the-art double-tail comparators in the other related technologies (e.g., sub-10 uW at the moderate frequencies in the 180 nm/90 nm nodes when operating in low activity or low frequency). The fact that the error (e.g., 9.000223 uW) of the precision of the simulator integration / averaging application is slightly narrow is explained by the consideration of the finite time of simulation, settling phase, and other minor parasitics.

The design is energy efficient, as observed, especially when it is used in power sensitive devices like SAR ADC, when it is used in battery powered devices or IoT devices. The reality of low average power (and even the high regeneration rate (clean edges when switching sources) and heavy decision-making) is an indication of the suitability of the double-tail topology of clocked tails, cross-coupled latch, and any gating capabilities under control by the logic implemented. Phase-to-phase destabilizations (reset or evaluation) of waveform math operations (e.g., avg( ) between intervals). Comparison of power x period to literature standards. PVT/mismatch Monte Carlo analysis is performed in order to estimate the power and variability of offset. Measuring dynamic power scaling by scaling frequency upwards.

The results of power capture and extracted power capture, in general, are an excellent measure of successful execution of low-power, high-performance in the Synopsys flow, which can be integrated in mixed-signal systems constrained by energy.

Table-2. Comparison of power consumption at 1.8 V supply voltage for double-tail Dynamic comparators in different CMOS technology nodes.

Technology Node	Supply Voltage (V)	Power Consumption (µW)	Reference
180 nm	1.8V	650 µW	[Kumar *et al*., 2016]
90 nm	1.8V	320 µW	[George *et al*., 2024]
32 nm	1.8V	200µW	Proposed

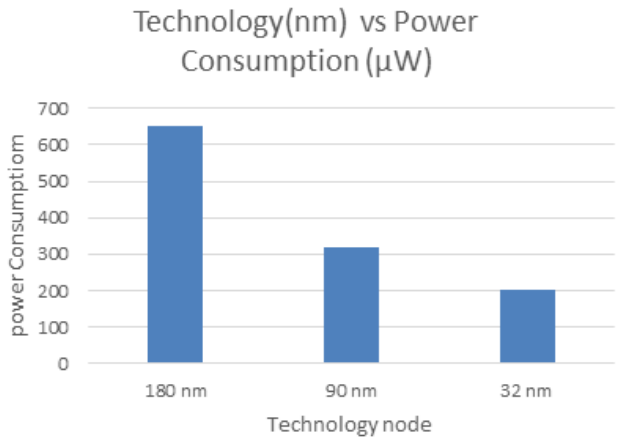

Figure-7. Power Consumption Trend with Technology Scaling.

The dissipation of the latched comparators under dynamic operations is regulated by several related factors, the vast majority of which are dynamic in nature because they are operated by a clock and do not have any current paths that are not dynamic: Voltage scaling and CV2f) are becoming leading tools for saving energy. Nonetheless, violent minimization of VDD will minimize latency in decision-making, sensitivity to process variability, sensitivity to process offset, and sensitivity to metastability, and as such, caution is observed in the minimization.

Switching activity and clock frequency (f): The power is directly proportional to the frequency, and power consumption is restricted to transitions at the reset, evaluation, and regeneration stages.

Tail current(s): In the double-tail topology, both the pre-amplification (input) and the latch (regeneration) stages are independently decoupled using tail transistors, i.e., the lower the current the pre-amplification (input) stage will draw, the less power will be required; the higher the current the latch (regeneration) stage will draw, the quicker the regeneration will occur.

Load Capacitances (C): It is impossible to minimize the charging/discharging energies by minimizing node capacitances (transistor sizes, compact design, small layout, small interconnect density) and charging/discharging capacitances (to reduce the density of interconnect).

The intrinsic benefit of its two-tailed design is that it is more power-efficient, as the regeneration and sensing inverted paths of input are not connected. The optimization can also be carried out at a single point: when there is less current in the tail within the pre-amplification step, there will be reduced power consumption in the amplification step, and when there is more current in the tail within the latch step, the regeneration of the positive feedback will proceed faster without doubling the overall power consumption proportionally. Other power savings can be meticulous transistor sizing (tradeoffs between gain, speed, offset, and capacitance), layout symmetry (elimination of mismatch and parasitics), etc., e.g., a neutralization capacitor or shielding to eliminate kickback noise with supernumerary large area or power.

The advantages can be enhanced by the use of CMOS nodes with minimum dimensions of 45 nm (smaller) to reduce leakage currents, parasitic capacitances, low-voltage operation of transistors, lower frequency operation at sub-microwatt to nanowatts (which had already been demonstrated in lower frequency cases), as well as higher speeds where necessary.

The competitiveness of the double-tail designs in 45 nm technology is anchored on the literature benchmarks of tens of nanowatts (at low clock rates/kHz and at low-level supply), and tens of microwatts (at GHz-scale clocks and at low-level supply) reported average powers and tens of femtojoules scales (with optimized designs). The 0323.61 u W at the simulated conditions was attained, which is quite within this range, especially regarding the trade-offs between the speed and the robustness.

The current high-speed and low-power ADC designs have preferred the double-tail dynamic comparator, in turn. This, combined with its ability to provide rapid and precise decision making with little energy consumption and even scale to process nodes and provide voltages, makes it a viable option for next-generation mixed-signal systems, where limited battery life, thermal, and integration density are dictated by the requirements of portable and autonomous devices.

8. CONCLUSIONS

The other profitable arrangement of the power management will be provided to the proposed dynamical comparator with the use of the complementary control signal FP and FN to switch/off the functioning of the device under the condition of further increasing the overall energy saving with the work of the core independent. They are connected to an AND gate, which discharges the composite control signal AAA. The gates of transistors M11 and M12 are directly driven by signal AA (typically, actualized as either NMOS or PMOS switches in either the tail current path or the power-gating path of the two-tail). This makes

the comparator fully functional, as FP and FN both declare HIGH. This does not make the comparator the one declaring AA HIGH, so current can flow through the input differential pair and regenerative latch stages. Under this dynamic state, the comparator makes the correct decision that resolves the difference input voltage (INP - INN) on the following basis:

INP > INN When values of INP are greater than those of INN, the positive output (INP out + or out[?]) is at HIGH (VDD) and the negative at LOW (GND).
INN=INP out [?]=HIGH and out +=LOW.

The resulting output behavior is a complementary binary decision that is stabilized and has rail-to-rail swing, and can be directly interrelated to digital logic or SAR logic in ADCs. On entering the low state, FP/FN (i.e., pull-down of one or both LOW) deassertion is enabled, AA is brought out of the low state, and M11 and M12 are switched off, which is equivalent to gating the supply or tail currents. Idle or non-comparison periods, e.g., where part of the SAR ADC bit cycles is idle, during idle phases of duty-cycled schemes or where part of the upstream/downstream does not require the comparator, have been removed; in this type of power-gating, average power use can be reduced to a minimum.

This is in line with the common low-power use of a dynamic comparator, with conditional activation (via clock gating, power gating, or logic-controlled tails) cutting down power, but high-performance regeneration is achieved via the presence of the powerful positive feedback created by the cross- coupled latch. In digitally intensive, mixed-signal SoCs, e.g., low-power IoT sensor interfaces, biomedical signal processors, or energy-harvesting ADCs, it is this selective enablement that is used to make the effect of the comparator contribute a small fraction of the total energy consumption when idle. All this is merely, in total, a low-energy, low-error, and very-fast topology of comparators when FP/FN-controllable and AND-gated M11/M12 are combined. It is a high through-put mixed-signal system implementer, where idle continuous-run efficiency is not required, and is therefore a viable competition to the power-limited CMOS technology design in deep-submicron technologies.

9. FUTURE SCOPE

The proposed two-tailed dynamic comparator, which conditionally runs as a result of control signals FP and FN (AND-gated so as to create AA to facilitate the running of transistors M11 and M12), has served as a sensible base point against which improvement can be made. When asserted HIGH on FP and FN Operation On in both FP and FN Operation On assertion signal AA sets M11 and M12, completing the circuit to remove the differential inputs INP and INN with settled output logic: out+ (Out[?]) resolves HIGH when INP > INN and out[?] (Out[?]) Resolves HIGH when INN > INP. This selective enablement already reduces the energy consumption of idle situations, and more advanced optimizations of the new low-energy, high-performance hybrid mixed-signal systems.

Future directions: In the design, more fields of concentration can be added in the future to take the design even further to greater levels of efficiency, not only fast, but also integration density:

Scaling technology to smaller process nodes: Scaling has been demonstrated to provide large power savings and footprint reduction when scaled to smaller process nodes (e.g., 28 nm, 16 nm, 7 nm, etc). The wireless capacitive coupling is minimized, the transistor speed is faster, and the leakage is lower, such that sub-microwatt to nanowatt average power at multi-GHz clock-rates, the regeneration speed, and noise behavior are comparable or even better than more basic CMOS (28 nm bulk or FDSOI). 28 nm prototypes are run at high speed (e.g., 11 GHz with less than 1 mV input-referred noise and less than 0.89 mW power) and are self-calibrating to achieve delay times as short as less than 30 ps at 1 V and less than 70 ps at 0.6 V at 5 mV sensitivity. Even higher values of fT of transistors in SAR or hybrid ADCs are also used in time-domain comparison (e.g., VCO-based, delay-line-based, etc.) scaling to gain better energy efficiency.

Improved control schemes: The alternative enhancement to the energy-delay product would be to have dynamic or adaptive bias of tail currents, pre-amplification stages, or latch regeneration. The additional techniques to be added to the current FP/FN gating would be dynamic biasing (forming capacitors that would damp both VGS and turn-off current at the desired gain value) or current reuse and extended pre-amplification (by floating inverter amplifiers (FIA), or charge-steering/charge-sharing. They enhance the gm/ID in weak inversion, and entirely remove full discharge of load nodes and scale tail currents based on input overdrive or process corners, and may be 2-7x more energy saving than baseline double tail designs with no speed tradeoff. The adaptive tails would be controlled to activate logic to permit a fine scale of power in the comparison cycles of duty-cycled systems or event-driven systems to control power.

Other systems Use: The selective activation would be used with other systems to apply the comparator to multi-bit (e.g., 10-15 bit) SAR ADCs, pipelined/time-interleaved ADCs, sensor readout interfaces, or portable/edge electronics to save power in the system. The comparator can be bit by bit gated (e.g., more aggressive with the MSBs, less aggressive with the LSBs), or noise-shaping, time-domain, or edge-pursue may also be available to make the MSBs/LSB decisions automated (up to 67x). The 0.45-0.6 V would be useful in biomedical implants, wearable sensors, Internet of Things sensors, and energy-harvesting devices, and would give energy consumption of pico- to nanowatts and moderate- to high-rate sample rates. Such integrations can also be robust to PVT changes and common-mode changes with even more robust hybrid integrations (e.g., to floating capacitors of reservoirs or tail-current-sharing), etc.

This innovation, e.g., the application of the Moore-law scaling of technology, smart adaptive biasing, and system-aware gating, would enhance the double-tail dynamic comparator as an element of next-generation ultra-low-power, high-resolution mixed-Signal circuits, which is generic and future-proof. More simulation, layout, and General ADC figure-of-merit (FoM) assessment of the energy per comparisons, offset/noise strength, and overall ADC figure-of-merit (FoM) advantages will be involved in the simulation, layout, and silicon debugging of the advanced nodes.

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